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Implementation of Pseudo-Noise Sequence Generator on FPGA Using Verilog

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Abstract

The objective of this paper is to develop a Pseudo-noise sequence generator implementation on FPGA using verilog HDL (hardware description language). Each functional module of this sequence gnerator is designed as a separate module and is tested for functionality by using ModelSim simulator of mentor graphics. FPGA implementation of Pseudo-noise sequence generator is done in this paper. This paper involves two phases -simulation and synthesis of the Verilog codes using Modelsim PE student edition 10. 1c and Xilinx Synthesis Technology (XST) of Xilinx ISE design suite 13. 4 tool. A Verilog HDL specification can be executed in order to achieve high level satisfaction in its correctness before commencing design and may simulate one to two orders of magnitude faster than a gate level description. Model sim is a verification and simulation tool for VHDL, Verilog and System Verilog. It can simulate behavioral, RTL, and gate-level code separately or simultaneously. ModelSim also supports all ASIC and FPGA libraries, ensuring accurate timing simulations. ModelSim is known for delivering high performance, ease of use, and outstanding product support. A Pseudo-random Noise (PN) sequence/code is a binary sequence that is not truly random but has a finite length and is therefore deterministic, it is basically a periodic signal that is known to both transmitter and receiver. It appears to an unauthorised user to be truly random. The property which make pseudorandom signal truly appears to be random are as follows: Balance Property, Run Property, Correlation Property. The module of pseudo-noise sequence generator comprises of D-flipflop and XOR gate. Further research and development can be performed pseudo-noise sequence generator to enhance performance and functionality.

Keywords- Pseudo-random, Chip, FPGA, Verilog, LFSR

1. Introduction:

A Pseudo-random Noise (PN) sequence/code is a binary sequence that is not truly random but has a finite length and is therefore deterministic, it is basically a periodic signal that is known to both transmitter and receiver. Even though the signal is deterministic it appears to shave statistical properties of sampled white noise. It appears to an unauthorised user to be truly random. A truly random signal can not be predicted its future variations can only be described in statistical sense. PN generators are heart of every spread spectrum systems. In a direct-sequence spread spectrum system, each bit in the pseudorandom binary sequence is known as a *chip* and the *inverse* of its period as *chip rate*. *Compare bit rate and baud*. Each symbol or bit in the sequence is called as *Chip*. PN generators are based on *Linear Feedback Shift Registers (*LFSR). The contents of the registers are shifted right by one position at each clock cycle. The feedback from predetermined registers or taps to the left most register are XOR-ed together.

2. Pseudo-Noise sequence generator Components and Basic Operation:

A PN-sequence generator consists of D-Flip Flop and a XOR gate. In this each bit is right shifted and the output of second and third flip-flop are XORed For together and their output is fed back to the first flip-flop the sake of convenience three flip-flops are considered the block diagram is as follows:

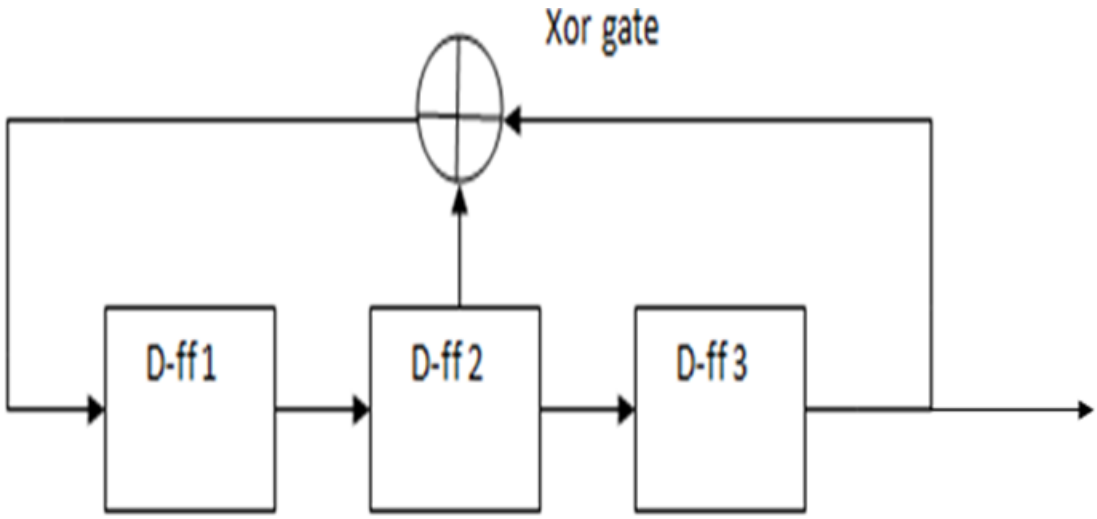

Fig. 2. 1 Block diagram of pn-sequence generator

The longer the number of stages of shift registers in the PN generator, longer the duration of the PN sequence before it repeats. For a shift register of fixed length N, the number and duration of the sequences that it can generate are determined by the number and position of taps used to generate the parity feedback bit. A maximum length sequence (L)[1] for a shift register of length N is referred to as m-sequence and

is defined as:

$L = 2^n - 1$

Where n is the number of flip-flops.

3. The property of pseudorandom signal:

The property [2] which make pseudorandom signal truly appears to be random are listed below:

- Balance Property
- Run Property
- Correlation Property

3. 1 Balance Property:

good balance requires that in each period of the sequence the number of binary ones differs from the number of binary zeros by at most one digit.

Output of pn sequence generator= +1+1+1−1−1+1−1 = +1

3. 2 Run Property:

A run is defined as a single type of digits. The appearance of alternate digit in a sequence starts a new run. The length of run is the number digits in the run. Among the runs of one and zeros in each period it is desirable that about the one-half runs of each type are of length 1, about one-fourth are of length 2, one-eight are of length 3 and so on.

000100110101111

3. 3 Correlation Property:

If the period of sequence is compared term by term with any cyclic shift of itself, it is best if the number of agreements differ from the number of disagreements by not more than one count.

000100110101111
100010011010111
daaddadaddddaaa

4. Implementation Results:

4. 1 RTL Schematic:

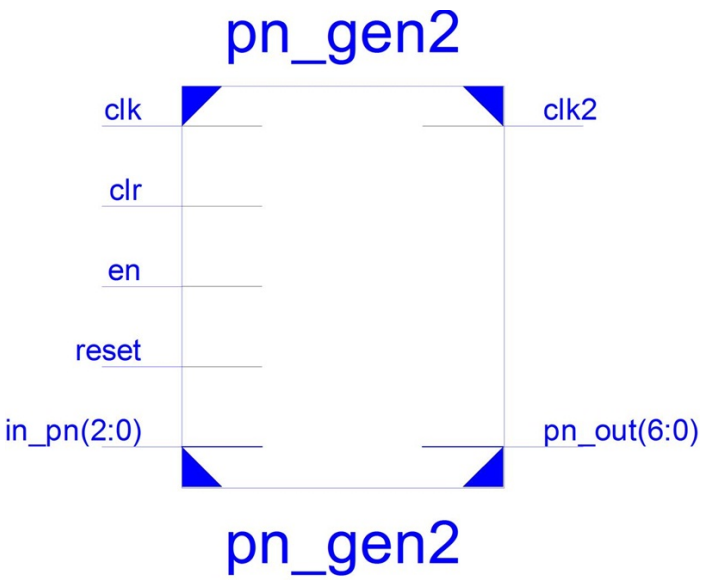

Fig. 4. 1

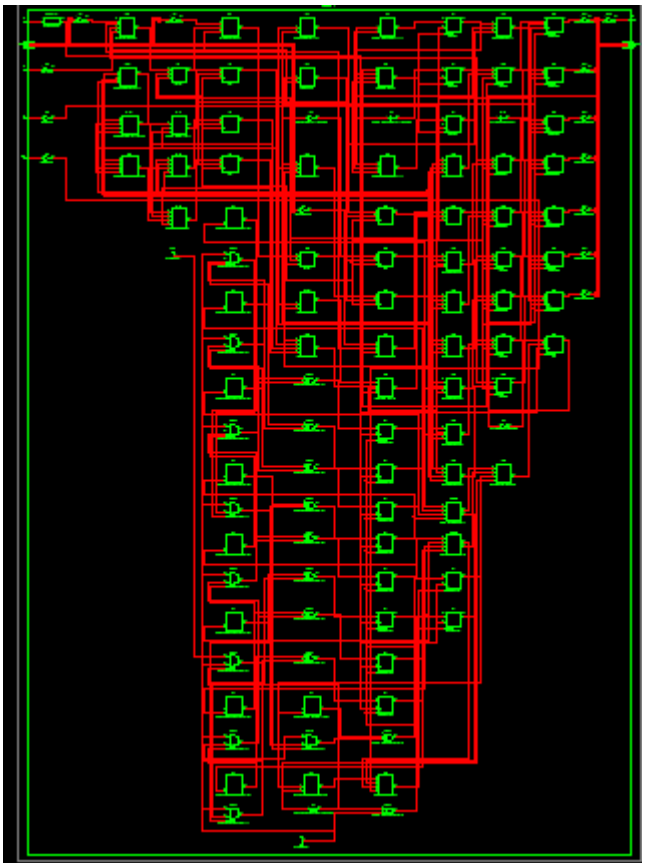

Fig. 4. 2

4. 2 Simulation Result:

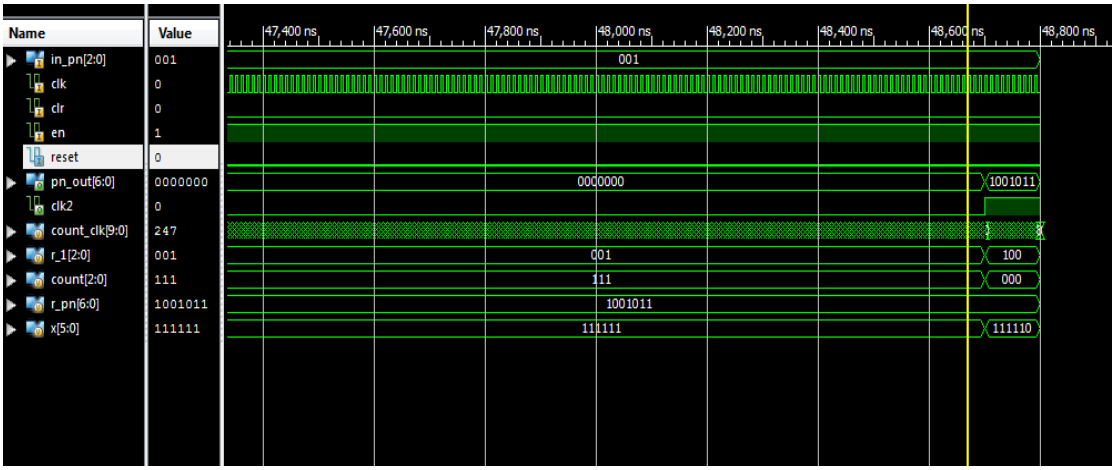

Fig. 4. 3

5. Conclusion:

In DS-CDMA system Data or message is transmitted after multiplying the data with partially random sequences generated by PN sequence generator. The major objective of this paper is to generate the spreading code i. e. coded data to spread the spectrum of information signal and this spreaded spectrum helps in suppression of the interference. DSSS(Direct sequence spread spectrum)[4] uses a signal structure in which the sequence of chips produced by the transmitter is already known by the receiver. The receiver can then use the same PN sequence to counteract the effect of the PN sequence on the received signal in order to reconstruct the information signal. “Chip” is basically continuous string of pseudonoise (PN) code symbols, each of which has a much shorter duration than an information bit. That is, each information bit is modulated by a sequence of much faster chips. Therefore, the chip rate is much higher than the information signal bit rate. Since we know that the spread spectrum technique involves multiplication of code signal with the information signal. This code signal has property similar to white Gaussian noise. White Gaussian noise [3] is a mathematical model that by definition has infinite power spread uniformly over all frequencies. Effective communication is possible with this noise of infinite power because only the finite power noise components that are present within the signal space (in other words, share the same coordinates as the signal components) can interfere with the signal. For typical narrowband signal, this means that only the noise in the signal bandwidth can degrade the performance.

PN generator produces signal at a rate of 100khz. The data signal and pn signal are multiplied to produce spreaded signal which is as follows:

$$S(t) = X(t).\ G(t)$$

X(t) is message signal and G(t) is pn signal

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