DESIGN AND ANALYSIS OF PHASE FREQUENCY DETECTOR USING D FLIP-FLOP FOR PLL APPLICATION

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Abstract

Novel design of 50T Phase frequency detector (PFD) using D Flip Flop is proposed and qualitatively compared with 52T NAND gate based phase frequency detector. Proposed 50T Phase frequency detector (PFD) design consumes significantly low power ~18% than other class of PDF. W/L of NMOS in the proposed design is kept 540/180 nm whereas for PMOS it is 1620/180 nm. Delay and power analysis of the PFD’s under discussion are done at different Vdd. Proposed 50T Phase frequency detector (PFD) using D Flip Flop design may be advantageously used in phase locked loop (PLL).

Keywords: PFD, low power, dynamic power, PLL, VLSI.

1. INTRODUCTION

The scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of Digital circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of chip. Phase frequency detector (PFD) is used as basic component for designing phase locked loop. Phase Locked Loops (PLL) has a negative feedback control system circuit. There is an increasing demand for a high frequency operation and low jitter PLL. A common architecture for clock generation uses a phase frequency detector (PFD) for simultaneous phase and frequency acquisition.
2. DESIGN DESCRIPTION

Present investigation deals with a qualitative comparison of two different logic designs of CMOS PFD’s that are sequentially depicted in fig.1 and fig.2. accommodates schematic of proposed design whereas others are used in the discussion as reference schematics. Investigators of fig.1 [ref.1] initially developed respective designs of PFD with 380nm and 180nm CMOS technology. However, to provide a fair comparison environment all the logic designs under discussion are simulated herein with 180nm CMOS technology.

52T NAND based phase frequency detector

The schematic of 52T NAND Based PFD [ref.1] is shown in fig.1. This 52T NAND Based PFD design accommodates 52 CMOS transistors which suffer from dead zone, blind zone, limited frequency range. It has slow PLL locking time and frequency. Output waveform and power of 52T NAND Based PFD is shown in fig.2 and 3 respectively. It has two outputs UP and DOWN. If the reference signal and feedback signal frequency are different then UP and DOWN signal are leading and lagging.

![Fig.1. Schematic of 52T NAND based phase frequency detector circuit](image1)

![Fig. 2. Output waveform of 52 T NAND Based PFD](image2)
50T phase frequency detector using DFF

50T Phase Frequency Detector using D Flip Flop is shown in fig.4. It is consists of two edge-triggered D flip flops which are identical to each other. 50T PFD using DFF has two inputs A and B with enable signal E. when E input at logic ‘1’ then only the PFD output comes otherwise both outputs $Q_A$ and $Q_B$ are low. Output and power waveform of 50T phase frequency detector using D Flip Flop is shown in fig.6 and 7 respectively.

Fig.3. Output power of 52 T NAND Based PFD

Fig.4. Schematic diagram of Phase frequency detector
D flip flop are used for the design of PFD which is shown in fig. 5. It is consist of 3-input NAND gate and 2-input NOR based structure. It has three inputs D, CP and rst and two outputs Q and Q_bar.

**Fig. 5.** Schematic of edge triggered D flip flop

**Fig. 6.** Output waveforms of phase frequency detector using D flip flop
3. RESULTS AND DISCUSSION

Simulation results related to the delay and power consumption of the circuits under discussion are represented in Table 1 and Table 2.

**Table 1:** Delay analysis and Transistor count for various designs

<table>
<thead>
<tr>
<th>PDF’s</th>
<th>Delay (ns) at different Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.8 V</td>
</tr>
<tr>
<td>50 T PFD</td>
<td>1.9158</td>
</tr>
</tbody>
</table>

**Table 2:** Power analysis for various designs

<table>
<thead>
<tr>
<th>PDF’s</th>
<th>Power (mW) at different Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.8 V</td>
</tr>
<tr>
<td>52 T PFD</td>
<td>0.7525</td>
</tr>
<tr>
<td>50 T PFD</td>
<td>0.7125</td>
</tr>
</tbody>
</table>

Table 2 refers that power consumption for reference PFD circuit of fig.1 is 0.7547 mW whereas it is observed 0.7149 mW for proposed PFD of fig.4. This shows that reducing the transistors from the reference design of fig.1 records 18% reduction in
power consumption for proposed PFD of fig.4. Thus the purposed PFD design consumes least power than other designs of reference a PFD at similar 180nm CMOS technology platform. This suggests that the purposed PFD designs may be adequately useful for the PLL.

4. CONCLUSION

In this paper, the main goal is to improve the performance of Phase Frequency Detector such as delay for generating output and to reduce the overall power dissipated in the circuit with less number of transistors. All circuits designed with 0.18μm CMOS technology on tanner tool and compared delay, power with 52T and 50T PFD. Due to less number of transistors, low power, and small delay 50T using D Flip Flop Phase Frequency Detector is quite useful for PLL applications.

REFERENCES


[8] Wen-Chi Wu,C,h ih-Chien Huung, Chih-Hsiung Chang’, Nui-Heng Tseng,

