HBZVR-Type Single-Phase Transformerless PV grid connected Inverter with Constant Common-mode voltage

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Abstract
Transformerless photovoltaic (PV) inverters are attractive in grid-connected applications due to the advantages of lower cost, smaller in weight and higher in efficiency compared to isolated systems. Nonetheless, reduction of leakage current should be carefully considered, when designing a transformerless inverter because of the high operational risk and high output current distortion. According to the international standards, the leakage current must be suppressed within permissible levels. This paper reviewed the complete elimination of the leakage current using HBZVR-based inverter. Subsequently, the relationship among the existing topologies and the performance of CMV clamping branches are also investigated. Based on the analysis, a simple HBZVR-type transformerless PV inverter is proposed. To verify the accuracy of the proposed topology, the theoretical findings are validated via Matlab/Simulink. Finally, a universal prototype is built and tested for validation of both theoretical and simulation results.

Keywords: Photovoltaic (PV) inverter, HBZVR, leakage current, common mode voltage (CMV).

I. INTRODUCTION
The energy demand is increasing due to fact that the rapid increase of the human population and fast-growing industries [1] - [5]. Recently, photovoltaic (PV) energy has become very popular because of government incentives, declining price of PV arrays
and advancement of semiconductor technology [4]. PV inverters are usually categorized into with transformer and without transformer grid-tied systems. Traditionally, PV inverter is embedded with low frequency transformer on the AC side and high frequency transformer on DC side. Nonetheless, the transformer increases the cost, size and the difficulty in installation [8]-[9]. Therefore, transformerless PV inverters are introduced with reduced size, weight and higher efficiency [6]-[7]. In order to suppress the leakage current in transformerless PV inverter, the common mode voltage (CMV) must be kept constant [10]-[11]. According to German VDE 0126-1-1 standard, the grid must be disconnected within 0.3s if the root-mean-square value of the leakage current is more than 30 mA [16]. The root mean square value of the leakage current and their corresponding maximum allowable disconnection time are illustrated in Table 1. Many transformerless topologies have been proposed to solve the issues of leakage current and low conversion efficiency in [5]-[25]. A family of half bridge inverter is proposed in [18]. However, half Nonetheless, it leads to high switching losses and magnetic inductor losses, which results in lower conversion efficiency. On the other hand, the CMV clamping method is suitable for transformerless PV inverters due to improved CMV and low leakage current [17]-[19]. The required conditions for improved CMV is the potential of the freewheeling path should be clamped to half input voltage during the freewheeling periods, instead of disconnect the PV array from the utility grid. Based on this principle, different topologies were introduced in [17]-[25]. In [18], author Kerekes et al, introduce the new freewheeling path via passive elements (diode), which allows only one way of directional clamping, results relatively poor CMV in freewheeling periods. Suan [19] et al brings the additional diode to solve the issues of floating voltage and leakage current. Apparently, the performance of the CMV and leakage current are different among the discussed topologies due to clamping ability. In this paper HBZVR based clamping transformerless inverter is reviewed. A simple PV inverter is then proposed by adding one bidirectional switch, which ensures the half input DC-link voltage during freewheeling periods.

<table>
<thead>
<tr>
<th>Leakage current(mA)</th>
<th>Disconnection time(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>0.3</td>
</tr>
<tr>
<td>60</td>
<td>0.15</td>
</tr>
<tr>
<td>100</td>
<td>0.04</td>
</tr>
<tr>
<td>150</td>
<td>0.04</td>
</tr>
</tbody>
</table>

Table 1. Leakage current value and corresponding disconnection time illustrates in VDE 0126-1-1 standard [16].
This results in constant CMV and thus low leakage current. Finally, a universal prototype has been built to validate the performance of the proposed topology.

This paper is organized as follows: Existing single phase transformerless topologies are reviewed in section 2, proposed topology and its operating principles are discussed in section 3. Loss analysis is carried out in sections 4, Simulation and experimental tests are presented in section 5 and section 6 respectively. The final conclusion is reported in section 7 to summarize the observations and results.

II. REVIEW ON EXISTING TRANSFORMERLESS TOPOLOGIES

In this section, existing HBZVR type clamping inverters are reviewed in detail. The CMV of the PV systems, can be calculated as

\[ V_{cm} = \frac{V_{AN}+V_{BN}}{2} \]  

(a) HBZVR

It extends the principle of HERIC (Highly Efficient and Reliable Inverter Concept) topology with a passive clamping method known as HBZVR (H-bridge zero voltage state rectifier), as shown in Fig.1 (a). The operating principle is almost similar to the HERIC topology with an additional clamping function which is implemented through an active switch and four diodes. Due to limitations of the clamping branch, CMV is floating in one half of the grid period. As a result, leakage current is increased.

(b) HBZVR-D

As shown in Fig.1 (b), HBZVR-D (H-bridge zero voltage state rectifier diode) is recently introduced by modifying the HBZVR [18]. To improve the common-mode behaviour, one additional fast-recovery diode D6 is added to the freewheeling path, to fully clamp the CMV to constant, and the leakage current is eliminated. It is clearly seen that the clamping branch is important as it determines the common-mode behaviour of the PV system.
III. PROPOSED TOPOLOGY

According to the above analysis, a simple modified HBZVR topology is proposed by adding one bidirectional switch at midpoint of the DC-link known as HBZVR-S (H-bridge zero voltage state rectifier switch), as shown in Fig. 2. In addition, switches S1-S4 are employed in the full bridge inverter; the clamping circuit consists of four diodes D1-D4, switches S5 and S6. The filters are made up of L1 and L2 (L2=L1) at the grid lines. With the clamping effect, the CMV is clamped to half of the DC input voltage.
If compared with existing topologies presented in Fig.1, the difference among proposed topology is automatically observed in the freewheeling path ability.

Furthermore HBZVR-S topology simplifies the CMV clamping branch, from few diodes to one single switching device. It is reported in [28] that active clamping is more superior to passive clamping method in terms of loss distribution. The loss analysis will be carried out in a later section.

(a) Analysis and Modes of operation:

The operating principles of the proposed topology and its equivalent circuits are illustrated in four modes, which are depicted in Fig.3.

In Mode1: During the positive half cycle S1, S4 is turned on and remains off, inductor current increases and flows through S1,S4, equivalent circuit as shown Fig.3 (a). In this mode $V_{AN}=V_{DC}$, $V_{BN}=0$ and $V_{AB}=+V_{DC}$, therefore the common mode voltage can be derived as

$$V_{cm} = \frac{V_{AN}+V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} = 0.5V_{DC} \quad (2)$$

In Mode2: During the positive freewheeling period the S5 on and other turned off, inductor current decreases and freewheels via D2, D3 and the grid lines, equivalent circuit as shown in Fig.3 (b). In this mode $V_{AN}=V_{DC}/2$, $V_{BN}=V_{DC}/2$ and $V_{AB}=0$, therefore the common mode voltage can be derived as

<table>
<thead>
<tr>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>$V_{AN}$</th>
<th>$V_{BN}$</th>
<th>$V_{DM}$</th>
<th>$V_{CM}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$V_{DC}$</td>
<td>0</td>
<td>$+V_{DC}$</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$V_{DC}/2$</td>
<td>$V_{DC}/2$</td>
<td>0</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$V_{DC}$</td>
<td>-$V_{DC}$</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>$V_{DC}/2$</td>
<td>$V_{DC}/2$</td>
<td>0</td>
<td>$V_{DC}/2$</td>
</tr>
</tbody>
</table>
\[ V_{cm} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2} \left( \frac{V_{DC}}{2} + \frac{V_{DC}}{2} \right) = \frac{V_{DC}}{2} = 0.5V_{DC} \quad (3) \]

In Mode3: During the negative half cycle S2, S3 are turned on and remains are turned off, inductor current increases and flows via S2, S3 and grid lines, equivalent circuit as shown in Fig.3 (c). In this mode \( V_{AN} = 0 \), \( V_{BN} = V_{DC} \) and \( V_{AB} = -V_{DC} \), therefore the common mode voltage can be derived as

\[ V_{cm} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2} (0 + V_{DC}) = \frac{V_{DC}}{2} = 0.5V_{DC} \quad (4) \]

In Mode4: During the negative freewheeling period S5 on and the other turned off, inductor current decreases and freewheels via D1,D4, and the grid lines, equivalent circuit as shown in Fig.3 (d). In this mode \( V_{AN} = V_{DC}/2 \), \( V_{BN} = V_{DC}/2 \), therefore common mode Voltage can derive
It is clear that the CMV is constant at $V_{DC}/2$ and $V_{DM}$ varies between $+V_{DC}$, 0, $-V_{DC}$ isolated full bridge USPWM. Nonetheless, Table 2 shows the operation modes, switching states and the direction of the grid-in current, the differential-mode voltage. Hence, proposed topology is suitable for transformerless application.

**b. Operating principles of the proposed clamping branch**

**Fig.4.** Equivalent circuits of the proposed topology during the clamping mode (a) Potential down (b) Potential up.
The freewheeling branch is bidirectional. During freewheeling periods (mode 2 and mode 4 shown in Fig.3), if the freewheeling path voltage ($V_{FP}$) ($V_{FP}=V_{AN}-V_{BN}$) is lower than the DC-link voltage, the current freewheels through switch S6 and anti-parallel diode of the switch S5. As a result, the freewheeling path voltage is completely clamped the $V_{FP}$ to $V_{DC}/2$, as shown in Fig.4 (a). On the other hand, if freewheeling path voltage is higher than to DC-link voltage, the current freewheels via body diode of switch S6 and anti-parallel diode of the switch S5 to increase the freewheeling path voltage to $V_{DC}/2$, as shown in Fig.4 (b).

In HBZVR, the ability of freewheeling path is limited due to unidirectional clamping diode known as passive clamping via D5. The freewheeling path is only clamped to half of the input voltage. The clamping path is not functioning properly due to reverse biased D5 in one half of the cycle. This can be rectified by adding of bidirectional switch in the proposed HBZVR-S topology. With improved clamping branch via active switch S6, it guarantees that CMV holds to $V_{DC}/2$ during the whole freewheeling periods. Therefore, leakage current is completely reduced, which dependent on the constant CMV, as discussed earlier.

**IV. TOTAL LOSS CALCULATION AND COMPARISON IN SEVERAL TOPOLOGIES**

It is hard to measure the device losses for predicting the maximum efficiency in power electronics converters [31].

**Table 3** Analysis of device operation in discussing topologies.

<table>
<thead>
<tr>
<th>Topologies</th>
<th>Device type</th>
<th>HBZVR</th>
<th>HBZVR-D</th>
<th>HBZVR-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of devices</td>
<td>IGBT</td>
<td>5</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>Switching loss</td>
<td>IGBT</td>
<td>3</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Conduction loss</td>
<td>IGBT</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Freewheeling loss</td>
<td>IGBT</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Diode</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Reverse recovery</td>
<td>IGBT</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Gate loss</td>
<td>IGBT</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

However, it is noticeable that the loss calculation is based on the theory and its accuracy depends on the device data sheet accuracy. In this section device loss are calculated and compared via thermal module in PSIM [30]. The diode conduction losses are calculated in the following equations (6)-(7), which is dependent on the duty ration (D) on the device with periodically conduction.

\[
\text{Conduction losses} = V_d \times I_F
\]  

(6)
Conduction losses = \( V_d \times I_F \times D \)  \hspace{1cm} (7)

While \( V_d \) presents the diode voltage drop and \( I_F \) describes the forward current of the diode. Similarly turn-off losses are calculated in the following equations, when the diode is neglected.

\[
P_{sw-off} = E_{rr} \times f \times \frac{V_R}{V \_R\_datasheet} \hspace{1cm} (8)
\]

\[
P_{sw-off} = 0.25 \times Q_{rr} \times V_R \times f \hspace{1cm} (9)
\]

Where the reverse recovery losses are presented with the \( E_{rr} \), \( Q_{rr} \) recovery charge, switching frequency ‘off’, an actual reverse blocking voltage as \( V_R \) and \( V \_R\_datasheet \) presents reverses blocks voltage in the data sheet with characteristics of\( E_{rr} \). Under test conditions the \( Q_{rr} \) can be calculated in the following equation (10).

\[
Q_{rr} = 0.5 \times t_{rr} \times I_{rr} \hspace{1cm} (10)
\]

Under specific conditions, \( E_{rr} \) presents in the datasheet then losses are calculated using \( E_{rr} \), if not considered it can measured through \( Q_{rr} \).

| Table 4. Total power device losses |
|-----------------|-----------------|-----------------|
| Topology        | Losses (W)      | Total losses(W) |
| HBZVR           | S1   | S2   | S3   | S4   | S5   | S6   | D1   | D2   | D3   | D4   | D5   | D6   |       |       |
|                 | 1.732| 1.699| 1.735| 1.720| 3.166| 0    | 1.032| 1.026| 1.026| 1.032| 0.656| 0    | 14.824|
| HBZVR-D         | 1.725| 1.718| 1.720| 1.727| 3.176| 0    | 1.038| 1.032| 1.032| 1.039| 0.709| 0.710| 15.626|
| HBZVR-S         | 1.727| 1.719| 1.717| 1.718| 2.163| 0.664| 1.032| 1.023| 1.029| 1.035| 0    | 0    | 13.827|

And predominantly if the \( Q_{rr} \) is not mentioned then utilize \( t_{rr} \), \( I_{rr} \) and finally both are not specified and then assume the losses are null. Furthermore, in the discussed topologies are configured with active IGBT modules, therefore the losses are measured in the following equations (11)-(12), which conducts in both continuous and periodical modes conditions

\[
Conduction losses = V_{cc} \times I_c \hspace{1cm} (11)
\]

\[
Conduction losses = V_{cc} \times I_c \times D \hspace{1cm} (12)
\]

While \( V_{cc} \) illustrates the saturation voltage between the collector and emitter, \( I_c \) presents the collector current and ‘D’ for duty cycle. Consequently the switching losses of the IGBT during ON and OFF conditions are calculated in the following equation’s.

\[
IGBT \ Turn \ on \ losses = E_{on} \times f \times V_{cc} \times \frac{V_{cc}}{V\_cc\_datasheet} \hspace{1cm} (13)
\]
\[
\text{IGBT Turn off losse} = E_{\text{off}} \times f \times V_{\text{CC}} \times \frac{V_{\text{CC-datasheet}}}{V_{\text{CC-datasheet}}} \tag{14}
\]

Where \( E_{\text{on}} \) & \( E_{\text{off}} \) describe the energy losses during ON and OFF conditions with switching frequency, \( V_{\text{CC}} \) presents the DC-bus voltage and \( V_{\text{CC-datasheet}} \) describes the DC bus voltage of \( E_{\text{on}}, E_{\text{off}} \) using datasheet under test conditions. The IGBT FGA15N120 [30] with 1200V of rated voltage and current is loaded in the PSIM via thermal module device database editor. Table.3 shows the distribution of device number in HBZVR, HBZVR and HBZVR-S topologies as shown in Fig. (1)- (2) respectively. Fig.5 shows the total losses of each switching device for the discussed topologies. However, the loss distribution is mostly depends on the switching criteria together with good thermal design. And other calculation methods and theoretical analysis are studied and verified in the literature [23] -[27] which is not major contribution in this paper. Table.4 shows the loss analysis of the discussed topologies. On the other hand, it is shown that the proposed HBZVR-S topology has lower losses as compared to its HBZVR-D counterpart, due to the simplified CMV clamping branch, and also an active clamping method.

![Fig.5. Device losses](image)

V. SIMULATIONS

To verify the theoretical analysis and overall Performance of the HBZVR, HBZVR-D and Proposed topologies are conducted in MATLAB/Simulink. And simulations parameters are followed and listed in Table.5. The PV array is modeled with DC supply 400V, the two parasitic capacitance (\( C_{pv1}, C_{pv2} \)) 100nF and the symmetrical filter inductance can be considered as \((L1, L2)\) 3mH, the filter capacitance can be considered as \((C_F)\) 4µF, the switching frequency is 10 kHz with the grid voltage of 230V (rms) at a 50Hz frequency respectively [19].
Fig. 6 shows the simulation waveforms of $V_{AN}$, $V_{cm}$, $V_{BN}$, $V_{out}$, $I_{out}$, and $i_{leak}$ for HBZVR, HBZVR-D and proposed HBZVR-S topologies. It is clear that, large oscillation presents in HBZVR with magnitude of 0-200V due to poor utilization of clamping branch. As a result, leakage current will be increased significantly with HBZVR topology, as shown in Fig. 7. And HBZVR-D, proposed topologies present constant common mode voltage with magnitude of 200V, as a result zero leakage current is observed in both HBZVR-D, proposed topologies, which is most dependent on CMV. Hence, from simulation results, it can be concluded that the proposed topology with improved clamping branch using bidirectional switch could overcome the demerits regarding CMV and leakage current.
VI. EXPERIMENTAL RESULTS

In order to verify the simulation results and the effectiveness of the proposed topology a universal prototype has been built and tested in the laboratory using same specifications are listed in Table.5. The photograph of the test-bed experimental setup is depicted in Fig.6. For the convenience in the simulation results grid is replaced with resistive loads without affecting the performance [18]-[19]. All control algorithms are realized in FPGA Spartan-6. The experimental results of the output grid current, DM voltage $V_{AB}$ for the HBZVR, HBZVR-D topologies are depicted in sub Fig. 9. And the common mode voltage and leakage current for the HBZVR, HBZVR-D and proposed HBZVR-S topologies are illustrated in Fig.9, Fig.10. The output voltage of three topologies follows unipolar with three level output voltage $V_{PV}$, 0, -$V_{PV}$, where spikes arise during the dead time between the active and freewheeling periods with magnitude of 200V, as shown in Fig.9 and Fig.10. And the load current is fulfilling the requirement of IEEE 1547.std [29].Fig.9 and Fig.10 shows the experimental waveform of $V_{AN}$, $2V_{cm}$ (= $V_{AN}$+ $V_{BN}$), calculated in the digital oscilloscope (DSO) by using the math function), $V_{BN}$ and leakage current. In all three
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Fig. 8. Universal experimental test-bed

Fig. 9. Tested DM, CM characteristics of HBZVR, HBZVR-D topologies (a)-(c) $i_g$ (CH1), $V_{DM}$ (CH2). Enlarge of $V_{DM}$ (CH3), (b)-(d) $V_{AN}, V_{cm}, V_{BN}$ and $i_{leak}$ (Left-Right)
topologies extra spikes are present due to junction capacitance and turn-on delay time of the freewheeling diode. In addition, the common mode voltage fluctuation can be minimized by using the different power switches. However, the proposed HBZVR-S topology has excellent DM characteristics, which is good agreement with Fig.9. (a)- (b) and Fig.10.(a). It is observed that, during negative power region CMV oscillation present in HBZVR topology, as shown in Fig. 9 (a), which increases the leakage current. On the other hand, the magnitudes of the measured leakage current for HBZVR, HBZVR-D and Proposed HBZVR-S topologies are follows 45.82 mA, 21.12 mA and 21.18 mA (rms) respectively. According to listed in Table 1, the RMS values are still minor and acceptable for transformerless PV grid connected systems. Obvious the leakage current in HBZVR topology is double among other existing
topologies due to high frequency common mode voltage are not clamped properly as discussed earlier. Therefore, it confirms that proposed HBZVR-S topology has a lower leakage current compared to HBZVR topology, but closer to HBZVR-D topology. Fig.10 (c)-(d) shows the experimental waveforms of collector-emitter voltage stress across the switches S1, S3, S4 and gate drive signals of S5, S6. It is clear that no extra voltage present and there is no blocking voltage of the added switch is half the DC input voltage. As a result switching losses for the added devices are reduced significantly.

Fig.11 shows the efficiency comparison curve between HBZVR, HBZVR-D and proposed topologies with unity power factor. The HIOKI 3198 power analyzer has been used to measure the efficiency. It is well noted that the present efficiency diagram covers the total device losses and filter losses, which does not include the control circuit losses. The calculated Californian efficiency for HBZVR, HBZVR-D and HBZVR-S are 95.25, 96.27 and 96.28 respectively [18], shown in Fig.11. However the conversion efficiency is higher than to the HBZVR topology due to the fact that blocking voltages of the gate drive signals of switches S5, S6 are clamped.

<table>
<thead>
<tr>
<th>S.No</th>
<th>Parameter</th>
<th>HBZVR</th>
<th>HBZVR-D</th>
<th>HBZVR-S</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_{LL} pattern</td>
<td>Unipolar</td>
<td>Unipolar</td>
<td>Unipolar</td>
</tr>
<tr>
<td>2</td>
<td>CMV</td>
<td>Floating (~200V)</td>
<td>Constant</td>
<td>Constant</td>
</tr>
<tr>
<td>3</td>
<td>Leakage current (mA_{rms})</td>
<td>45.84</td>
<td>21.12</td>
<td>21.18</td>
</tr>
<tr>
<td>4</td>
<td>THD (%)</td>
<td>1.9</td>
<td>1.8</td>
<td>1.6</td>
</tr>
<tr>
<td>5</td>
<td>Californian Efficiency (%)</td>
<td>95.25</td>
<td>96.27</td>
<td>96.28</td>
</tr>
</tbody>
</table>

Fig.11. Efficiency analysis
half input voltage and its current through S6 is too small and little impact on the capacitor divider. The proposed topology with HBZVR-type active clamping inverter is a suitable candidate for high performance PV transformerless grid connected system. It is shown that proposed topology maximum efficiency is 96.28% under full load conditions, but higher than HBZVR, HBZVR-D. The Californian efficiency can be calculated by combining several weighted factors at different output power, depicted in (15).

\[ \eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \]  

Therefore, proposed topology with active clamping is not only eliminating the leakage current, but also achieves higher conversion efficiency. Table 6 summarized the performance comparisons of the all discussed topologies.

VII. CONCLUSIONS

This paper presents an improved HBZVR type inverter with active clamping method. In addition, proposed topology has following advantages:

(1) Common mode voltage is constant during the whole the grid period, thus leakage current is reduced significantly.

(2) The blocking voltages of the added switch are half of the input DC voltages, as a result switching losses are reduced considerably during the whole grid period.

Above merits are validated and compared by universal prototype rated at 1kW, 230V/50Hz. Hence, it is concluded that the proposed HBZVR based clamping inverter (known as HBZVR-S) is a suitable for high performance single-phase transformerless PV grid connected applications.

REFERENCES


