A Novel Design Based Approach of High Performance CMOS Based Comparator Using PSpice

Ayushi Chaurasia  
M.Tech. (E.C.), Scholar  
Amity School of Engineering and Technology  
Amity University, Lucknow, U.P., India.

Rajinder Tiwari  
Department of Electrical and Electronics  
Amity School of Engineering and Technology  
Amity University, Lucknow, U.P., India.

Abstract

A new continuous-time CMOS current comparator having high speed and low power is proposed as an important component of current mode signal processing unit. It comprises of CMOS complementary amplifier with a feedback MOS resistor, two resistive load amplifiers and two CMOS inverters. Short response delay, low power consumption and small area are some of its features. Due to the absence of bias current and voltages, the circuit is robust to process deviations. The superiority on speed/power ratio over other existing high performance CMOS current comparator can be verified by PSPICE simulation result with 1.2µm CMOS process.

Keywords: CMOS, Speed/Power Ratio, Current Comparator, High power, Low power

1. INTRODUCTION

Current-mode circuits have become increasingly very popular among analog circuits designs in recent years. This is basically attributed to larger bandwidth, higher speed and lower supply voltage requirement as compared to the voltage mode circuit counterpart. Current mode circuit is considered as an alternative to voltage mode circuit because of the shrinking of VLSI feature size and the increasing demand for high speed and low power applications[1-3]. The current comparator is widely used in
A/D converter, oscillator, VLSI neural network etc. as a fundamental component of current mode signal processing circuit.

![Fig. 1 Original CMOS current comparator](image1)

Fig. 1 Original CMOS current comparator [1]

Fig. 1 shows the earliest continuous time CMOS current comparator based on high output-resistance cascoded current mirror. The voltage amplifier amplifies the difference between $I_1$ and $I_2$ and $V_{out}$ is the voltage mode comparison result signal. Some CMOS stages are added to increase the amplitude of the output voltage to achieve rail-to-rail output. The biggest problem of the current comparator arises because the current mirrors have high output resistances, the added capacitive CMOS stages reduces the frequency response of the comparator, so it is not suitable for high speed applications.

Recently, some high speed continuous time CMOS current comparator has been proposed. A conventional current comparator is represented in Fig. 2(a), where $I_a$ is the difference between two input currents, $V_{out}$ indicates the comparison result and for the simplicity CMOS stages have been omitted [4-5]. It uses a source follower as the input stage and a CMOS inverter as the positive feedback and it enables lower input resistance and shorter response time.

![Fig. 2(a) Conventional CMOS current comparator](image2)

For the dynamic response of small input current exists a dead band region which has the two input transistors and both are turned off temporarily and at this time the input
resistance is high. The dynamic response time of the current comparator will increase with the decrease of the input current[4-5]. To solve this problem a current comparator is proposed in fig. 2(b).

![Proposed Current Comparator](image)

This comparator adds two transistors and four bias current which changes the biasing scheme of input stage from class B to class AB operation, this reduces the dead band region and decreases the response time when input current is small. This circuit is complicated as many transistors are needed to implement the four current sources as biasing circuit, so the power consumption increases. The process deviations create great effect on the comparator as the performance is closely related to the values of the four current sources. The bulks of the two biasing contemplementary transition are connected to their sources, not ground and power respectively, so complicated twin-tub CMOS process needed for this circuit[6-7].

The proposed current comparator is comprised of three current sources inverting amplifier and a CMOS inverter. In the first current-source inverting amplifier a resistive feedback network is added to decrease the input impedance. The circuit exhibits low response time and good process immunity, but its resolution is limited by the bias current. To achieve high resolutions applications, large bias current is needed and power consumption is increased. Because of the use of current-source amplifiers, its power consumption will not decrease when input current increases and it exhibits great contrasts with those of the proposed new comparator. A new continuous time CMOS current comparator is proposed in this paper. Some of its features are short response delay time, low power consumption, small area and process robustness. Simulation results indicate that its speed/power ratio is better than those of the above current comparator.

2. CIRCUIT DESIGN:

In Fig. 3 we can see the proposed new robust high-speed and low-power continuous-time current comparator. It consists of two resistive-load amplifier (M6-M9), one CMOS complementary amplifier (M1-M2) and two CMOS inverters (M10-M13). M3
and M4 decrease the working current because M1 and M2 both work in the saturation region. The transistor M5 acts as the negative feedback resistor of the CMOS complementary amplifier because it works in the linear region.

![Figure 3: New CMOS current comparator](image)

According to the small signal analysis, when we neglect M3 an M4 then the input and the output resistances of the CMOS complementary amplifier with a feedback resistor can be expressed as

\[
R_{in} = \frac{R_5 + R_p}{1 + (g_{m1} + g_{m2}) R_p} \tag{1}
\]

\[
R_{out} = \frac{R_5 + R_c}{1 + (g_{m1} + g_{m2}) R_c + (R_5 + R_c) R_p / R_p} \tag{2}
\]

Where \( R_p = (r_{ds1} / r_{ds2}) \), \( g_{m1} \) and \( g_{m2} \) are the transconductances of M1 and M2 respectively, \( R_5 \) is the on-resistance of M5, \( R_c \) is the output resistance of the input current source. Because generally \( R_5 << R_E \) and \( (g_{m1} + g_{m2}) R_p >> 1 \) exist, it can be concluded as follows

\[
R_{in} \sim R_{out} \sim \frac{1}{g_{m1} + g_{m2}} \tag{3}
\]

The small input and output resistances reduce the voltage swings at node 1 and node 2 which results in the decrease of response time of the comparator. Two resistive load amplifiers are used to provide additional gains to amplify the voltage swing at node 2. The last two CMOS inverters outputs a rail-to-rail compared result signal, while the introduced delay time is negligible in practice[8-9]. The new current comparator has no external bias currents and bias voltages, so the process deviation immunity is enhanced.

3. SIMULATION RESULTS:

For comparing the performances of the new current comparator with the performance of others in PSPICE simulations are performed for the four comparators using standard 1.2µm CMOS technology parameters with 3V power supply. Table 1. Represents the transistor dimensions of the proposed circuits.
Table 1. Transistor Dimension of new circuit [1]

<table>
<thead>
<tr>
<th>Device</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>M7</th>
</tr>
</thead>
<tbody>
<tr>
<td>W(µm)</td>
<td>7.5</td>
<td>2.4</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>L(µm)</td>
<td>1.2</td>
<td>1.2</td>
<td>2</td>
<td>8</td>
<td>8</td>
<td>4</td>
<td>2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>M8</th>
<th>M9</th>
<th>M10</th>
<th>M11</th>
<th>M12</th>
<th>M13</th>
</tr>
</thead>
<tbody>
<tr>
<td>W(µm)</td>
<td>4</td>
<td>4</td>
<td>11.5</td>
<td>4</td>
<td>8.4</td>
<td>3</td>
</tr>
<tr>
<td>L(µm)</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1.6</td>
<td>1.6</td>
</tr>
</tbody>
</table>

The transient responses of these four comparators are stimulated for input-square are currents with amplitudes ranging from ±0.01 µA to ±10 µA. Transient waveform of the output voltages for the proposed comparator and when the input-square wave current changes between 0.1µA and -0.1µA is represented in fig 4. We can see that the delay time of the proposed comparator is about 8ns.

![fig 4](image)

Fig. 4 Transient output voltages against input square-wave current[1]

Fig. 5 represents the average delay time of the four comparator as a function of the amplitude of the input-square wave current.

![fig 5](image)

Fig. 5 Average delay times against input current [1]
With the increase of input, the four delay time decreases with the order of the magnitude. The four delay times are almost the same when the input current is 10µA because under this condition propagation delay of the inverting amplifier stages determines the delay time, rather than the time to apply enough negative feedback. The power consumptions of the four comparators as a function of the amplitude of the input-square wave current are represented by fig. 6.

![Fig. 6 Power consumptions against input current](image)

The power consumption is achieved with the expense of the large response delay for small input currents when its voltage swing is larger. When the input current of the proposed comparator is 0.01µA their power consumption are almost the same. By increasing the input current, the power consumptions of the proposed comparator and that of [5] decreases, while that of [6] remains the same, because it uses current source amplifiers, its bias current also does not change with the change in input current. When input current is 1µA, the power consumption of the proposed comparator and those of [5] and [6] are 0.3mW, 0.37mW respectively, their delay time are almost the same, so the speed/power ratio of the proposed comparator is about 127% and 177% over those of [5] and [6] respectively. Their characteristic is suitable for high speed and low power applications.

4. **CONCLUSION:**

A Robust high speed and low power continuous time CMOS current comparator has been designed, whose delay time can be compared to the existing fast current comparator. Its speed/power ratio is better than the other comparator due to its low power consumption. The simple structure and process robustness makes this circuit suitable to real applications[10-13].

We can conclude that with the increase in input current the power consumptions of the proposed comparator and that of [5] decreases while that of [6] remains same.
A Novel Design Based Approach of High Performance CMOS Based Comparator

5. ACKNOWLEDGEMENT:

The authors are thankful to Mr. Aseem Chauhan (Additional President, RBEF and Chancellor AUR, Jaipur), Maj. General K. K. Ohri (AVSM, Retd.) Pro-VC, Amity University, Uttar Pradesh Lucknow, Wg. Cdr Anil Kumar (Director ASET, Lucknow Campus), Brig. U. K. Chopra (Director AIIT & Dy. Director ASET), Prof O. P. Singh (HOD, Electrical & Electronics), Prof. H. K. Dwedi (Dy. Director, Research in Electronics) and Prof. N. Ram (Dy. Director ASET) for their motivation, kind cooperation, and suggestions.

REFERENCES

[1] Lu Chen**, B ingxue Shi and Chun Lu, A Robust High-speed and Low-power CMOS Current Comparator Circuit'
[2] Surachet Khucharoenis and Varakorn Kasemsuwan, a 3v robust high-speed low input impedance CMOS current comparator, IEEE, 2004