Abstract—In this paper interleaved high stepup converter is simulated with different types of filters and controllers. The simulation of converter with different controllers were performed and voltage regulation is measured. Also, the performance of converter is analyzed with different filters and output is tabulated. From the analysis, the Fuzzy Logic Controller performs better in terms of voltage regulation with cascaded filter.

KEYWORDS : High step-up DC-DC converters, boost converters, charge pump circuits, c filter, [-]-Filter, cascade filter, controllers.

I. INTRODUCTION

High step-up DC-DC converters are the subject of intensive research efforts by the power electronics community due to their widespread applications in distributed generation systems. A quite vast overview of the different techniques can be found in [1] – [5]. Most of the topologies presented in literature are based on the basic Boost cell, like in [6] and [7], meaning that the switch voltage stress, even if lower than the output voltage, always remains higher than the input voltage, and dependent on the switch duty cycle. On the other hand, switched-capacitor (SC) topologies may allow reducing the switch voltage stress to the minimum value corresponding to the input voltage, like in the topologies proposed in [8]. The conversion efficiency of SC converters depends on the relative value of capacitor charging/discharging time constant compared with the switching period T_s. The best efficiency is obtained when \( T_c \geq T_s \), so the charging/discharging currents are almost constant in any phase. However, this favorable situation is not likely to occur in discrete SC converter implementations, where low RDSon of the switches, together with the relative low switching frequency compared with integrated solutions, will require impractical capacitance values to satisfy the above inequality. In these situations, good efficiencies can still be obtained even in discrete implementations for high power levels, by shaping the charge/discharge currents through inductors (both parasitic elements and/or intentionally added), like in [8], and despite their attractiveness in terms of modularity and possible integration due to the lack of magnetic elements, a very high voltage gain requires a large number of active devices, with relative driving circuitry.

The circuit diagram of basic voltage doublers switched capacitor cell is shown in figure 1. It consists of diodes D0 and D1 and capacitors C0 and C1 along with V0 and V1 and consists of switches S1 and S2 in which S1 and S2 are opened.

The circuit diagram of modified topology for higher voltage gains is shown in figure 2. It consists of buck cell (Lb-Cb) is added to generate duty cycle control voltage \( V_{b}=D_{v}v \) the coupled inductor turns ratio into capacitor C1 and C2 during the S2 the conduction interval leakage inductance \( L_d \) helps to shape both charging and discharging currents.
II. PRINCIPLE OF OPERATION

The circuit diagram of operation of coupled voltage is shown in figure 3, which has switch S1 is turned ON and resonant tank is formed involving C1, C2, Cb and Ld. S2 is closed. COUPLED VOLTAGE = C1 + Ld

In the circuit diagram of time response for main switch ON shown in figure 4. It consists of switch S1 is closed and in the remaining part of main switch on time, neglecting the magnetizing current ripple, the capacitor Cb continues to be charged and time response is less than t and has less duty cycle.

The circuit diagram of polarity voltage is shown in figure 5. In this interval S2, D1 and D2 are conducting, thus recharging C1 and C2 in a resonant manner hence S2 is closed and has an t1 = S1 + Lb.

III. SIMULATION

A. Open loop circuit diagram of nonisolated high step up converter with C-Filter

The simulation diagram of Open loop non isolated high step up converter with C-Filter is shown in figure 7. It consists of two switches and perform DC to DC conversion. The waveform of input voltage, output voltage are shown in figure 8 and 9. The input voltage of this circuit is 15 V.

Fig.3. Operation of coupled voltage

Fig.4. Time response for main switch ON

Fig.5. Polarity voltage

Fig.6. Free-wheeling phase of the buck sub-section

Fig.7. Open loop circuit diagram of nonisolated high step up converter with C-Filter

Fig.8. Input voltage waveform

Fig.9. Output voltage waveform across RL load
The waveforms of output voltage and output voltage ripple are shown in figure in 9 and 10. The output voltage is 65V

Fig. 10. Output voltage ripple waveform across RL load

The waveform of output voltage ripple across RL loads shown in figure 10 which has 5V

Fig. 11. Output current waveform through load

The waveform of output current and output current ripple are shown in figure 11 and 12. The output current is around 0.06A and output power has an value of 44watts,

Fig. 12. Output current ripple waveform through RL load

B. Open loop circuit diagram of nonisolated Interleaved high step up converter with \( \Pi \)-Filter

The simulation diagram of Open loop circuit diagram of non-isolated interleaved high step up converter with \( \Pi \)-Filter is show in figure 13. It consists of four switches and it performs dc-dc conversion. The waveform of input voltage output voltages is shown in figure 14 and 17. The input voltage of the circuit is 15V and the output voltage of the circuit is 85V.

Fig. 13. Open loop circuit diagram of nonisolated interleaved high step up converter with \( \Pi \)-Filter

Fig. 14. Input voltage for \( \Pi \)-Filter

In compare to C-filter and \( \Pi \)-Filter the circuit is interleaved in \( \Pi \)-Filter and the output current, output voltage and output power is improved.

C. Circuit diagram of nonisolated interleaved high step up converter with Cascade-Filter

The waveform of output voltage and output voltage ripple waveform across RL load are shown in figure 15 and 16. The output voltage is 85V and the output ripple voltage is 1.2V.

Fig. 15. Output voltage waveform across RL load

Fig. 16. Output voltage ripple waveform across RL load

The waveform of output current and output ripple are shown in figure 17 and 18. The output current is around 0.01A. The waveform of output power is 74w.

Fig. 17. Output current waveform through load

Fig. 18. Output current ripple waveform through RL load
The simulation diagram of non-isolated interleaved high step up converter with cascade filter is shown in figure 19. It consists of 4 switches and performs DC-DC conversion and they have an extra one capacitor compared to [-]-Filter. The wave form of input voltage is shown in figure 20. The input voltage of this circuit is 15V.

![Fig.20. Input voltage for cascade filter](image)

The wave forms of output voltage and output ripple voltage are shown in figure 21 and 22. The output voltage is 85V and output voltage ripple is 0.6V.

![Fig.21. Output voltage across RL load](image)

The waveform of Output current And Output ripple is shown in figure 23 and 24. The output current is around 0.006A.

![Fig.22. Output voltage ripple across RL load](image)

![Fig.23. Output current through load](image)

The waveform of output current ripple through load is shown in figure 24. It has 0.006A. The output power is 74w.

The table 1 and 2 shows the comparison of converter with various filter for output voltage and current. From this comparison, converter with cascade filter performs better.

### Table 1 Comparison of high step up converter and interleaved converter

<table>
<thead>
<tr>
<th>Converters</th>
<th>Vin</th>
<th>Vo</th>
<th>Vor</th>
<th>Ior</th>
<th>Po</th>
</tr>
</thead>
<tbody>
<tr>
<td>High step up converter</td>
<td>15V</td>
<td>65V</td>
<td>5V</td>
<td>0.06A</td>
<td>44W</td>
</tr>
<tr>
<td>Interleaved high step up converter</td>
<td>15V</td>
<td>85V</td>
<td>1.2V</td>
<td>0.01A</td>
<td>74W</td>
</tr>
</tbody>
</table>

### Table 2 Comparison of output voltage ripple and output current ripple

<table>
<thead>
<tr>
<th>converters</th>
<th>Vor</th>
<th>Ior</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-filter</td>
<td>5.0V</td>
<td>0.06A</td>
</tr>
<tr>
<td>[-]-filter</td>
<td>1.2V</td>
<td>0.01A</td>
</tr>
<tr>
<td>Cascade filter</td>
<td>0.6v</td>
<td>0.006A</td>
</tr>
</tbody>
</table>

D. Circuit diagram of non isolated interleaved high step up converter with PI controller

The simulation diagram of non-isolated interleaved high step up converter with PI controller is shown in figure 25. It consists of four switches, specify capacitors, inductance, constant gain and one proportional integral control (PI) controller. It performs dc-dc conversion. It is a closed loop simulation diagram. The input voltage wave form is shown in figure 26. The input voltage of this circuit is 15V.

![Fig.25. Circuit diagram of non isolated interleaved high step up converter with PI controller](image)

The wave forms for output voltage and output current is shown in figure 27 and 28. The output voltage is 85V.
In the output voltage of PI controller, it has an rise time of 0.48ms, settling time is 1.2ms, peak time is 0.70 and Error occurs in 1.6 ms.

In the output voltage of PID controller, it has an rise time of 0.44ms, peak time is 0.56ms, settling time is 0.80ms and Error occurs in 0.8ms.

The wave forms of output voltage and output current are shown in figure 31 and 32. the output voltage is around 85V.

The simulation diagram of non-isolated interleaved high step up converter with FL controller is shown in figure 33. It consists of switches, specify capacitors, inductance, constant gain, power gui, pulses and one Fuzzy logic controller (FLC). It performs dc-dc conversion. It is an closed loop simulation diagram. The input voltage wave form is shown in figure 34. The input voltage of this circuit is 15V.
The wave forms of output voltage and output current is shown in figure 34 and 35.

![Fig.35. Output voltage for FL controller](image)

Fig.35. Output voltage for FL controller

In the output voltage of FL controller, it has a rise time of 0.12ms, peak time is 0.30ms, settling time is 0.50ms and Error occurs in 0.2ms.

![Fig.36. Output current for FL controller](image)

Fig.36. Output current for FL controller

<table>
<thead>
<tr>
<th>Controller</th>
<th>Rise time $Tr$</th>
<th>Settling time $Ts$</th>
<th>Peak time $Tp$</th>
<th>Error $Ess$</th>
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<tbody>
<tr>
<td>PI</td>
<td>0.48</td>
<td>1.2</td>
<td>0.70</td>
<td>1.6</td>
</tr>
<tr>
<td>PID</td>
<td>0.44</td>
<td>0.80</td>
<td>0.56</td>
<td>0.8</td>
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<tr>
<td>FLC</td>
<td>0.12</td>
<td>0.50</td>
<td>0.30</td>
<td>0.2</td>
</tr>
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</table>

The table 3 shows the comparison of time domain parameters with various controller for rise time, settling time, peak time and steady state error. From this comparison controller with fuzzy logic controller performs better.

IV. CONCLUSIONS

Ripple is reduced with $\Pi$ Filter. Settling time is reduced from 1.2 to 0.50sec by using FL controller. Rise time is reduced from 0.48 to 0.12sec by using FL controller. Peak time is reduced from 0.7 to 0.30sec by using FL controller. Steady state error is reduced from 1.6v to 0.2v by using FL controller.

REFERENCES