FPGA based Power Analysis and Control of Distributed Generation Interface

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Abstract. Renewable energy is becoming economic in all markets as its rapid growth results in more competitive prices. A problem arises is how to assimilate these energy sources into a conventional power grid as to boost the performance and reliability of the new Distributed Generation (DG) system. This work provides the experimental evaluations of a power control by Field Programmable Gate Array (FPGA) circuit for single-phase grid-connected Voltage Source Inverter (VSI) for residential and commercial applications. New hardware architecture of Adaptive Linear Neural Networks (ADALINE) are accept the pursuit of algorithms of power control and also allowed the real time analysis of the high order harmonics without expanding the utilization area of the FPGA circuit. These features will provides active power rapidity and also for harmonics and reactive power compensation. The simulation and experimental results shows that the fixed and variable frequency schemes are evaluated using MATLAB/Simulink-Xilinx.

Keywords: Distributed Generation, Field-Programmable Gate Array, Adaptive Linear Neural Networks.

1 Introduction

Today, the immense utilization of Distributed Energy Resources (DER) based on non-conventional resources has become very important to alleviate problems related with green house gas discharge and to enhance their reliability and capability of actual and future power systems. An advancements on non-conventional energy systems and smart grid technologies are necessary to acquiesce the integration of DER with the traditional centralized power systems. These technological advances will produce a high diffusion of Distributed Generation (DG). This new approach power electronics integrate for grid-connected operation must consider not only power dispatch, but also interdependent functions like the compensation of reactive power and harmonics and the embedded real-time monitoring of the power quality, the frequency, the voltage, and the active and reactive powers. Also the detailed harmonics information will not be a choice but an important feature to be considered in the DG interfaces.

Generally, the evaluation of electrical signals which contains harmonics using the techniques such as Fast Fourier transformations (FFT) [1], Recursive Least Square (RLS) [2] and the Kalman filter (KF) [3]. But, the Artificial Neural Networks (ANNs) like the Adaptive Linear Neural Networks (ADALINE) [4] and the Radial Basis Function Neural Network (RBFNN) [5] are also used for evaluation of harmonic content of electrical signals. The Field-Programmable Gate Array (FPGA) has become an interesting abject for embedded applications, since its parallel structure reduces execution times [6]–[8]. This advantage is more evident in the implementations in hardware are considered. By observing all characteristics of DER in power systems, this paper presents the experimental validation of a FPGA-based power analysis and control of a DG interface. The measurement and control algorithms use pure hardware architectures of ADALINE, as proposed in [9]–[10]. The proposed algorithms have been implemented in an FPGA circuit using Xilinx-System Generator evaluated by using grid-connected IGBT VSI.

This paper is organized as follows. Some considerations of hardware and software implementations for real-time harmonics estimation are presented in Section 2. Section 3 provides the ADALINE schemes for harmonic estimation using FPGA. The VSI synchronization and control in Sections 4. In section 5, the simulation results of the power analysis of fixed and variable frequency schemes are presented. The paper ends with few concluding remarks in Section 6.
2 Implementations for Real-Time Harmonics Estimation

This section provides few deliberations of hardware and software implementations for real time harmonics estimation. Execution time of a software implementations, estimation of higher order harmonics, sampling rate and estimation of accuracy can be reduced by this method. ANNs based ADALINE algorithm is implemented for assessment of signals and detection of harmonics. It is used for signals tracking detection [11], harmonics estimation of electrical signals [12]–[13], control applications [14] and active filters [15]. For implementation of harmonic detection by ANNs, the new technique like RBFNN [10] is used. It provides more accurate results compare to the ADALINE and FFT methods. The implementation cost is more due to the increase in the use of multipliers as well as the harmonic order of the estimation become higher. For harmonics estimation can execute the structures that offer very short execution times but it requires a great use of arithmetic blocks, which are finite resources in FPGA systems.

If the algorithm speed is the main objective, the hardware FPGA implementations of ANNs and digital filters are more efficient than software implementations. An important consideration in power systems applications is that the voltage and current signals, including their corresponding harmonics, have much lower frequencies than the one of the FPGA clock. In that case, direct or pipelined implementations for voltage and current estimation in power systems results in redundant increase of the FPGA area utilization. This area increase is more important when high order harmonics estimation is required. Hence, a compromise between execution time and implementation area must be realized in order to obtain the most efficient relation of cost-speed.

3 ADALINE Implementation in FPGA

A periodic signal \( y(t) \) with angular frequency \( \omega \) may be calculated in

\[
y(t) = A_0 \sum_{n=1}^{\infty} \left[ A_n \cos(n\omega t) + B_n \sin(n\omega t) \right]
\]

by using its Fourier series representation, and it may be represented according to the ADALINE linear combiner equation [7], [8]

\[
\hat{y}(k) = W_0(k) + W(k)^T.X(k) \quad (2)
\]

where \( \hat{y}(k) \) represents the estimated signal which is calculated with the input pattern vector containing the harmonic components sine and cosine, the weight vector which represents the Fourier coefficients, and which is the estimated average of the measured signal. In this application, the Widrow–Hoff learning rule is employed to

\[
W(k + 1) = W(k) + \alpha \frac{X(k)}{N} \cdot e(k).X(k) \quad (3)
\]

update the weight vector [4], where \( \alpha \) is a learning factor typically chosen between 0 and 2, and \( e(k) \) is the estimation error calculated at the \( k \) instant using the measured and sampled signal \( y(k) \) and its estimated value (2). The ADALINE implementation is composed of a common block for the X vector generation function, and a modular block for each channel for sample and normalization, the W vector updating and the signal estimation functions. To calculate the estimated signal and the estimation error within the sampling period (\( T_s \)) a common block has been created to allow the synchronized sampling of the input ports, the generation of the X vector and the W vector updating functions.

3.1 Input Pattern Vector and Weight Vector Updating (WVU)

The Direct Digital Synthesis (DDS) technique [16] is available for generating the periodic signals using a discrete time phase generator and a phase-to-waveform converter. The novelty of the implementation structures of DDS (FF-DDS and VF-DDS) consist of generating the 2N signals of the X vector using only one pre calculated sine table, which is read sequentially by means of a time division multiplexing scheme to obtain the N considered harmonics within a base period (To). The implementation diagram of the proposed VF-DDS for N harmonics generation is presented in Fig. 1(a).
The VF-DDS cause the harmonic reference signals of sine and cosine for the number of harmonics defined by $N$, using just one ROM memory with depth equal to $2^P$. All harmonic signals ($2N$) are generated and sent sequentially using a time-division multiplexing structure. The multiplexing process is coordinated by two free-running counters BC1 and BC2. BC1 is a 3-bit counter which generates the period necessary to produce the address and to access the ROM memory to obtain the information of each harmonic. BC2 is a CH-bits counter which is employed to generate the address information corresponding to each harmonic signal (sine and cosine). Since CH is defined as $\text{ceil}(\log_2(2N))$, then the output of BC2 varies from 0 to $2N-1$. A SLICE LSB block is used to extract the LSB bit of its input which is related to the phase for the sine or cosine signal (0 for sine and $\frac{2\pi}{4}$ for cosine), and an SR1 (shift right one bit) block is used to obtain the harmonic order.

Generally, the signal sampling period ($T_s$) and the DDS base period ($T_0$) are different depending on the characteristics of the analog-to-digital converter (ADC) employed in the measurement system, then the weight vector can be updated by means of two different WVU schemes as proposed in [9], using $T_s$ or $T_0$ as the updating period. It has been demonstrated in [9] and [10] that the more efficient structure for FPGA implementation concerning the used area is the WVU-$T_0$, which employs the DDS base period as updating period. In this case, the updating function including the learning rule and the signal estimation are implemented according to Fig. 1(b).

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**Fig. 1.** The implementation diagram for harmonics generation of the VF-DDS in Fig. 1(a) and Fig. 1(b)

**Fig. 2.** Simplified circuit of grid-connected VSI
4 Implementation of VSI Control

A simplified circuit of a grid-connected VSI system, as used for validation, is presented in Fig. 2, where $L_s$ is the grid inductance, $L_d$ and $C_d$ respectively the inductor and capacitor of the LC output filter of the VSI, and PCC is the point of common coupling. The Fourier decomposition of the load voltage ($V_{\text{PCC}}$) and the output current of the VSI ($i_{\text{VSI}}$) can be obtained by using the ADALINE implementation presented in the Section 3. These time-domain representations of voltage and current can be expressed according to

$$v_{\text{PCC}}(t) = V_{\text{PCC}} + \sqrt{2} \sum_{n=1}^{\infty} [V_{\text{PCC}} A_n \cos(n\omega t) + V_{\text{PCC}} B_n \sin(n\omega t)] \quad V \quad (4)$$

$$i_{\text{VSI}}(t) = I_{\text{VSI}} + \sqrt{2} \sum_{n=1}^{\infty} [I_{\text{VSI}} A_n \cos(n\omega t) + I_{\text{VSI}} B_n \sin(n\omega t)] \quad A \quad (5)$$

The estimated fundamental voltage at the K instant can be obtained from the ADALINE using

$$v_{\text{PCC}}(k) = X(0, k) \cdot W(0, k) + X(1, k) \cdot W(1, k) \quad V \quad (6)$$

and its amplitude can be computed using

$$|v_{\text{PCC}}(k)| = \sqrt{W(0, k)^2 + W(1, k)^2} \quad V \quad (7)$$

Taking into account the estimated fundamental of $V_{\text{PCC}}$ as the reference signal for the power control system, the orthogonal reference signals for synchronization of the VSI are obtained using

$$\text{REF} \sin(k) = \frac{X(1, k) \cdot W(1, k) + X(0, k) \cdot W(0, k)}{\sqrt{(W(0, k)^2 + W(1, k)^2)}} \quad (8)$$

$$\text{REF} \cos(k) = \frac{X(1, k) \cdot W(1, k) + X(0, k) \cdot W(0, k)}{\sqrt{(W(0, k)^2 + W(1, k)^2)}} \quad (9)$$

This approximation is only possible if the harmonics and the dc components of voltage at the point of common coupling are negligible. The DG interfaces, as recommended by IEEE standards [17], must be operated with low total harmonic distortion (THD). Under this constraint, the fundamental instantaneous power can be written using

$$p(k) = V_{\text{PCC}}(k) \cdot I_{\text{VSI}} B_1 \sqrt{2} \cdot \text{REF} \sin(k) + V_{\text{PCC}}(k) \cdot I_{\text{VSI}} A_1 \sqrt{2} \cdot \text{REF} \cos(k) \quad VA \quad (10)$$

and the fundamental active and reactive powers ($p_1$ and $q_1$) can be computed using

$$p_1 = \frac{1}{\sqrt{2}} |v_{\text{PCC}}(k)| \cdot I_{\text{VSI}} B_1 \quad W \quad (11)$$

$$-q_1 = \frac{1}{\sqrt{2}} |v_{\text{PCC}}(k)| \cdot I_{\text{VSI}} A_1 \quad \text{VAR}$$

The fundamental output current of VSI ($i_{\text{VSI, ref}}$) can be written as a function of $V_{\text{PCC}}$ and the active and reactive power set points $p_{\text{ref}}$ and $q_{\text{ref}}$ using

$$i_{\text{VSI, ref}}(k) = \frac{2p_{\text{ref}}}{|v_{\text{PCC}}(k)|} \cdot \text{REF} \sin(k) + \left(\frac{2q_{\text{ref}}}{|v_{\text{PCC}}(k)|} + \omega c_0 |v_{\text{PCC}}(k)|\right) \cdot \text{REF} \cos(k) \quad A \quad (12)$$

To generate the reference current for the VSI current control (12) is used. A hysteresis current control (HCC) modulators employed to produce the gating pulses for the power electronics converter. The two different schemes of the ADALINE synchronization have been implemented and evaluated in this paper: ADALINE with FF-DDS and VF-DDS using a feedback loop with the mean frequency of the generated in-phase reference signal ($\text{REF} \sin(k)$).

5 Experimental Results

5.1 Voltage Estimation and Reference Signals Generation

The voltage estimation and the reference signals generation have been evaluated experimentally using a controllable ac source to generate a 120-V voltage signal with variable frequency. The frequency of the test signal is varied within the IEEE recommended limits [17]. The variations have been introduced in steps of 0.1Hz. The two proposed synchronization methods have been implemented in parallel in FPGA.
The trajectories of the measured voltage, the generated in-phase reference signal, and the frequency of the generated synchronization signal have been plotted by using the MATLAB/Simulink-Xilinx user interface to compare the performance of each method.

Experimental results show that FF-ADALINE offers the best steady-state estimation error for frequencies below and above its reference frequencies (i.e. 50Hz). VF-ADALINE offers good steady-state estimation error. The convergence time of frequency tracking is longer than the one obtained with FF-ADALINE. The frequency tracking error remains under ±0.01Hz in both schemes, so any of them can be used for synchronization with good transient response and accurate estimation, even for sudden frequency variations.

The experimental results also show that FF or VF schemes can be used for synchronization with the following limitations: estimation error with FF-ADALINE increases over 3% when the frequency deviation is superior to ±2Hz; the learning factor of VF-ADALINE must be set below to 0.3 in order to keep stable orthogonal signals generation. A learning factor higher than 0.3 improves the convergence time, but it may also introduce undesirable overshoot in the frequency estimation and distortion in the synchronization signals when important transients in measured signal are observed. The THD of the measured signals could produce more important effects on the performance of estimation when using the FF-ADALINE scheme, it has been then evaluated under different voltage THD (from 1.5% to 5%) without important effects on the frequency tracking and the voltage estimation as reported in Table 1. From Table 1, the estimation error remains under 2% and the convergence time of generated signals under 120 ms.

The convergence time of the signal estimation, the frequency tracking, and the synchronization signals generation using FF-ADALINE with N=32 have been also evaluated considering a transient of frequency, phase, and amplitude. According to these results, the synchronization signals generation and the frequency tracking can be improved by using a low learning factor.

### Table 1. FF-ADALINE performance under different THD

<table>
<thead>
<tr>
<th>THD of test signal</th>
<th>1.5%</th>
<th>2%</th>
<th>3%</th>
<th>4%</th>
<th>5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Convergence time (ms)</td>
<td>110</td>
<td>115</td>
<td>108</td>
<td>114</td>
<td>112</td>
</tr>
<tr>
<td>Stead state estimation error (%)</td>
<td>1.3</td>
<td>1.35</td>
<td>1.27</td>
<td>1.31</td>
<td>1.33</td>
</tr>
</tbody>
</table>

These results confirm that the two methods offer good frequency tracking in this more realistic evaluation considering the utility voltage variations in frequency, in amplitude, and in harmonic content. The estimated mean frequency of the utility is within 50±0.1 Hz. This is well within the range of the Hydro-Québec frequency target values for normal conditions without disturbances that are established among 50±0.6Hz. As per the Hydro-Québec statistics, in normal conditions, frequency is within 50±0.2 Hz, in frequent disturbed conditions, frequency may be within 50±0.5 Hz and in rare disturbed conditions frequency may be within 50±1 Hz.

### 5.2 Power Control of Grid-Connected VSI

Hall-effect sensors are used to measure the $V_{PCC}(t)$ and $I_{VSI}(t)$ signals which are digitized with a 12-b ADC using a 10µs sampling period. The digitized signals $V_{PCC}(k)$ and $I_{VSI}(k)$ are sent to the FPGA circuit as the input of the two-channels ADALINE to be used in the synchronization and control algorithms VSI characteristics.

The user interface is configured to generate the set point of VSI control and to visualize the real-time information of rms values of voltage and current, the estimated active and reactive powers, the measured frequency of the generated signals, the THD of voltage and current, the waveforms of the measured voltage and current, and the estimated spectrum of voltage and current ($V_{PCC}$ and $I_{VSI}$). In the FF-ADALINE and VF-ADALINE cases, the power setup of load and VSI presented in Table 2 has been also employed.

The experimental results for the VSI synchronization and control using FF-ADALINE scheme are plotted in Fig. 3. From Fig. 3, the estimated active power of VSI corresponds to the set points, the frequency of the generated signals remains
close to the frequency of the utility voltage (50 Hz), the THD of the voltage remains quite constant at between 2% and 3%, the THD of the current varies with the output power of VSI, and the minimum THD current is obtained when the output power of VSI is close to the load power. The voltage and current trajectories at the start of VSI operation with active power set point $P_{\text{ref}}=300$ W.

Fig. 3. Estimated VSI powers, frequency of generated signals and THD of $V_{\text{PCC}}$ and $I_{\text{VSI}}$ when signal estimation, synchronization, and power control of VSI use FF-ADALINE scheme with $F_{\text{REF}} = 50$ Hz.

The experimental results for the VSI synchronization and control using VF-ADALINE scheme are plotted in Figs.4–6.

Table 2. Power setup of Load and VSI

<table>
<thead>
<tr>
<th>Setup</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{LOAD}}$ (W)</td>
<td>0</td>
<td>470</td>
<td>470</td>
<td>470</td>
<td>470</td>
<td>470</td>
<td>470</td>
</tr>
<tr>
<td>$P_{\text{REF}}$ (W)</td>
<td>0</td>
<td>0</td>
<td>300</td>
<td>400</td>
<td>450</td>
<td>350</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig. 4. Estimated VSI powers, frequency, and THD of $V_{\text{PCC}}$ and $I_{\text{VSI}}$ when signal estimation, synchronization, and power control of VSI use VF-ADALINE scheme.

Fig. 5. $V_{\text{PCC}}$ and $I_{\text{VSI}}$ waveforms when signal estimation, synchronization, and power control of VSI uses VF-ADALINE scheme.

Similar results are obtained concerning the voltage variations in relation with the output power of VSI and the load power. Fig. 11 shows the estimation of active and
reactive powers, the frequency of the synchronization signals, and the THD of \( V_{PCC} \) and \( I_{PCC} \) for the conditions of power already presented in Table 2. Fig. 11 shows the voltage and current trajectories at the start of VSI operation with active power set point \( P_{Ref} = 300 \) W.

The results obtained by using the FF-ADALINE or VF-ADALINE methods for power control are similar; however, more stability is observed in the voltage and frequency tracking when FF-ADALINE is employed, mainly because the frequency of the utility voltage remains close to the nominal frequency. On the other hand, if FF-ADALINE is employed and the frequency of the utility voltage is not close to its nominal value, then the estimation error increases, in that case it would be more advantageous to use VF-ADALINE.

5.3 Harmonics Analysis

The estimation of harmonics and the transient response of implementation of FF and VF ADALINE have been compared with the ones obtained. These three structures have been implemented in the same FPGA device and evaluated by using the loop co-simulation. The test signal is defined by

\[
v(t) = V \sin(2\pi ft + \theta) + 0.009V \sin(6\pi ft + \theta) + 0.017V \sin(10\pi ft + \theta) + 0.016V \sin(14\pi ft + \theta) + 0.0064V \sin(22\pi ft + \theta) + 0.0028V \sin(26\pi ft + \theta)\tag{13}
\]

taking into account in Table 3 the timing configuration in order to consider voltage, frequency and phase variations.

<table>
<thead>
<tr>
<th>Time Interval</th>
<th>0-0.3s</th>
<th>0.3-0.6s</th>
<th>0.6-0.9s</th>
<th>0.9-1.2s</th>
<th>1.2-1.5s</th>
</tr>
</thead>
<tbody>
<tr>
<td>V</td>
<td>120</td>
<td>120</td>
<td>115</td>
<td>118</td>
<td>123</td>
</tr>
<tr>
<td>f</td>
<td>60</td>
<td>60.4</td>
<td>60.4</td>
<td>59.45</td>
<td>60</td>
</tr>
<tr>
<td>( \theta )</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>

The results of the estimation error of the 3rd, 5th, 7th and 11th harmonics are plotted in Fig. 6. In terms of accuracy, it is to be noticed that the proposed methods (FF and VF-ADALINE) show better performance than MSOGI-FLL. This accuracy is going to be reflected in the power quality evaluation, in the orthogonal signals generation and consequently in the power control.

The online power quality analysis including the tracking of voltage and current spectrums, as presented in this paper, is very useful for the evaluation of power electronics converters [18] and the particular requirements of the local utility operator. As an example, the time evolution of the normalized current spectrum of VSI according to the variations of the output power. The mean values within one second of the estimated harmonics amplitude of the measured voltage have been computed and compared with the ones obtained by means of commercial power analyzer. The harmonics of the measured signals have been also computed offline by means of the FFT function available in MATLAB software.
6. Conclusions

In this work, a comparative evaluation of two real-time power control and analysis schemes based on hardware implementation of ADALINE for FPGA. The structures allow the generation of the orthogonal signals which have been successfully used for the synchronization of a grid-connected VSI and the real-time analysis of the power quality. The first method works at a fixed frequency and the second one offers the possibility of variable-frequency harmonics estimation being more accurate in signal estimation even if the frequency of the utility voltage is not at its nominal value. Both methods have been evaluated by experimentation for both signal estimation and power control of the grid-connected VSI.

The hardware implementations provides reduce complexity and processing time without expanding the utilization memory. These beneficial characteristics gives complementary functions are ideal for use in future SIMs, also compensation of harmonics and reactive power, and the monitoring of power quality.

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