Design and Analysis of 4-BIT SRAM using Sleepy-Stack with Keeper and Dram Using Microwind

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Abstract
As the technology increases the amalgamated compactness of transistor also increases. There is a demand for portable devices like mobiles, notebooks and laptops etc. For this compactness design, feature estimate is diminished by the enhanced innovation. Reduced feature size devices require low power for their activity. Diminished power supply lessens the edge voltage. Low limit gadgets have better performance yet sub-edge leakage current paramount in such a deep submicron regime. Henceforth reducing this leakage is a noteworthy incitement for architects. To explain this numerous fieldworkers have proposed divergent thoughts. In this paper we proposed 4-bit static RAM cell using sleepy-stack keeper approach and also we implemented the 4-bit DRAM. The schematic of RAMs has been developed using DSCH and its layout has been created using Micro wind

Key-words: Sub-threshold leakage, Deep submicron regime, SRAM, DRAM.

INTRODUCTION
Initially all processors and computers were made up of CPU with only one hard disk which has the speed of 80M-120MHZ which is very slower to give data to CPU in time. That is the reason they placed the RAM in between CPU and ROM which works with speed near to CPU speed. Later on CPU is updated with multitask processor then it needs high speed access memory that time RAM is divided into SRAM and DRAM. With the quick development of present day correspondences and signal processing system, handheld remote PCs and buyer gadgets are winding up progressively prevalent[1]. A computer uses RAM to temporarily hold instructions and data for CPU processing tasks. In networking equipment, memory is used to buffer information. The demand for static random access memory (SRAM) is expanding with extensive utilization of SRAM in versatile items, System On-Chip (SoC) and high-performance VLSI circuits. SRAM is critical segment utilized for the cache memory. Dynamic random-access memory (DRAM) is a type of storage that is widely used as the main memory[2].

BASIC 6T SRAM
It is a type of semiconductor. It can store each bit by the use of bistable latching circuitry. When the memory is not powered, the data will be lost in the SRAM. In the SRAM it does not periodically refreshed and it is more expensive. It is typically used for CPU cache. SRAM cell is made of 6 MOSFETs[3]. Each bit in an SRAM is stored on 4 transistors(M1,M2,M3,M4) that are from two cross coupled inverters. It has two stable states that are 0 & 1.

HOLD operation
Write Line is disabled, no reading and writing is possible

READ operation
Reading starts with preloading the Bitlines to 1. Now the Writeline gets activated. If Q is 1 then BL gets pulled to one and $\overline{BL}$ towards zero. A sense amplifier senses which line hast the higher voltage[4].

WRITE operation
Setting the Bitline to 1 (BL = 1, $\overline{BL} = 0$) then enabling the write line will write a one. The input-drivers have to be much stronger than the transistors.
SLEEPY STACK APPROACH

The sleepy stack approach has a structure combining the stack and sleep approaches by dividing every transistor into two half width and placing a sleepy transistor in parallel with one of the divided transistor. Sleep transistors are placed in parallel to the divided transistor closest to $V_{dd}$ for pull up and in parallel to the divided transistor closest to GND for pull down[5]. The sleepy stack approach can have advantages of both the stack approach and the sleep approach. During the active mode, the sleepy stack approach results in lower delay than the stack approach because sleep transistors placed in parallel reduce resistance and already on[6].

![Figure 3. sleepy approach](image)

PROPOSED WORK

The leakage reduction of the sleepy stack structure occurs in two ways. One is Leakage power is suppressed by high voltage transistors which are applied to the sleep transistors and the transistors parallel to the sleep transistors.[7] Another is Stacked and turned off transistors induce the stack effect.

According to forecast technology parameter, supply voltage VDD for 50nm and 90nm technology is taken as 0.5v,1.0v respectively.

![Figure 4. The 4-bit SRAM using sleepy stack with keeper](image)

CIRCUIT SIMULATION & TABLE

Here the 4-bit SRAM cell is designed using a sleepy stack with keeper technique and the waveforms shows the operations at different technologies. In this we can observed that if we increase the technology then the power consumption also increases[8].

![Figure 6. Waveforms of 4-bit SRAM cell at 90nm technology.](image)
**Figure 7.** Waveforms of 4-bit SRAM cell at 50nm technology.

**Table 1:** Area and power analysis of 4-bit SRAM

<table>
<thead>
<tr>
<th>SRAM design</th>
<th>Area</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-bit SRAM</td>
<td>113μm²</td>
<td>0.112μW</td>
</tr>
<tr>
<td>SSK 6T</td>
<td>143μm²</td>
<td>83.02μW</td>
</tr>
<tr>
<td>4-bit SRAM</td>
<td>270μm²</td>
<td>2.3mw</td>
</tr>
<tr>
<td>50 nm</td>
<td>360μm²</td>
<td>14.3μW</td>
</tr>
<tr>
<td>90nm</td>
<td>360μm²</td>
<td>0.23mw</td>
</tr>
</tbody>
</table>

**BASIC DRAM**

Dynamic random access memory (DRAM) is a type of random access memory stores each bit of information in a different capacitor inside an incorporated circuit. The capacitor can be either charged or discharged, these two states are taken to represent the two values of a bit, conventionally called ‘0’ and ‘1’. Since capacitors is charged, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposite to SRAM and other static memory. The main memory (the “RAM”) in personal computers is dynamic RAM (DRAM)[9]. It is also used in the laptop and work station computers as well as video game.

**WRITE operation**

Writing operation works with both bitlines to charge or uncharged capacitors.

**READ operation**

In Read operation, the voltage of a bit line is discharged to the ground through the transistor where the gate is charged with the high voltage[10]. The Read operation is non-destructive since the voltage stored at the node is maintained during the read operation.

**PROPOSED WORK**

The correspondence layout of the 4-bit DRAM cell is implemented on microwind tool. The figure shown below

**CIRCUIT SIMULATION & TABLE**

MICROWIND software is used for this approach to analyse the leakage power dissipation. The waveforms of the DRAM cell is shown below.

**Figure 8.** 1T DRAM cell

**Figure 9.** 4-bit DRAM schematic

**Figure 10.** Layout of 4-bit DRAM

**Figure 12:** waveforms of DRAM at 90nm technology.
In this we observed that if we increase the technology then the power consumption also increases.

Table 2: Area and power analysis of 4-bit DRAM

<table>
<thead>
<tr>
<th>DRAM design</th>
<th>Area</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-bit DRAM</td>
<td>53μm²</td>
<td>2.06mw</td>
</tr>
<tr>
<td>4-bit DRAM</td>
<td>88μm²</td>
<td>0.21μw</td>
</tr>
<tr>
<td>50 nm</td>
<td>88μm²</td>
<td>0.15μw</td>
</tr>
<tr>
<td>90nm</td>
<td>88μm²</td>
<td>1.39μw</td>
</tr>
</tbody>
</table>

CONCLUSION

In this paper we can observe that by using sleepy stack with keeper technique we can reduce the power consumption in static random access memory and also we implemented the dynamic random memory of 4-bit. Both schematics are designed in DSCH tool and layout implemented in MICROWIND tool. And also here we can observe that by reducing the technology we can save the power dissipation here we give the comparisons between 50nm and 90nm technology.

REFERENCES