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An FPGA Implementation of Low Dynamic Power & Area Optimized 32-Bit Reversible ALU

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Abstract

Today's Computer chips are facing a severe problem with power dissipation in addition to that heat generation. Reversible logic reduces power consumption as zero-energy computation has inspired it. It has various areas envisioned for its applications; they are low power CMOS design, Quantum & Optical computing, Nano-Technology, DSP, etc. Using this Reversible logic different combinational circuits are designed, like Decoders & Multiplexers. They have enhanced performance when compared to the conventional Circuits. This paper describes Design and Implementation of 32-Bit ALU built using reversible decoder controlled combinational circuits on Spartan3E (XC3S500E-FG320-5) FPGA. This proposed designed architecture provides 1.6 times less dynamic power consumption to conventional design and occupies 3% of the total memory in Spartan3E FPGA and saves area by 91% to the traditional design. This architecture has been modelled with Verilog in Xilinx ISE Design Suite 14.3.

Keywords: Reversible logic, Reversible decoder, Arithmetic and Logical Unit, Low dynamic power, Area Optimization

INTRODUCTION

As the capacity and density of an integrated circuit gradually increase in recent time's power dissipation has become a critical factor in design. Such VLSI circuits need more power so that the power consumption will be high. Thus, it can dissipate more heat causes damage to the reliability ICs. [1] By using Reversible Decoder for designing Combinational circuits power consumption is reduced to an optimum when compared to a conventional decoder based combinational circuits. [2] Reversible Circuits have an equal number of inputs and outputs and has a bijective mapping between them. Hence input vectors can always be uniquely derived from output vectors and vice versa. ALU is the basic building block of CPU. An ALU is a combinational circuit that can have one or more inputs and only one output. ALU output is dependent only on inputs applied at that instant as a function of time and not on past conditions. Basic ALU consists of two operands and one input to select the operation [10]. The paper is organized as follows. Section II presents the reversible logic concept Section III presents a review of earlier work Section IV is about reversible ALU and how a Reversible decoder is to be used in it, In Section V the simulation results are given. Finally, Section VI provides a conclusion.

REVERSIBLE LOGICS

The concept of reversible logic gates is used for reducing power consumption and loss of data. Reversible computing is the application principle of recycling to the computing. It is because input can be reconstructed from the output. This logic uses the reversible gates which have the same number of inputs and outputs. Some of the cost metrics like garbage outputs, number of gates, Quantum cost, constant outputs are used to estimate the performance of reversible circuits. [1] A Reversible circuit design can be modelled as a Sequence of discrete time slices and depth is a summation of total time slices.

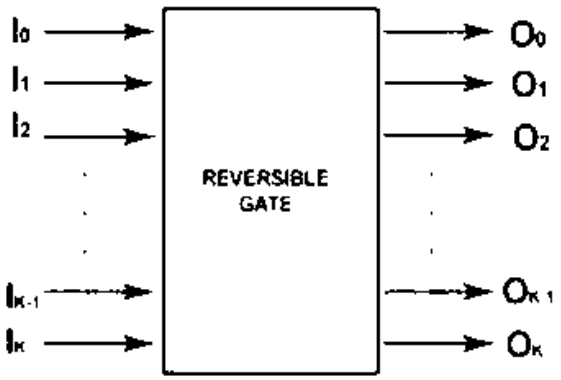

Figure 1: A n × n Reversible Gate

In Digital Electronics, the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various techniques are given to the design of combinational and sequential circuits in the undergoing research. The design of different combinational circuits like a binary comparator, Full adder, Full subtractor, Multiplexer circuits using reversible decoder is proposed with optimum Quantum cost. The reversible logic gates are

NOT GATE:

A NOT gate is the single Reversible Logic gate. It is 1×1 Reversible Logic Gate. The Not gate gives merely the complementary of the input-output as shown in the Figure 2.

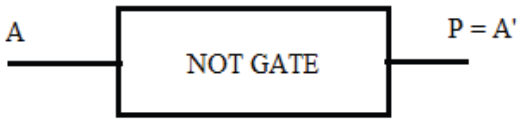

Figure 2: NOT Gate

FEYNMAN GATE (FG):

Feynman gate is a 2×2 reversible gate as shown in below Figure.3. The Feynman gate is used to replicate the required outputs.

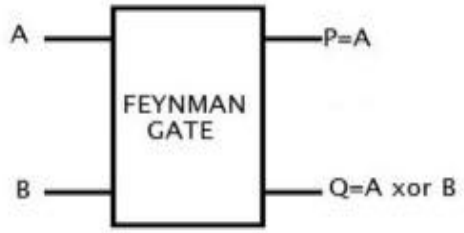

Figure 3: Feynman Gate

DOUBLE FEYNMAN GATE (DFG):

Double Feynman Gate is a 3×3 reversible gate. The outputs are expressed as shown in the below Figure.4. This gate can be used for replicate outputs.

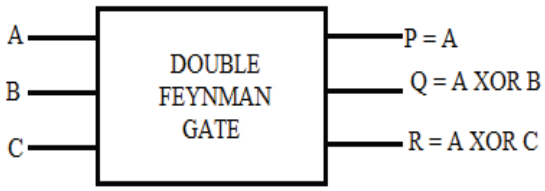

Figure 4: Double Feynman Gate

TOFFOLI GATE(TG):

Toffoli Gate is a 3×3 reversible gate. The outputs expressed as shown in the below Figure.5.

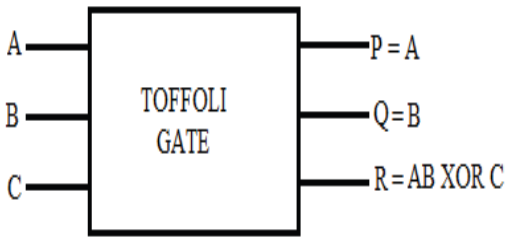

Figure 5: Toffoli Gate

FREDKIN GATE (FDG):

Fredkin Gate is a 3×3 reversible gate. The outputs expressed as shown in the below Figure.6.

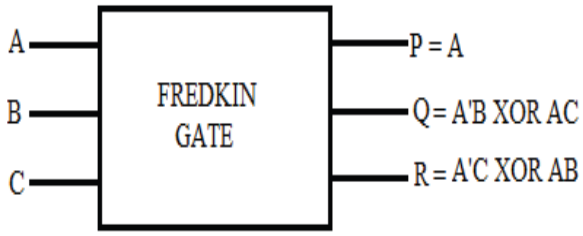

Figure 6: Fredkin Gate

PERES GATE (PG):

Peres Gate is a 3×3 reversible gate. The outputs expressed as shown in the below Figure.7.

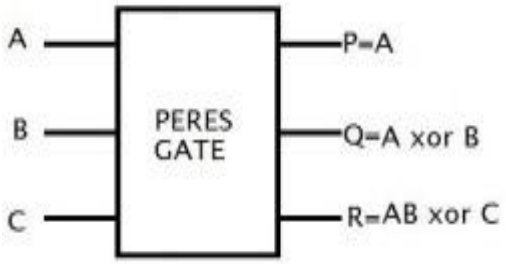

Figure 7: Peres Gate

TR GATE:

TR Gate is a 3×3 reversible gate. The outputs expressed as shown in the below Figure.8.

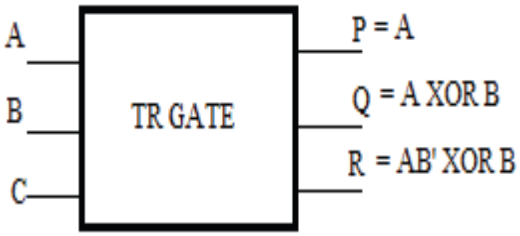

Figure 8: TR Gate

REVERSIBLE DECODER

The circuit that changes a code into a set of signals is decoder. The decoder does reverse encoding. The name "Decoder" means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output. Here in this paper we make a decoder with reversible logic

The new design of 4×16 decoder whose Quantum Cost is less than the previous model. Replacing Fredkin gates for designing 2×4 decoder [11] reversible gates like Peres gate, TR gate, NOT gate and CNOT gate is used as shown in Figure.9.

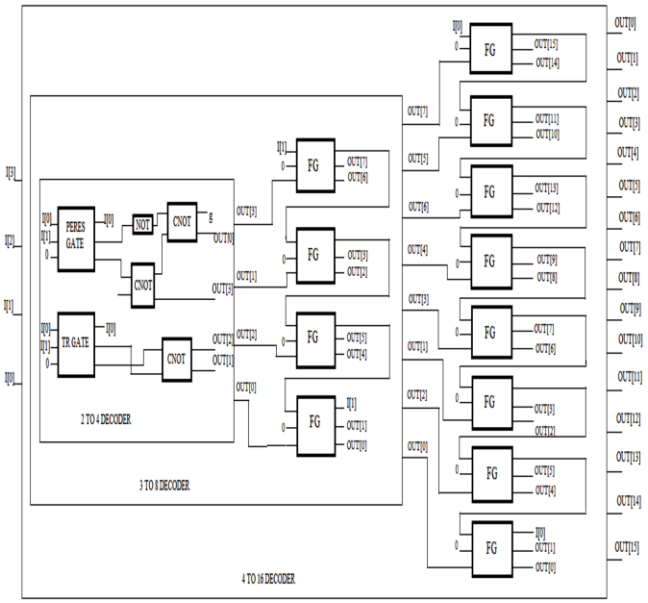

Figure.9: Reversible decoder

REVIEW OF EARLIER WORK

[1] Different Reversible Decoder circuits like 2×4, 3×8, 4×16are designed using Fredkin Gates (mainly), Feynman gates and Peres gate. Some combinational circuits like comparator adder, subtractor, multiplexers, etc., are created using these decoders. The concept of duplicating a single output to a required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation. The second input of Feynman gate was made to 0 which drives two split equivalent outputs. For designing a full adder, a 3 to 8 decoder and two four input OR gates are required. The minterms for SUM and CARRY derived from output pattern of the decoder.

Equation for sum S=∑ (1, 2, 4, 7)

Equation for carry C=∑ (3, 5, 6, 7)

Similarly, the full subtractor designed with the min term expressions of the decoder.

Equation for difference D=∑ (1, 2, 4, 7)

Equation for Borrow B=∑ (1, 2, 3, 7)

To design a multiplexer using a reversible decoder, reversible two inputs, AND gates, two input OR gates are required. The two input AND Gate and OR gate is designed using Fredkin gate. By using these designed gates, we can improve those gates to the required number of input gate. Each output line from the decoder driven by to 2 input AND gate along with multiplexer input. The outputs of all AND gates are made to operate that particular input OR gate [1].

The input binary integer values act as the selection lines. Similarly, by using 4×16 decoder, a 16×1 multiplexer is designed. In the above min term expressions, we can observe that the same min term output of decoder drives sum and carry outputs of full adder (i.e., out [7] of decoder output pattern). Since Fan-out is not allowed in reversible logic, the Feynman gate is used to duplicate outputs. Similarly, for full subtractor outputs of the decoder (i.e., out [1], out [2] and out [7]) are duplicated. By using this full adder, a 4-bit full adder/subtractor is designed. To design 4-bit full adder/subtractor circuit, four full adders are required. The Cin input drives the first full adder. If Cin is given with low input 4-bit addition is performed, and if Cin is given with high input the 4-bit subtraction in the form of 1's complement addition is shown [1].

REVERSIBLE COMBINATIONAL CIRCUITS AND REVERSIBLE ALU

REVERSIBLE COMBINATIONAL CIRCUITS:

A combinational circuit output of any circuit depends on the current values of inputs. The output never depends on any previous value of input as well as the past output value. Here in this paper, we design combinational circuits like Adder, subtractor, comparator Multiplexer, etc., with reversible logic based Decoder.

4×16 Reversible Decoder

A reversible decoder is designed with reversible gates like Feynman Gate, Fredkin Gate, Not gate, Peres gate, TRG gate etc., The RTL schematic of 4×16 decoder is given in below Figure.10

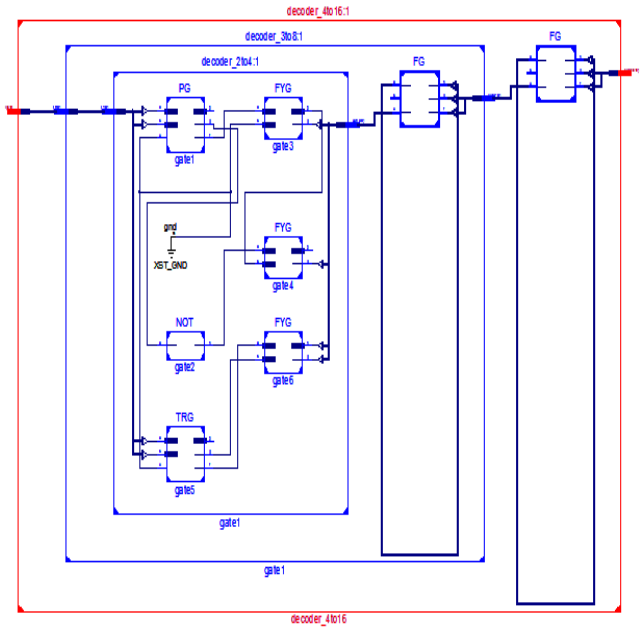

Figure 10: RTL Schematic of Reversible decoder

Full Adder/Subtractor:

A full adder designed with the help of reversible decoder here such that it has better performance criteria's is shown in Figure.11

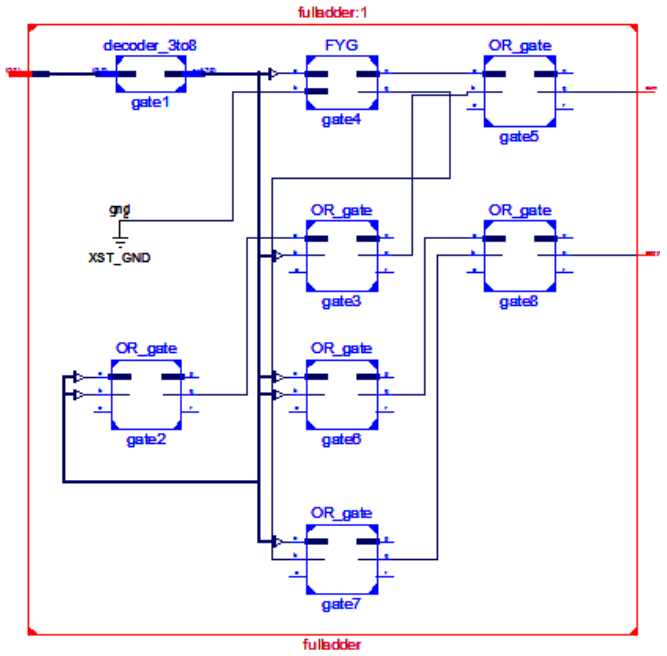

Figure 11: RTL schematic of Full adder with reversible decoder

A full Subtractor designed with the help of reversible decoder here such that it has better performance is shown in Figure.12.

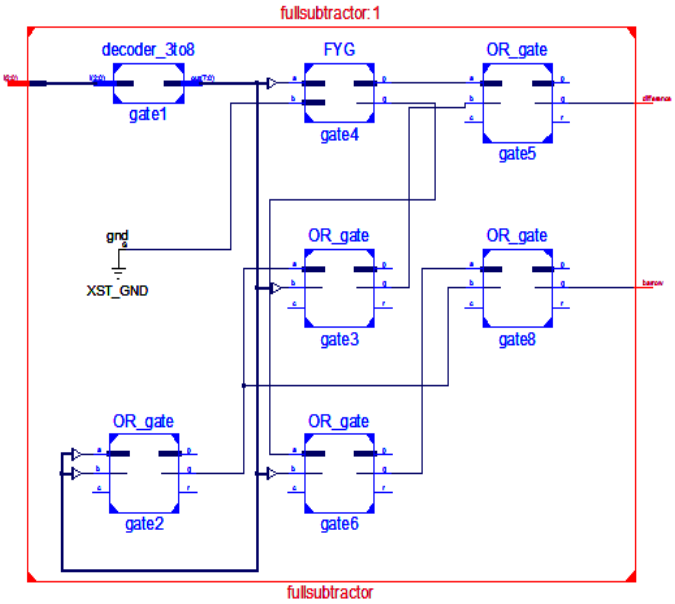

Figure 12: RTL schematic of Full subtractor with reversible decoder

Reversible Multiplexer:

Multiplexer is used to select the data from the lines it is also called as data selector. It is shown in Figure.13.

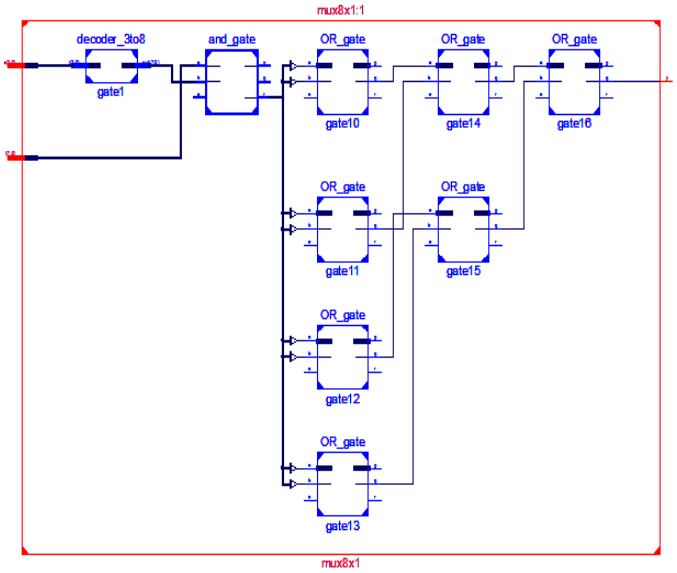

Figure.13: RTL schematic of Multiplexer with reversible decoder

Arithmetic and logic unit (ALU):

An ALU is the edifice integrant of microprocessors and microcontrollers. ALU performs operations as per the designed circuit architecture. The 32-Bit reversible ALU design flow shown in the flowchart Figure.14. Initially, the reversible logic gates are designed like Feynman, Toffoli, Fredkin, Double Feynman, Peres, TG, etc. Using these gates, we designed reversible decoder combinational circuits like a full adder, full subtractor, multiplexer, etc. These designed circuits used in developing of reversible ALU.

It has proven that the novel design in Figure.9 occupies less quantum cost, gates replaced by using the 2x4 decoder. In this proposed plan ALU is embedded using decoder controlled combinational circuits structured using reversible logic gates. The combinational circuits are designed using this decoder logic, and these are implemented in the design of Reversible ALU. The designed circuit implemented on Spartan3E (XC3S500E-FG320-5) FPGA kit. Reversible ALU occupies 3% of the area and saves area by 91% than conventional ALU. The dynamic power consumption decreased by 1.6 times than regular ALU. And total power is reduced by one time. In the proposed design, the dynamic power which is switching of logic from 0 to 1 and vice-versa is significantly reduced which is a crucial cause for heat dissipation in the chips. Furthermore, power consumption and heat dissipation can be reduced by implementing different strategies and by manually redesigning the circuit to reduce routing logic. Applying the constraints and using different novel designed gates and circuits give better performance to design

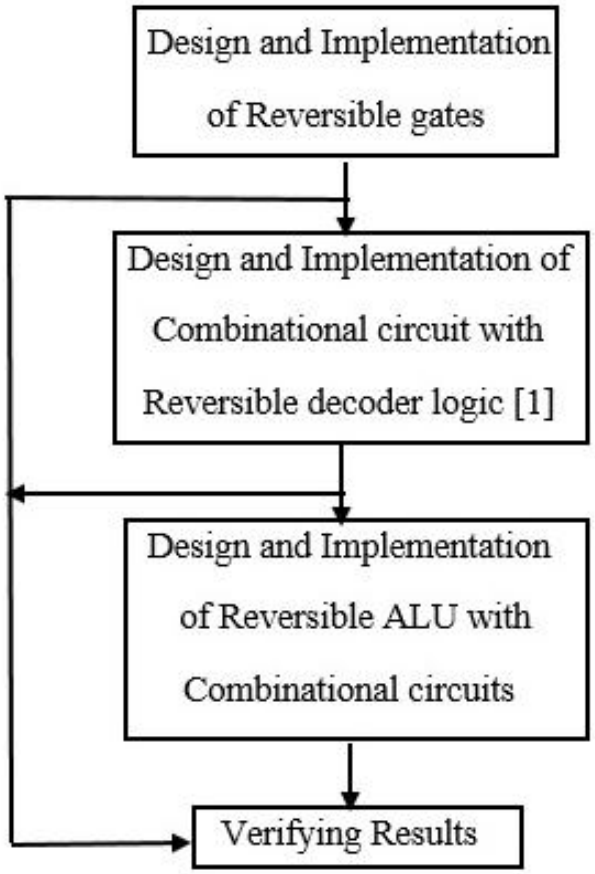

Figure 14: Flowchart of the Design

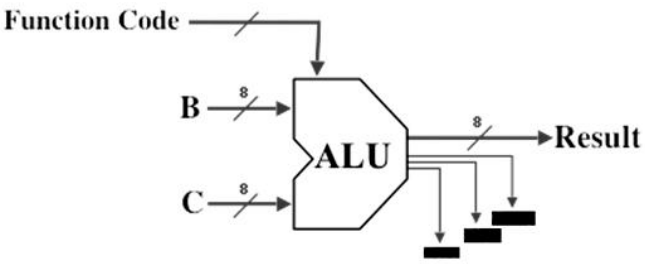

Figure 15: A simple 8-bit ALU

In the Above Figure.15, the function code referred to the selection input of ALU operations which can be either logical or arithmetic operation.

SIMULATION RESULTS

32-bit ALU with Reversible Logic:

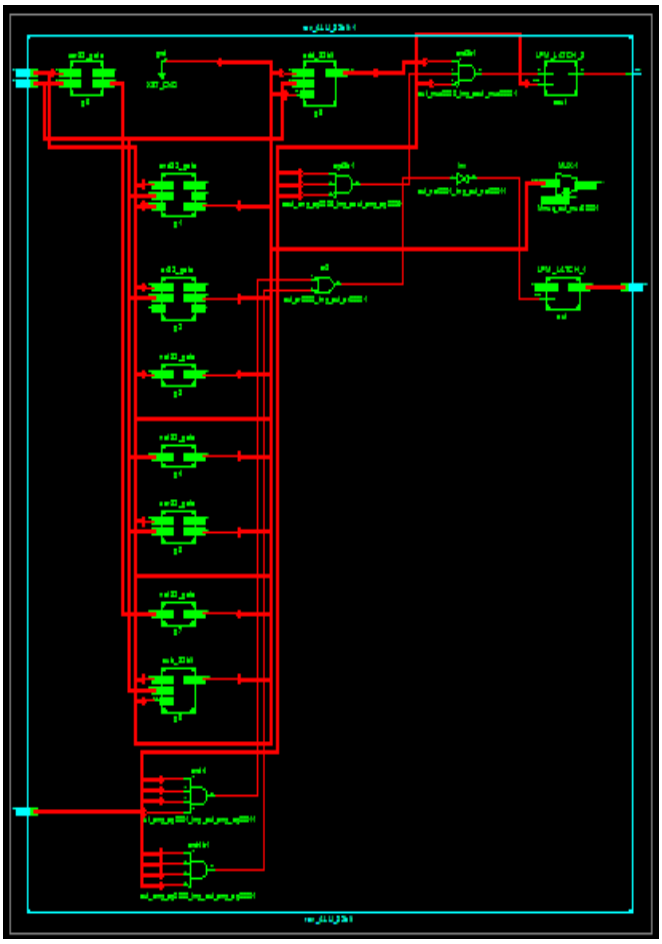

Figure.16: RTL schematic of 32 bit ALU

In ongoing miniaturization shrinking the size of the transistor and power dissipation are critical problems faced by the engineers. The advantage of Reversible logic circuits is that it occupies low power consumption less delay and low area when compared to the traditional logic design. The design of the circuit is same for both conventional and reversible logic. The entire design is modelled using Verilog HDL in Xilinx ISE design suite. The test bench is written for simulation using Verilog text fixture module. The design is simulated using Post-Place and route method of simulation. This maximum time taken for the input and output can be viewed using this simulation technique. This simulation provides us to get the estimated time taken by the circuit to implement in the real-time application.

In the simulation results of reversible ALU, Figure.16 shows the RTL schematic of the 32-bit ALU and Figure.17 shows the simulated output of 32-bit ALU and the results compared with the conventional ALU is tabulated in Table 1. Area & dynamic power are the two parameters that are varied to the traditional design of logic. In this design, the power occupied by the by reversible logic is decidedly less when compared to the conventional logic.

Figure.18 shows the pictorial view of the area optimized (area measured in slices) by the Rev_ALU towards traditional ALU. Figure .19 shows the pictorial view of the Dynamic power consumed (measured in milliwatts) by the Rev_ ALU towards conventional ALU. Figure.20 shows the pictorial view of the Total energy consumed (measured in milliwatts) by the Rev_ ALU towards conventional ALU.

Table 1: Summary Report Rev_ ALU vs ALU.

Parameters /ALU	Area (Slices)	Dynamic Power(mw)	Total Power(mw)
Rev_ALU	322	0.72	81.71
ALU	351	1.17	82.17

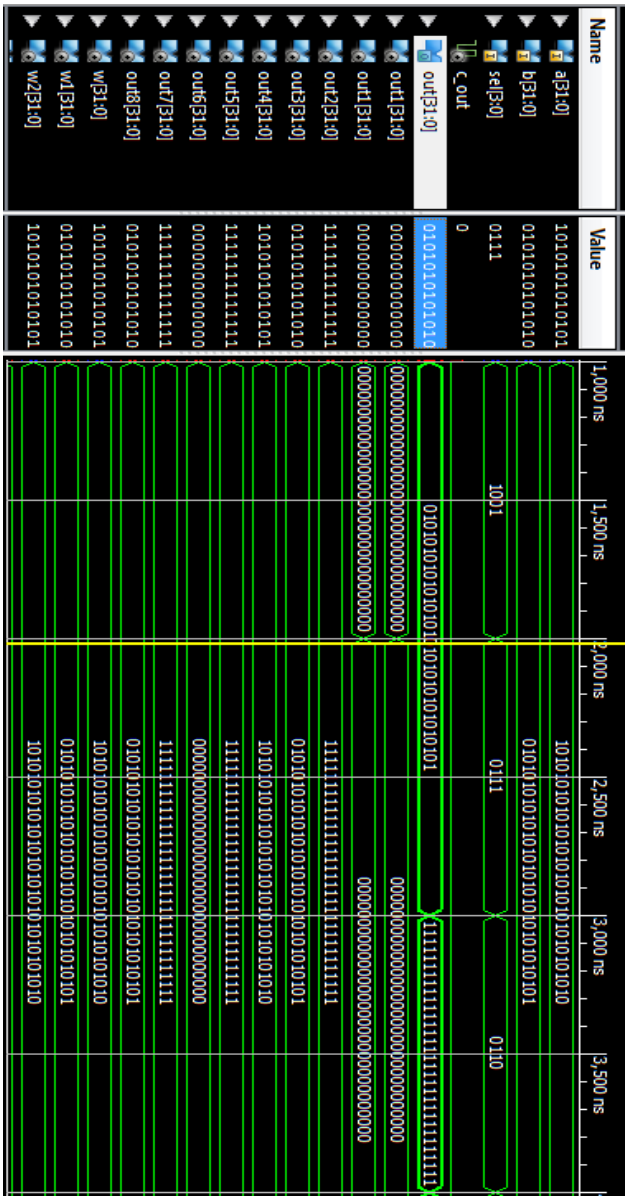

Figure.17: Simulated output of 32-bit ALU

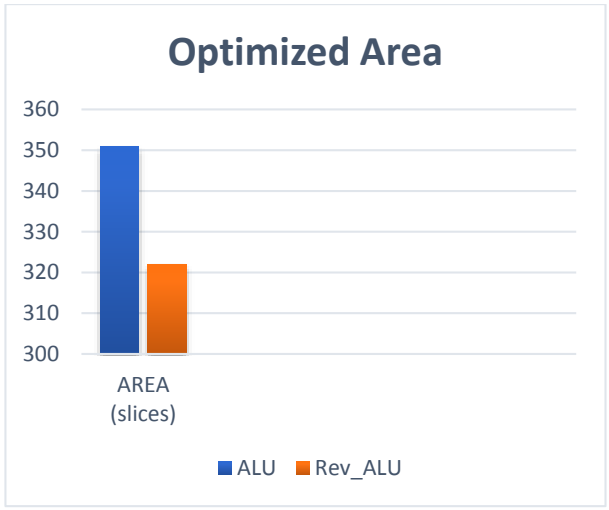

Figure 18: Representing Area Rev_ALU vs ALU

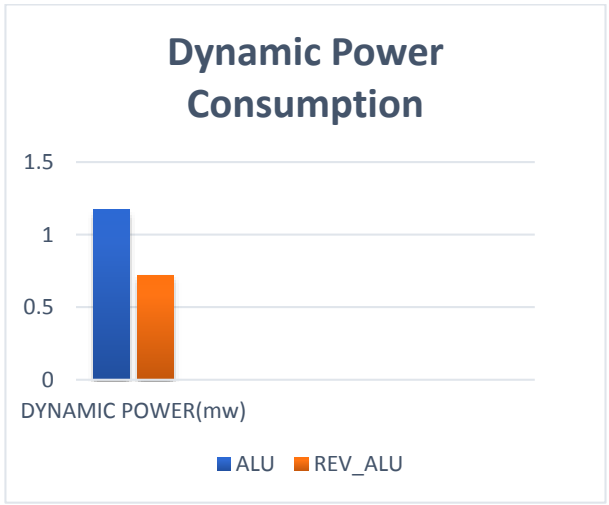

Figure 19: Representing dynamic power consumption Rev_ALU vs ALU.

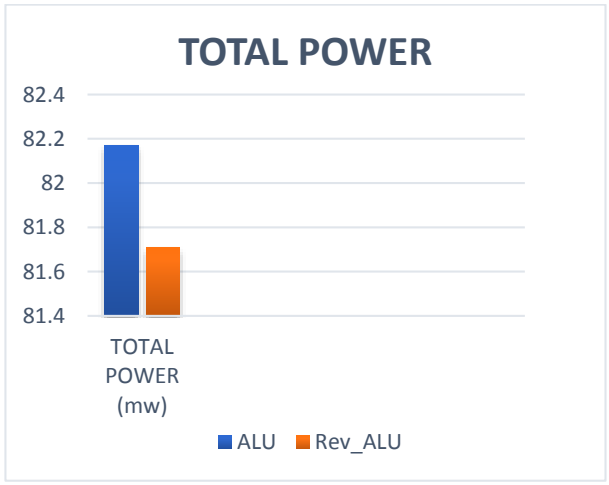

Figure 20: Total power consumption Rev_ALU vsALU.

CONCLUSION

Reversible logic computation has various applications in different fields. This proposed reversible ALU architecture modelled on Spartan3E (XC3S500E-FG320-5) FPGA kit using decoder controlled reversible combinational circuits performing arithmetic and logical operations. In this design, the area is reduced by 91%, and dynamic power consumption decreased by 1.6 times when compared to conventional architectures. Furthermore, improvements can be made in future designs by implementing calculated constraints to optimize area, power, and delay for most exceptional performances.

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