

Asynchronous Level Crossing ADC Design for Wearable Devices: A Review

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Abstract

Asynchronous level crossing ADCs (LC ADC) saves power through non-uniform sampling making it suitable for wearable devices. This paper presents a review of asynchronous level crossing ADCs based on an exhaustive survey of papers from 1966 to 2016. The various architectures of level crossing ADCs are studied and classified into two types, LC ADC with feedback DAC and LC ADC with Flash ADC like architecture. The performance trends such as figure of merit, resolution, power consumption, die area, supply voltage scaling, and technological scaling are compared with other asynchronous ADCs and synchronous ADCs to evaluate the suitability of LC ADCs in wearable devices. The algorithm for general framework of LC ADC using MATLAB is presented in this paper. The signal from the general LC ADC is reconstructed using polynomial interpolation achieving a SNDR of 32.27dB.

Keywords: Wearable, Asynchronous, Synchronous, ADC

INTRODUCTION

The advent of personalization of medical treatment has brought wearable technology to forefront. A patient can rest comfortably at home and can be monitored by a physician using wearable monitoring devices. This will reduce the risk and also reduce the treatment cost for individual patients. Personalized and customizable forms of medicine administration will become more effective with the help of wearable devices. Routine physiological signal monitoring will provide more information. This information can be used to develop more advanced drugs, devices and artificial intelligence.

Besides medical treatment applications like fitness tracker, hearing aids, speech and voice therapy aids, ECG and EEG monitoring, wearable technology is used in sports tracker, navigation tools, communication gadgets and wearable cameras with augmented reality and virtual reality headsets.

Wearable devices require their batteries to have longer battery life and smaller area for the convenience of the customer. Lower power consumption, lower supply voltage and smaller size are desirable qualities in wearable devices. Analog to digital converters (ADC) are integral part of wearable devices. Synchronous ADCs and asynchronous ADCs are the two main types of ADCs. Most of the ADCs available in the market are synchronous. The presence of global clock in synchronous ADCs increases its power consumption and area. Other disadvantages of synchronous ADCs are clock skew, metastable behavior and electromagnetic interference. The

asynchronous ADC is now emerging as a promising research field evolving to be an alternative for synchronous ADCs in various low power wearable and portable applications.

Level crossings ADCs discussed in this paper are asynchronous ADCs that generate output samples only when the input signal crosses a threshold level. This non-uniform sampling approach results in lower number of samples resulting in lower power consumption.

The paper begins with an introduction to the asynchronous ADCs and level crossing ADCs followed by a discussion about the previous literature on level crossing ADCs. Next section compares the level crossing ADCs with other asynchronous ADCs. This is followed by a comparison of level crossing ADCs with synchronous ADCs and conclusion.

PREVIOUS LITERATURE ON LEVEL CROSSING ADCS

Level crossing sampling is a non-uniform sampling approach first introduced by H. Inose et al in 1966 [1]. Level crossing ADC generates output samples whenever the input signal crosses a threshold level and the time between the level crossing samples are quantized and encoded in uniform steps[2], [3]. Level crossing sampling is shown in Figure 1.

Level crossing ADC architectures in previous literature can be generally classified into two types: LC ADC using feedback DAC [4-6], [9], [10-17],[19],[20],[21]and LC ADC with flash ADC like architecture [7],[8],[18],[22]. A general architecture of LC ADC using feedback DAC is shown in Figure 2. They usually consist of feedback DAC, comparators, counter and timer. The feedback loop with the DAC keeps the comparison window of the comparators around the input signal. The power consumption of DAC and comparator dominates the overall power consumption. The benefits of the DAC are rail to rail input swing, decreased settling time, decreased leakage and decreased output drift. Table 1 shows the performance summary of the level crossing ADC using feedback DAC.

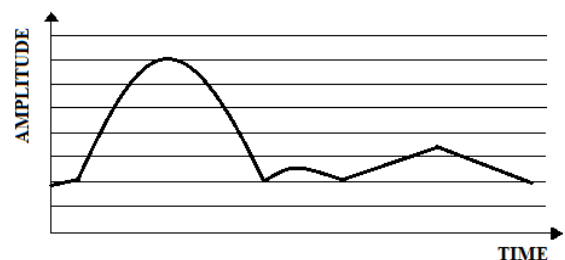


Figure 1. Level crossing sampling

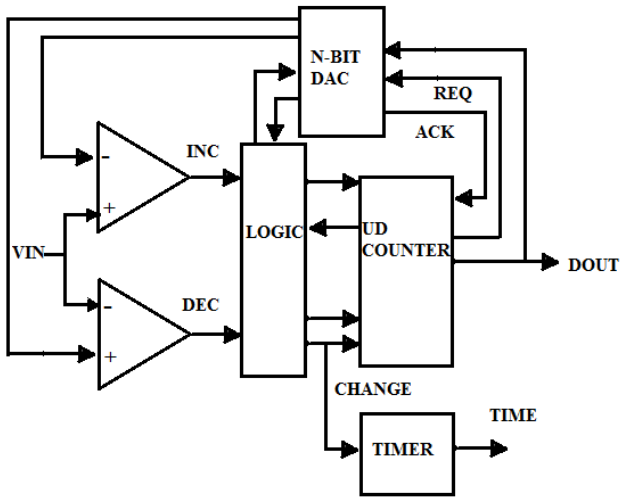


Figure 2.General LC ADC architecture using feedback DAC

The general architecture of LC ADC with FLASH ADC like architecture is shown in Figure 3. The comparators shown in the circuit compares the input signal with the corresponding threshold levels generated by resistive or capacitive circuit [7], [8], [18] or by sequential algorithmic circuitry [22]. The absence of the feedback loop gives more stability to the flash type LC ADC whereas power consumption of the circuitry is dominated by the number of comparators. Performance characteristics of LC ADC with FLASH ADC like architecture are shown in Table 2.

The lowest performance metrics both in terms of power consumption and area was achieved in the LC ADC with feedback DAC proposed by Li Y et al. (15) as shown in Table 1. This dramatic reduction was achieved by using a novel level crossing detection technique. The proposed LC ADC uses a 1 bit DAC instead of n bit DAC used in conventional LC ADC architectures.

Table 1. Performance characteristic of LC ADC with feedback type DAC

LC ADC	[4]	[5]	[11]	[13]	[14]	[15]	[17]	[19,20]	[21]
Technology (nm)	180	90	180	130	180	180	250	180	500
Supply voltage (v)	0.8	1	0.7	0.8	0.7	0.8	-	1	3.3
Resolution (bit)	8-12	8	4-8	4-8	8	6	6	-	7
Reconstruction	-	Test DAC	6 th order interpol-ation	Test DAC	3 rd order interpolat-ion	3 rd -6 th order interpolat-Ion	-	5 th order interpo-lation	-
SNDR(dB)	-	47-62	43.2	47-54	50	40-49	38.6-53.7	46.4-50.2	34
Input bandwidth	114 KHz	200 Hz -4 KHz	1Hz-1.1KHz	20Hz-20 KHz	5KHz	5Hz-3.3 KHz	1-22 KHz	0.11 KHz - 1.1KHz	1 KHz
Full-scale Input (V _{PP})	-	0.5	1.4	0.72	0.8	1.6	-	10m	2.68
Power consumption	1.6 mw	40 μw	25μW	2.6-7.4 μW	1.42μW	313-582Nw	16.1-17.0mW	8.49 μW	10.7 μW
Active area (mm ²)	0.027	0.06	0.96	0.36	-	0.045	0.27	0.49	-

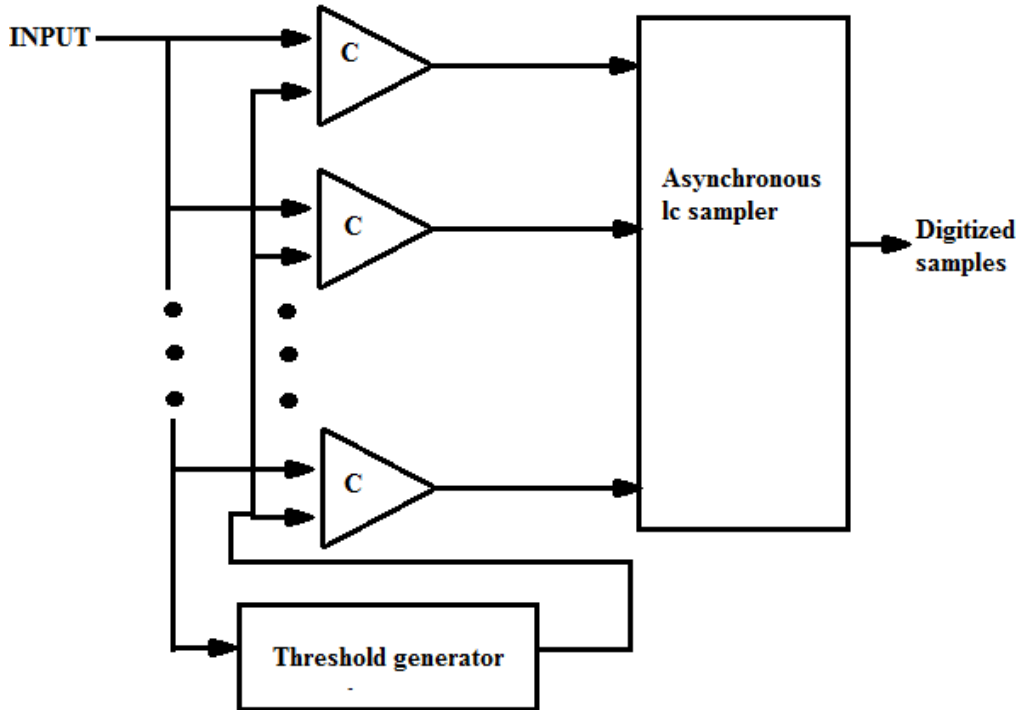


Figure 3. General Architecture of a LC ADC with FLASH ADC like architecture

Table 2. Performance characteristics of LC ADC with FLASH ADC like architecture

	[7]	[8]	[18]
Technology(nm)	180	(Simulated in MATLAB)	350
Supply voltage (V)	2.2	-	-
Resolution (bits)	4	-	4
Reconstruction	-	6 th order polynomial interpolation in MATLAB	ACT algorithm
SNDR (dB)	-	84.5	75
Input bandwidth	5MHz	9.42KHz	1-10MHz
Full-scale Input (V _{PP})	-	Varies	10mV-1.65V
Power consumption	438μW	-	175mV
Active area	-	-	1.8 mm ²

COMPARISON WITH OTHER ASYNCHRONOUS ADC ARCHITECTURES

Data was collected through an exhaustive survey of IEEE, Springer, Elsevier journals and conference publications presenting measured ADC performances for past 15 years. The evaluated performance trends like power consumption, area, process technology, signal to noise distortion ratio (SNDR), effective number of bits (ENOB), supply voltage of asynchronous ADCs like level crossing ADCs[1-22], FLASH ADCs[23], sigma delta ADC[24-26], successive approximation register ADC[27-35], binary tree ADC[36-38] and pipeline ADC[39-40] are given in Figure 4 .

The power consumption of the asynchronous ADCs has drastically reduced over the years making them an excellent choice in low power applications. The SAR ADCs and level crossing ADC architectures have the lowest power consumption amongst the various asynchronous ADC architectures. The power consumption of the ADCs has been reducing over the decade. At the same time, the CMOS technologies used to implement the surveyed ADCs have scaled down from 600nm to 40nm technology. The power supply voltages have also been reduced with the reduction in the technology over the years. The supply voltage has varied from 5V supply to 0.7V.

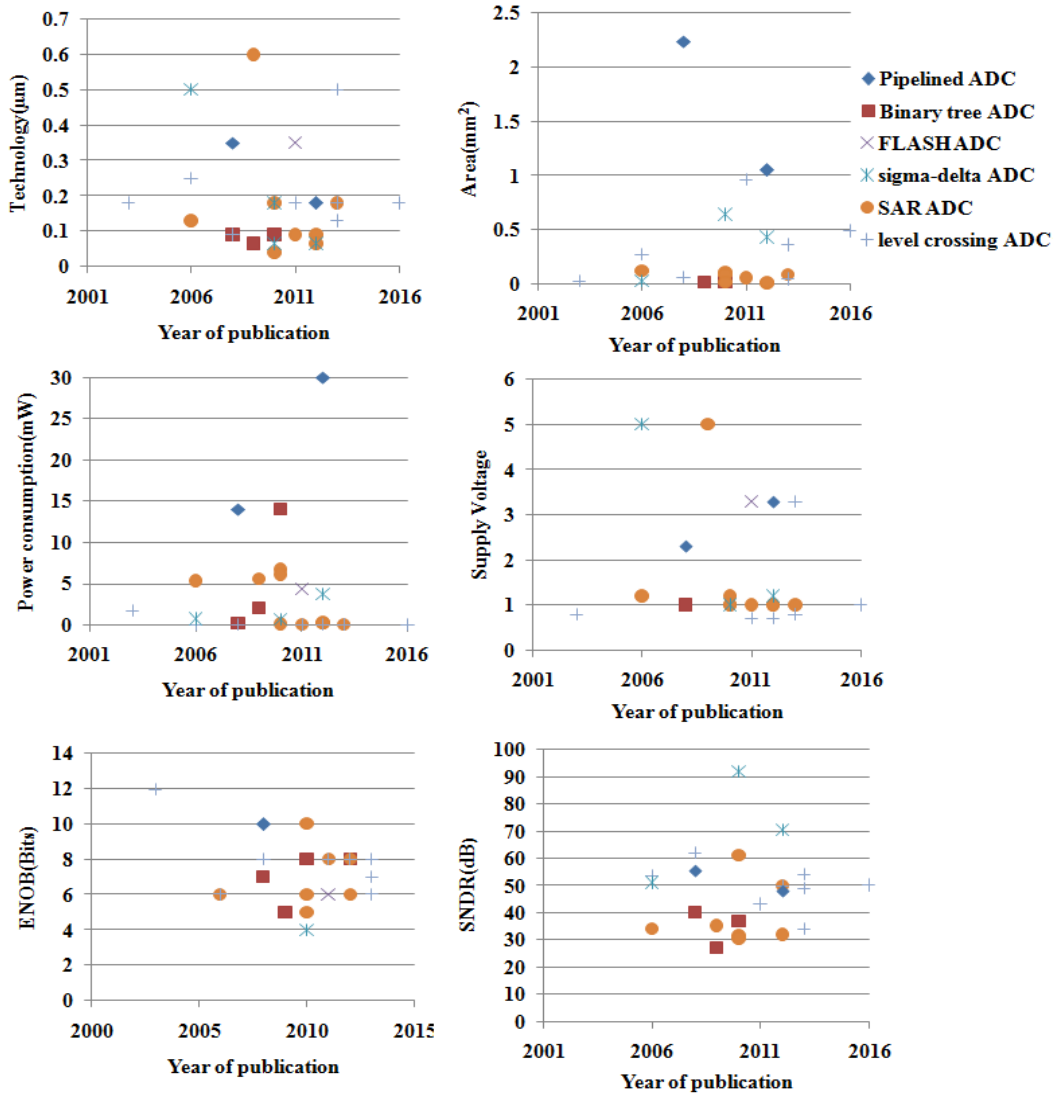


Figure 4. Performance trends of different asynchronous ADCs over past 15 years

Asynchronous ADCs are relatively new research field emerging as an excellent alternative in place of synchronous ADCs. Level crossing ADCs offer lower sampling rate, power consumption and area than other asynchronous ADCs. Level crossing ADCs working in Hz to MHz frequency regime has been reported. Level crossing ADCs has been mainly used in embedded sensing systems, such as environmental sensors (temperature and pressure sensors), implantable biomedical applications, hearing aids and ultrasound applications [4], [7], [11], [12], [14], [15], [18]. The delta-sigma ADC architectures are also used in biomedical applications and also operate in Hz to MHz frequency regime [41]. Asynchronous SAR ADCs are faster and have lower power consumption than the synchronous SAR ADCs and can be used in applications such as wireless communication, imaging and in ISM (Industrial, scientific and medical bands) radio bands [28], [29], [30]. High input bandwidth in the range of GHz and medium resolution achieved by asynchronous SAR allows its use in radio frequency subsampling operation [25], [27]. It can be used in low energy radios in ISM (Industrial, scientific and medical bands) radio band due to high power efficiency. It has

been used in biomedical applications such as multisensory system and for recording biomedical signals such as ECG and EEG [30].

Asynchronous binary ADCs are suitable for digital wireless applications such as Ultra Wide Band (UWB) and Wireless Personal Area Network (WPAN) [37]. Ultra low area of binary tree structure presented by Petrellis et al. favors its use in sensor networks [38]. The higher accuracy of asynchronous pipeline ADC enables its use in self-triggered sensors such as in spectrometers. Spectrometers are used for astronomical applications as well as biomedical applications [39]-[41].

Comparison with other asynchronous ADC architectures shows that level crossing ADCs have achieved lower area and power consumption without compromising other performance metrics such as ENOB and SNDR making it an excellent choice for wearable devices. The power supply demands has been reduced drastically for level crossing devices with the lowest power supply voltage in the asynchronous ADC architectures being used by level crossing ADCs.

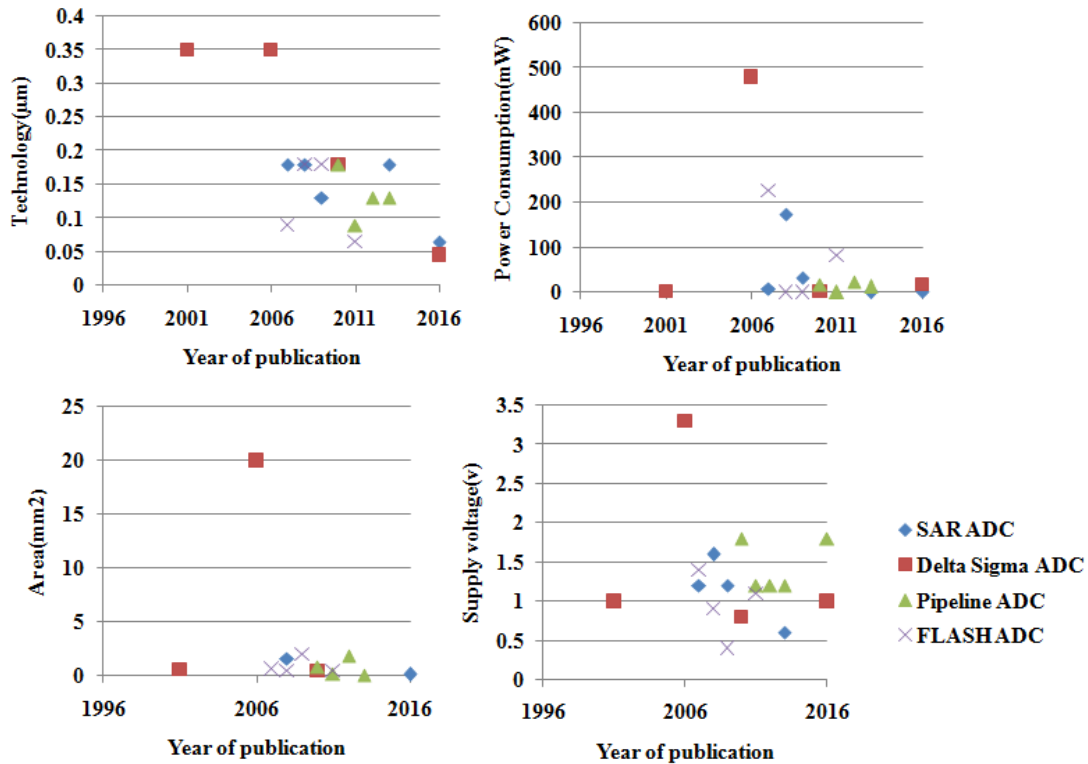


Figure 5. Performance trends of different synchronous ADC architecture over years

COMPARISON WITH OTHER SYNCHRONOUS ADC ARCHITECTURE

Performance trends of synchronous ADC architectures SAR ADC [42]-[46], delta-sigma ADC [47]-[50], pipeline ADC [51]-[55] and FLASH ADC [56]-[59] such as technology, area and power consumption were collected through exhaustive survey of IEEE, Springer and Elsevier journal and conference publications. Figure 5 shows the performance trends of different synchronous ADC architectures over the years. Figure 4 and Figure 5 infers that asynchronous ADCs offers superior performance both in terms of power and area compared to the synchronous ADC with LCADC playing a superior hand. LC ADC is thus inferred as an excellent choice for wearable devices.

Algorithmic Implementation of a General LC ADC Framework

This section presents the algorithmic implementation of a general LC ADC framework with 2^b-1 comparators. The input signal x_t bounded by a voltage A is given to the system. The level set, W_k is assumed to be spaced at $A/2^b$ intervals. The input signal x_t is sampled at a frequency of f_s Hz which is equal to $1/t_s$ to give the sampled signal x_{t_i} . The sampled input signal x_{t_i} is compared with the levels, W_k and a level crossing is recorded if the following equation holds.

$$(x_{t_i} - w_k) * (x_{t_{i+1}} - w_k) \leq 0 \tag{1}$$

If the level crossing l_i occurs, the quantized value of the time interval between two level crossings, $Q(l_i)$ and the amplitude

of level crossing which belongs to the level set W_k , $L(l_i)$. Following equations (2) and (3) shows the values to be recorded when a level crossing l_i occurs.

$$Q(l_i) = t(l_i) + t_s/2 \tag{2}$$

$$L(l_i) = W_k \tag{3}$$

When a sinusoidal input of amplitude 1mV and input frequency 110 Hz sampled at 100 KHz is given to the LC ADC framework, a level set of 15 levels (0.000125, 0.0025, 0.00375, 0.0005, 0.000625, 0.00075, 0.000875, -0.001, -0.000875, -0.00075, -0.000625, -0.0005, -0.00375, 0.0025, -0.000125) is generated. The signal is reconstructed using third order polynomial interpolation in MATLAB. An SNDR of 32.2763dB was achieved as shown in the FFT plot of LC ADC algorithm in Figure 6 for 1024 points.

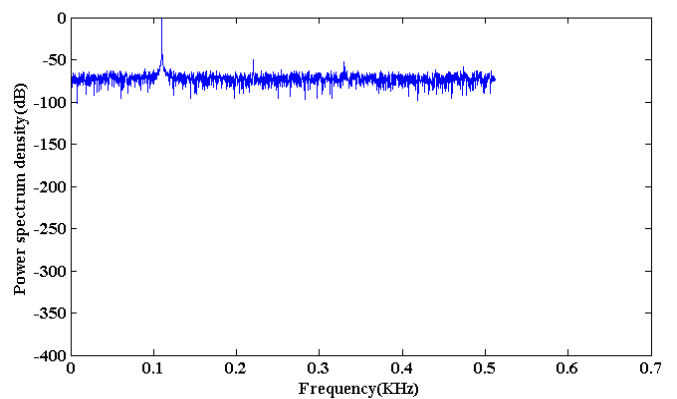


Figure 6. FFT plot of LC ADC for 1024 points

CONCLUSION

Based on historical data, various architectures of asynchronous ADCs are studied and performance trends are analyzed. LC ADC with feedback DAC and LC ADC with Flash ADC like architecture are studied in this paper. Performance trends of LC ADC such as figure of merit, resolution, power consumption, die area, supply voltage scaling, technological scaling are evaluated and compared with other asynchronous ADCs and synchronous ADCs. This paper also discusses suitability of asynchronous LC ADCs for wearable devices by evaluating the performance trends. The algorithm for a general framework of LC ADC is implemented using MATLAB.

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