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Hardware Implementation Issues of FPGA based Prototyping for Hysteresis Current Controlled Three Phase PWM Rectifier

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Abstract

Nowadays Field Programmable Gate Arrays (FPGA) are considered as one of the most advanced and efficient hardware solution to implement control algorithms for power electronic converters. The main features that makes the FPGAs superior to other technologies like microcontrollers or DSPs are its high-end parallel processing capabilities, reconfigurable hardware, high computational speed and low cost. This paper addresses the control algorithm and hardware design issues related to FPGA based laboratory prototype of three-phase Pulse Width Modulated (PWM) Rectifier. The hardware implementation details including the signal sensing and conditioning, integration of ADC with FPGA and the design of H-bridge with its drive circuits are discussed. Hysteresis current control is used to generate the gating signals for the converter where as a PI controller regulates the dc output voltage. The paper also explains a simplified algorithm used in this work to implement the PI controller with FPGA. Extensive simulation is done in MATLAB/SIMULINK and experimental verification is done using a laboratory prototype. The results obtained from the simulation and experimental results are analyzed to validate the concept.

Keywords: PWM Rectifier, Hysteresis Current Control, FPGA, PI controller algorithm, hardware.

INTRODUCTION

AC to DC power conversion is a widely used power conversion method in industry as well as at the customer end. Nowadays most of the high power conventional diode rectifiers used for AC to DC power conversion has been replaced by Pulse Width Modulated Rectifiers (PWM Rectifier) to meet the power quality requirements imposed by the existing standards. A desirable property of such converters is the ability to control power flow in either direction. Another property is the high power factor and low THD that can be attainable. Due to these features, PWM rectifiers are used in uninterruptable power supplies, battery chargers, power supplies for consumer goods and front end converters of variable speed drives.

Depending on the nature of the input, the PWM rectifiers can be broadly classified as Voltage Source Rectifiers (VSR) and Current Source Rectifiers (CSR). Similarly, based on the control parameter, the PWM rectifiers may be voltage controlled or current controlled and latter have superior performance in terms of dynamic response and quality of waveforms [1]. The control circuit of the PWM rectifier has to ensure unity power factor and regulated DC output voltage with low ripple [2]-[3]. This paper considers a three phase voltage-source current-controlled PWM rectifier for simulation and hardware implementation. Among the various current control schemes, hysteresis current control scheme is considered in this work because of its simplicity and good dynamic performance [4].

The conventional approach to realize hysteresis current control is by using discrete components and analogue integrated circuits (ICs). As the design of the control circuit is application specific, any modification of the control algorithm would result in the reconstruction of the hardware setup, which is time consuming and costly. Such circuits have some advantages such as better accuracy and higher bandwidth but they suffer from poor reliability and adaptability due to some of the operational issues like component parameter drift with temperature, age and transient stresses [5].

An alternate method to implement current hysteresis controller is by embedding the control algorithm in a microcontroller or digital signal processor (DSP) [6]-[7]. Such control algorithms requires simultaneously sampled and digitized phase voltages and currents to generate the switching pulses. Many of the low cost microcontrollers have multiplexed analogue channels and each channel is sequentially sampled and converted using a single ADC module. Advanced DSPs supports simultaneous sampling and errors due to sequential sampling can be reduced to an extent. But a microcontroller or DSP executes the control program in a sequential manner and it results in delayed switching pulses and poor quality of waveforms. To overcome this, DSPs may be replaced by field-programmable gate arrays (FPGA) which supports parallel execution of the control algorithm and results closer to analogue implementation can be achieved [8]-[9]. Usually FPGAs does not have inbuilt ADCs

and it is the choice of the designer to use high speed external ADCs. Fully configurable I/O lines of the FPGA permits high speed data transfer and multiple serial ADCs may be used to reduce the complexity of the printed circuit board. Simultaneous sampling, high speed data transfer and parallel execution of the hysteresis control algorithm results in accurate tracking of the reference currents.

The performance of FPGA based implementation of power electronic controllers is found to be excellent, but the hardware design and implementation issues are not reported in detail [10]-[12]. The focus of this paper is to have a detailed discussion on the implementation aspects of FPGA based ac/dc bidirectional converter. The experimental setup consists of a three-phase grid simulator constructed using a three phase VSI, LC filters and 24 V rechargeable lead acid batteries (explained in Section II B). The output of the grid simulator is connected to the laboratory prototype developed for the concept verification of hysteresis current controlled three phase PWM rectifier. Since the three-phase grid is derived from a 24V battery source, low voltage power MOSFETS may be used for the construction of the VSI and PWM rectifier. Such an experimental setup is compact, free from electric shock hazards and provides a portable platform for the concept verification of the control algorithm. Since the grid is simulated using a VSI, various conditions like grid voltage unbalance, frequency variations, sag or swell can be easily realized. This hardware setup is also useful for the control algorithm verification for systems like DSTATCOM and grid connected inverters.

BASIC BUILDING BLOCKS OF THE SYSTEM

The main functional blocks of experimental setup are shown in figure 1. They are

1. PWM rectifier
2. Grid simulator
3. Voltage and current sensing circuits
4. Spartan6 FPGA based controller

PWM Rectifier

The PWM Rectifier comprises of VSI built with 49A, 55V MOSFETs as shown in figure 2.The input three phase ac supply for the PWM rectifier is provided from the three phase grid simulator. The design of the PWM rectifier is done for a power rating of 24 Watts in order to make it suitable for low power laboratory prototyping. The set up is tested with a resistive load.

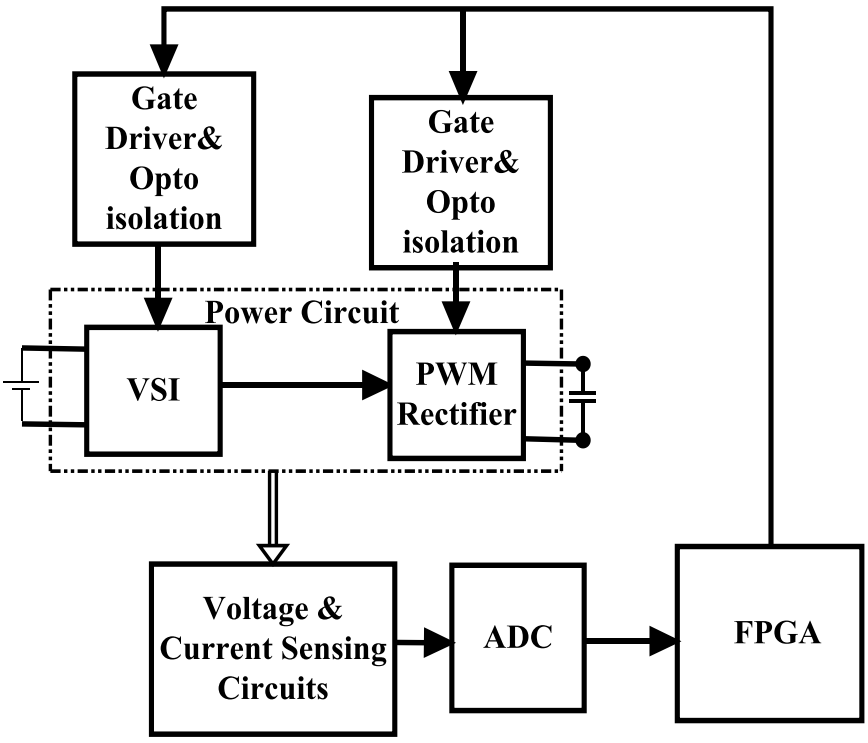

Figure 1. Functional Blocks of Experimental Setup

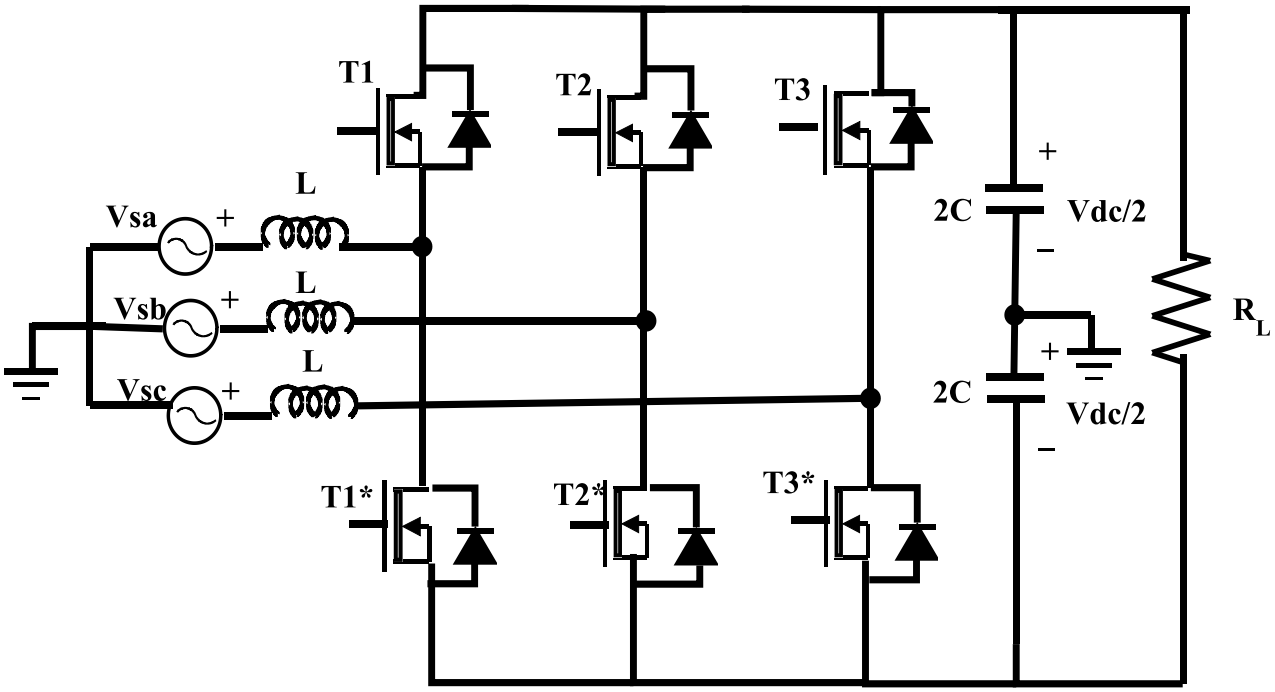

Figure 2. Three Phase PWM Rectifier

1) Design of DC link voltage

The average dc output voltage obtained from a three phase full bridge diode rectifier is given as [13].

$$V_d = \frac{3\sqrt{2}}{\pi} V_{LL} \quad (1)$$

Where V_d is the average dc output voltage and V_{LL} corresponds to the rms value of line to line input voltage. It can also be expressed in terms of the peak value of input phase voltage as

$$V_d = \frac{3\sqrt{3}}{\pi} V_m = 1.65 V_m \quad (2)$$

where V_m is the peak value of input phase voltage.

For the operation of the boost rectifier and to have a better current control for the PWM rectifier, the dc link voltage is taken as greater than the average dc output given by (2), and in this case is fixed at twice the peak of input phase voltage [14]. Therefore for an input voltage with peak of 12V, output dc link voltage is fixed at 24V.

II) Design of Input Inductance

The hysteresis current controller tracks the inductor current to stay within the reference value and the specified hysteresis band as the tolerance. The instantaneous switching frequency varies over a fundamental cycle and the maximum switching frequency (f_{max}) occurs at zero crossing point of the source voltage. The inductor should be designed in such a way as to limit this switching frequency[15].The per phase voltage equation of the PWM rectifier (Figure 2) with lower switch turned ON can be expressed as

$$v_s(t) - L_f \frac{di}{dt} + \frac{V_{dc}}{2} = 0 \quad (3)$$

From (3), corresponding to the zero instant of source voltage and with $V_{dc} = 2V_m$, the value of inductance can be obtained as

$$L_f = \frac{0.5 V_m}{h_b f_{\max}} \quad (4)$$

Where V_m denotes the maximum voltage and h_b corresponds to the hysteresis band in amperes. With a hysteresis band of 0.1A, and with maximum switching frequency of 10kHz, input inductance is obtained as 6mH.The inductance is designed to carry a rated current of 2A to meet with the PWM rectifier power demand.

III) Design of DC link capacitance

The DC link voltage may change during the transients in load demand or due to fluctuations in grid voltage. The rectifier needs to modify the real power exchange during these transients to meet the load demand and to maintain balanced three phase grid currents. This transfer of real power will result in the deviation of capacitor voltage from its reference value. DC link capacitance is designed based on the allowed dc bus voltage change during transients. Consider the voltage controller takes p cycles to restore any change, that is, pT seconds to act, where T is the time period of grid supply. Then the maximum energy exchange by the rectifier during

transient will be pST, where S is the Volt Ampere demand. This energy will be equal to the change in the capacitor stored energy [15]. Therefore

$$\frac{1}{2}C_{dc}(V_{dcref}^2 - V_{dc}^2) = pST \qquad (5)$$

For S=24VA, T=20msec, p=2cycles, Vdc_{ref} =24V, and

Vdc=0.8* Vdc_{ref}, the capacitance value is obtained as 10mF and the same is employed in this set up.

IV) Opto Isolated Driver

Spartan6 FPGA is chosen to implement the controller part for the PWM rectifier. The voltage level of the general purpose I/O (GPIO) lines of the FPGA is rated for 3.3V.Also the GPIO lines of FPGA can support a current of 7mA per pin and a maximum of 100mA per bank. The MOSFET selected for the hardware set up is IRF Z44N, which has a nominal range of gate to source voltage of 10 to 20V for turn ON. The suitable driver for this MOSFET is selected as TLP 250[16]. The recommended input current for TLP250 is 8mA. Hence to make the GPIO lines compatible with the TLP250, a current driver ULN2803A is used which has a maximum output current of 500mA[17]. The supply voltage range of TLP 250 is 15 to 20V.In this case, it is fixed at 16V, considering the MOSFET gate voltage requirements also. A decoupling capacitor of 0.1µF is connected across power supply lines to reduce loop area for the current path during MOSFET turn ON and thus improves the transient turn ON behavior. Figure 3 shows the schematic of the driver chips. The gate resistance Rg can be designed as

$$R_g = \frac{Supply\ voltage}{Output\ Current\ of\ TLP\ 250} \qquad (6)$$

Hence a 10Ω resistor is selected for this purpose for a supply voltage of 16V.

The three phase PWM rectifier is implemented with three half bridges. Each half bridge consists of two MOSFETs in series. Isolated MOSFET drivers are used for the upper and lower switches. These drivers are fed with isolated dc supply. One of the simple methods to provide this isolated power supply is by bootstrap technique. Even though the bootstrap technique is very simple and efficient, it suffers from the drawback of restriction on duty cycle range. Hence the isolated power supply is implemented with multiple output isolated dc to dc converters as shown in figure 4.

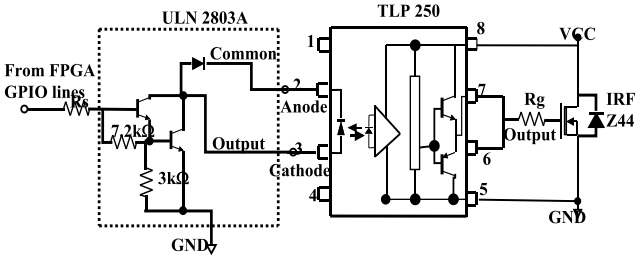

Figure 3. Opto isolated driver

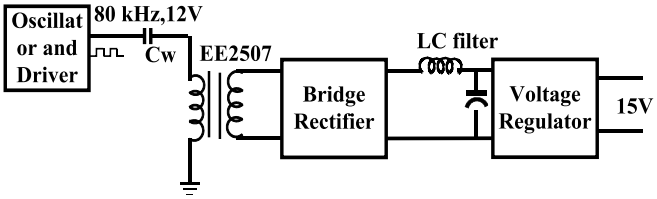

Figure 4. Isolated power Supply for Driver Circuit

Grid Simulator

The grid simulator is implemented with a three phase VSI using 49A,55V MOSFETS. The input for this grid simulator is from a 24V, 7Ah lead acid battery in order to support bidirectional power flow. The inverter is open loop controlled using sine triangle modulation. The gate pulses for the simulator as well as the PWM Rectifier are provided from the GPIO lines of the same FPGA. The internal up down counters of the FPGA are used to generate the triangular carrier wave of 12.5 kHz. The modulating sine wave is implemented with a look up table using 1024 locations of block RAM. The output of the sine wave inverter is filtered with LC filter to generate the fundamental sine wave of 50Hz and with a phase amplitude of 12V(peak).

Voltage and current sensing Circuits

I) Grid voltage sensing using Potential Transformer

Potential transformers (PT) with a voltage ratio of 24/6 are used to sense the three phase grid voltages. The Analog to Digital Converter (ADC) chosen here is AD7276, with an input voltage range of 0 to 3.3V.Hence the bipolar voltage of the transformer output is filtered and level shifted to the range of 0 to 3.3V in order to make the signal suitable with ADC input.

Grid Current Sensing

For grid current sensing, Hall Effect current sensor ACS725 having SOIC package is selected. This is a low cost current sensor with less PCB area and assures sufficient accuracy for this application. The input current range for this sensor is ±20A and the corresponding sensitivity is 64mV/A. The voltage corresponding to zero current is 1.65V when fed with a 3.3V power supply [18]. An external capacitor C_F is used to set the bandwidth and a 120kHz bandwidth is chosen for this application (figure.5).

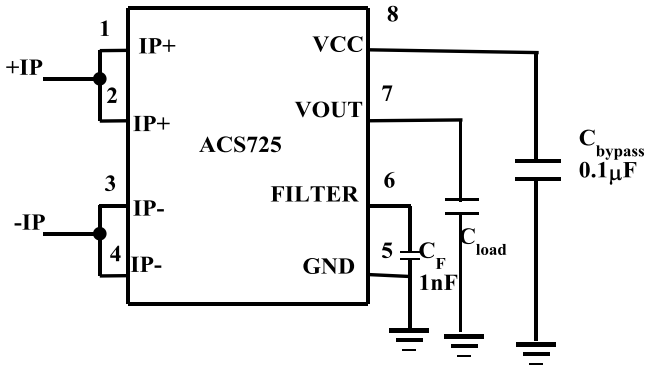

Figure 5. Circuit Arrangement of ACS 725

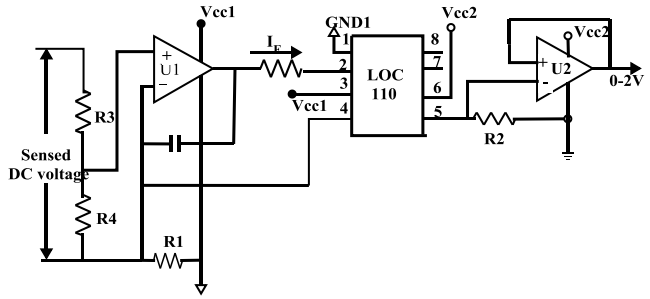

Figure 6. Configuration of LOC 110 for DC bus voltage sensing

DC Link Voltage Sensing

A linear isolation amplifier LOC110 is configured to provide dc bus signal isolation which consists of an infrared LED coupled to two phototransistors. One of the phototransistors provides isolation of output circuit from the input. The second phototransistor acts as a servo feedback mechanism to compensate for the non linear time and temperature characteristics of LED [19]. The circuit arrangement is as shown in figure 6. Two isolated power supplies of 5V and 12V are needed for this configuration. The 5V supply is derived from the main dc supply for the FPGA board and the 12V power supply is provided by PDS S5-S12, a dc to dc converter IC which converts from 5V to 12V[20].

Design of Isolation Amplifier for DC bus voltage Sensing

The design is done for an expected value of dc bus voltage of 50V.The value of resistors R3 and R4 of the voltage divider network can be calculated as

$$V_{IN}=V_{dc(max)}*R_4/(R_3+R_4) \quad (7)$$

V_{IN} can be maximum up to 2V for this IC. Hence select R3=23KΩ and R4=1KΩ.

From the datasheet, we obtain

$$K_1=\frac{I_1}{I_f}=\frac{\text{Servophoto Current}}{\text{Forward Current}} \quad (8)$$

Taking K_1=0.004 and K_2=0.004 for I_f=15mA (max)

From the circuit

$$V_{IN}=I_1*R_1 \quad (9)$$

$$and\ I_1=K_1*I_f \quad (10)$$

$$\text{We get} \quad R_1=\frac{V_{IN}}{K_1*I_f} \quad (11)$$

For V_{IN}=2V, we get R_1=33.3KΩ

Similarly for the output side we can write

$$V_{OUT}=I_2*R_2 \text{ and} \quad (12)$$

$$I_2=K_2*I_2 \quad (13)$$

$$\text{Thus,} \quad R_2=\frac{V_{OUT}}{K_2*I_f} \quad (14)$$

So for a V_{OUT} = 2V, we get R_2=33.3KΩ.

From (11) and (14), we can find

$$V_{OUT}=V_{IN}*\frac{R_2}{R_1} \quad (15)$$

Equation (15) shows that the output varies linearly with the input voltage in the entire operation range.

Analog to Digital Converters (ADC)

The FPGA does not provide integrated ADC and hence proper ADC has to be selected to meet the requirements of the system. In this work, separate ADC is used for each measured signal in order to do simultaneous sampling of all the analog channels and to assure same delay for all the digital inputs. For the proper functioning of hysteresis controller, the ADC sampling period can be a crucial factor. The bandwidth of the current sensors used here is 120 kHz and ten times sampling speed is selected for the ADC in order to have a better reconstruction of the digital signal. All the signals are processed with 12 bit accuracy and hence a 12 bit ADC would be preferred. Now the 12 lines from each ADC when connected to FPGA I/O lines would require about 84 I/O lines for connection, as there are 7 ADC channels in this case. At the same time if ADC with Serial Peripheral Interface (SPI) bus is chosen, only 12 lines are sufficient while maintaining same sampling rate. Thus minimum FPGA resources are utilized and the PCB size can also be reduced. Hence a successive approximation analog to digital converter AD7276 is chosen for this work. It has a 12 bit resolution with a sampling speed up to 3MSPS.The analog input range for this part is 0 to 3.3V and the conversion rate is determined by the clock [21]. The clock (SCLK) and chip select (CS) signals are common for all the ADCs. Hence simultaneous sampling is done for all the ADC channels and the digital outputs are available from 2nd to 14th clock pulse durations.

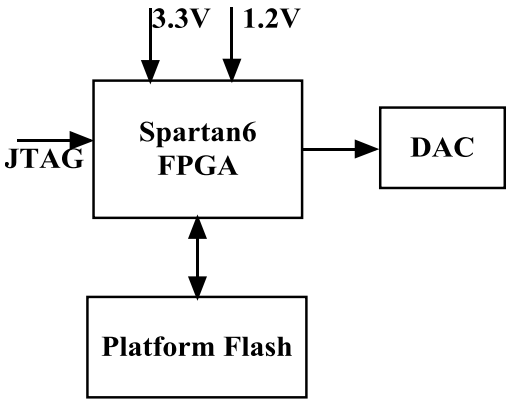

Figure 7. Parts of Spartan 6 FPGA Platform

Spartan6 FPGA based controller

Essential hardware parts of Spartan6 FPGA platform are as shown in figure 7.It is provided with 3.3 V regulated supply for I/O lines and 1.2 V for core of FPGA.JTAG connectivity and platform Flash memory is also arranged on the same board. It also has a 50MHz oscillator to provide system clock. The FPGA board is a four layer printed circuit board for good signal integrity. The top and bottom layers are used for signal routing where as the first layer is ground plane and second layer is power plane. Power supply decoupling capacitors are inbuilt for core and I/O section. During the testing of the hardware setup, it is essential to monitor internal variables. Hence a 12bit, high accuracy, DAC (LTC2630) with a full scale output of 2.5V is used for this purpose.

Control of three phase PWM Rectifier

As far as the operation of PWM rectifier is concerned, the main control parameters considered are

1) DC output voltage.
2) Input power factor.
3) Input current harmonic distortion.

To achieve these, an outer loop voltage controller and an inner loop current controller are used as shown in figure 8. A PI controller is used for the outer loop voltage control and hysteresis controller for the inner loop current control. The maximum value of the grid current per phase (I_m^*) is determined by the steady state output of the PI controller. The Phase Locked Loop (PLL) is used to track the grid voltage and a unit sinusoidal vector in phase with the phase voltage is derived from the PLL. Thus the instantaneous reference current is obtained by multiplying the unit vector from PLL with I_m^* (Maximum value of grid current). The function of the hysteresis controller is to generate proper switching pulses in such a way that the actual current follows the reference current. In this work the grid is simulated and the Sine PWM controller is implemented with Verilog program in the FPGA. Hence the PLL is not essential here to determine the angular position of grid voltage signal, instead it can be obtained from the reference sine wave of the PWM controller. It is to be noted that the PLL is essential in an actual system. The implementation of the PI controller and the hysteresis controller using FPGA is explained in Section.4 and 5.

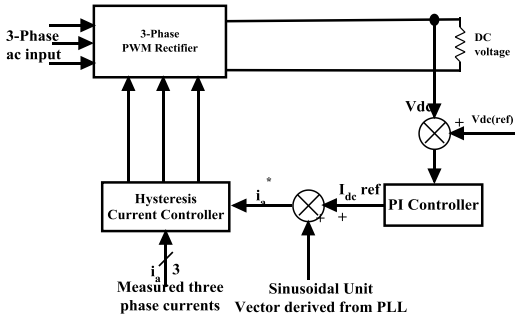

Figure 8. Controller for PWM Rectifier

Implementation of the PI Controller

The primary function of the PI controller is to regulate the dc output voltage irrespective of changes in grid voltage or load current. The PWM rectifier under unity power factor condition draws active current component (with maximum value I_m^*) from the source to regulate the dc bus voltage and to meet its losses in the rectifier. The error in dc bus voltage can be expressed as

$$\Delta V = V_{dc}^* - V_{dc} \tag{16}$$

This error is passed through a PI controller and its steady state output is taken as the maximum value of per phase grid current I_m^*.

$$I_m^* = k_1 \Delta V + k_2 \int \Delta V dt \tag{17}$$

where k_1 and k_2 are proportional and integral constants respectively.

The output of the PI controller is limited to vary between $\pm I_{sat}$, where I_{sat} is the maximum grid current that the rectifier is expected to draw in the worst case. A positive output from the PI controller shows the power flow from AC source to DC where as a negative value corresponds to a reverse power flow i.e from DC to AC.

Design of Proportional and Integral Constants

The output side of the PWM rectifier comprising the RC circuit can be modeled as shown in figure 9.

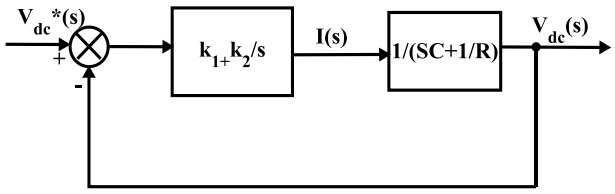

Figure 9. PI controller for dc voltage regulation

Closed loop transfer function is given by

$$\frac{V_{dc}(s)}{V_{dc}^{*}(s)} = \frac{k_1 R(s+\frac{k_2}{k_1})}{(s^2+2\xi\omega_n s+\omega_n{}^2)} \qquad (18)$$

Where $k_1 = 2\xi\omega_n C - 1/R$ and $k_2 = \omega_n{}^2 C$

k_1,k_2 corresponds to proportional and integral constants respectively, ξ is the damping factor (taken as 0.7) and ω_n is the natural frequency of oscillation (taken as 100 rad/sec).

Algorithm for Implementation of PI Controller in FPGA

The following are the steps for PI Controller implementation using FPGA.

1) The entire system including the PI Controller with designed values of k_1 and k_2 is modeled in MATLAB/SIMULINK and fine tuning of the controller parameters are done to obtain the desired performance.
2) With the fine tuned values of k_1 and k_2, the PI controller alone is simulated in open loop with a step input. The response obtained consists of a step change followed by a linear increase corresponds to the proportional gain and the integral part respectively. This response is treated as the reference. The step inputs and corresponding open loop response obtained from simulation is shown in figure 10.
3) To embed the same response in hardware, the block diagram shown in figure 11 is used to implement the PI controller with FPGA. All the variables used for the PI controller implementation are realized with 12 bit fixed point number system. Here the integrator is implemented as add and accumulate register with 24 bits to maintain enough accuracy.
4) The PI controller part in FPGA is tested in open loop with the same step input as given for the simulation.
5) The output can be observed with DAC and the controller parameters k_1 and k_2 are adjusted to obtain the same response as the reference.
6) The closed loop system incorporates this PI controller with the tuned parameters can provide the desired performance as obtained during simulation.

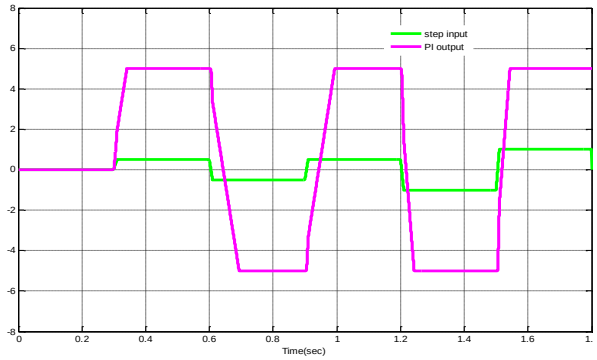

Figure 10. PI response Obtained from Simulation

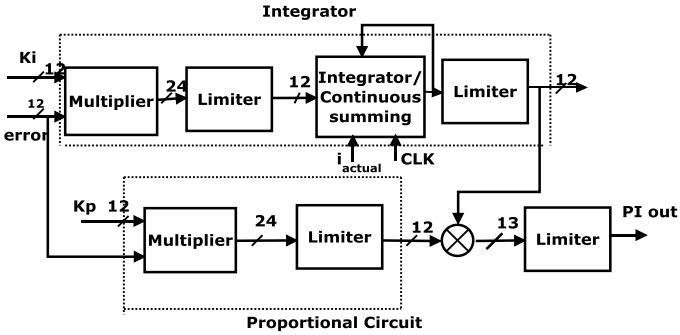

Figure 11. Logical Implementation of PI Controller with FPGA

Implementation of Hysteresis Controller

The function of the hysteresis controller is to make the actual current to follow the reference current by proper switching in each phase. The states of the switches can be controlled depending on the instantaneous values of reference and actual phase currents (the marked direction of current is taken positive as in fig.2) as given below.

$if\ i_a > i_a^* + HB$ then upper switch is turned ON and

$if\ i_a < i_a^* - HB$ then lower switch is turned ON.

The block diagram to implement the hysteresis controller in FPGA is as shown in figure 12. Here also both the actual current and reference current are represented with 12 bit fixed point number system. In order to avoid cross conduction, dead time is essential in a half bridge configuration. The value of dead time depends on the device property. Generally MOSFETs require less dead time than IGBTs due to its high speed operation. Here IRFZ44N is used to realize the half bridges and its rise time and fall time are specified as 60ns and 45ns respectively. Hence a dead time of 150ns would be enough to maintain proper switching. In this case, the dead time is also implemented in FPGA.A counter is programmed to introduce required dead time as shown in figure 13. When the input pulse is at its low state, the counter output is maintained low. Whenever the input is high, the counter starts to count up till the maximum count (which is decided by the required dead time) is reached. Once the counter reaches the

maximum count value, its output is made high and is maintained high till the input goes to low state.

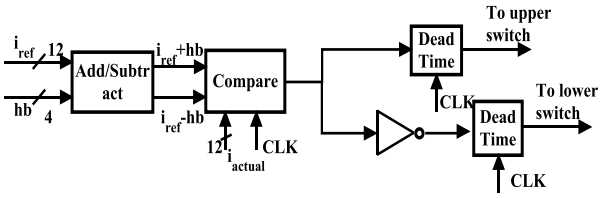

Figure 12. Logical Implementation of Hysteresis Controller

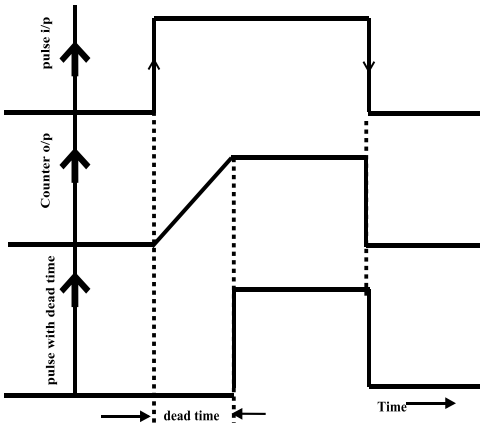

Figure 13. Realization of Dead time

SIMULATION RESULTS

The analysis of the system is done with MATLAB/SIMULINK model of a three phase PWM Rectifier. The system under consideration operating with a three phase 12V(per phase peak voltage) supply and with a dc link reference value of 24V.Figure 14 shows the dc link voltage regulation as the load current changes from full load to half load to value(from 1A to 0.5A). It can be seen that the dc link voltage is able to restore to the reference value within one cycle of input supply, after a small dip in voltage when the load current changes at t=0.3sec.Figure also depicts the grid current variation to such a load change. Figure 15 represents the grid voltage (phase value) and grid current waveforms. It can be noted that the voltage and current are in phase provides near unity power factor. The fourier analysis of the grid current waveform is done with the help of GUI (Graphical User Interface) tool in MATLAB/SIMULINK. It can be observed from the results (figure 16) that the total harmonic distortion (THD) is 0.72% with a hysteresis band of 0.01A.

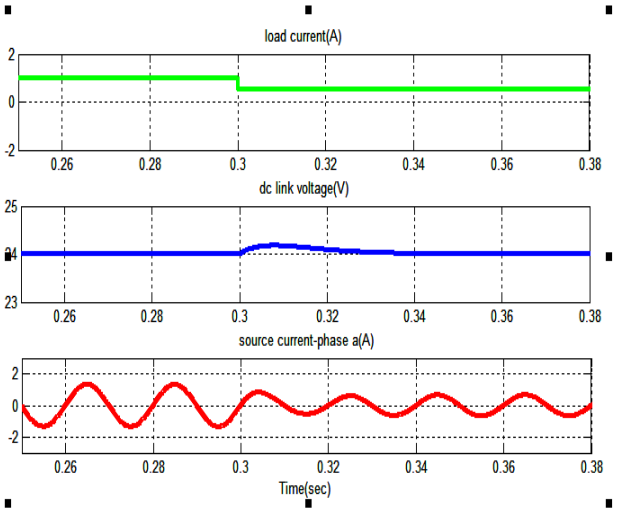

Figure 14. Dynamic response of DC output voltage and source current

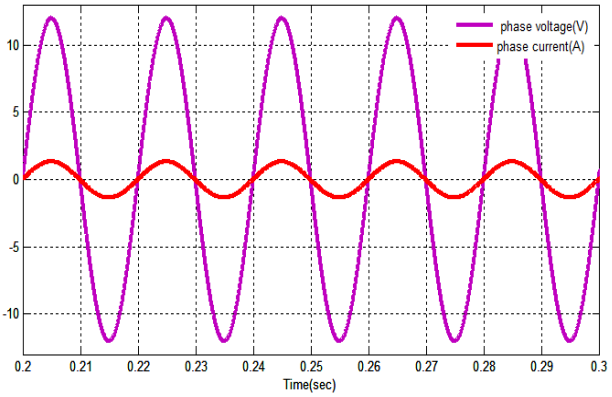

Figure 15. Source voltage and current waveform

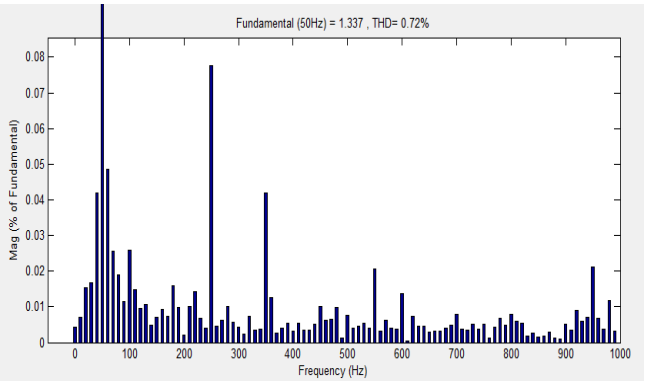

Figure 16. Fourier analysis of grid current waveform

HARDWARE RESULTS

The hardware set up is made for low power and the specifications of all the components used are as given in Table.1.All the voltage measurements are made using the DAC and current measurements with a current probe. Hence proper scaling factors are to be used with the measurements to get the actual magnitude.

The tracking of the dc bus voltage to a change in reference voltage is depicted in figure 17.Here the dc reference is made to change from 19V to 21V and it can be seen that the PI controller is capable of following the change in reference voltage with a very small delay. Figure 18 depicts the change in load voltage of the PWM rectifier where the load current changes from 1.2A to 0.6A while keeping the reference voltage at 21V.It can be noted that the load voltage is restored back to the reference after a small increase in voltage. From the waveforms of per phase grid current and voltage (figure 19), we can observe a near unity power factor at grid side. Actual measurements for grid voltage corresponds to 9V (peak value) and the grid current with 1A peak. The photograph of the hardware set up is also shown in figure 20.

Table 1. PWM Rectifier Specifications

Item	Specification
Input dc voltage	24V
Filter inductance (Inverter)	5mH
Filter Capacitance (Inverter)	22µF
Filter inductance (PWM Rectifier)	2mH
DC link Capacitor	10mF
Output dc voltage	24V

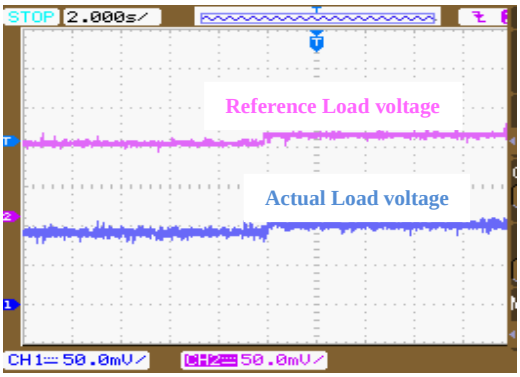

Figure 17. Response of dc link voltage for a reference change.

Figure 18. Response of dc link voltage for a load change.

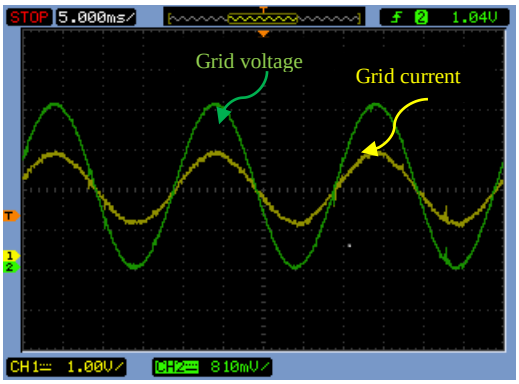

Figure 19. Source voltage and current waveform

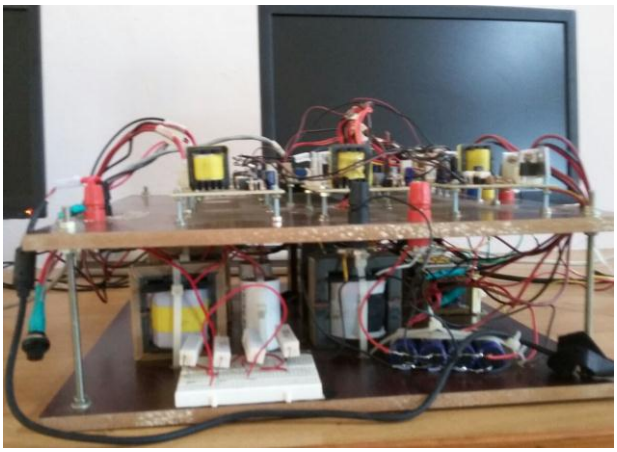

Figure 20. Photograph of the hardware set up

CONCLUSION

The design and implementation of FPGA based PWM rectifier has been explained in this paper. The proposed algorithm for PI controller has been found very effective and simple to implement. The hardware issues related with the low power laboratory prototype explained in this paper would benefit the academic community for experimental verification of the concepts.

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