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Design and Implementation of DSP based Interleaved Buck Converter fed PMBLDC motor Drive

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Abstract

BLDC motors has many advantages compared to brushed D.C motors like better torque speed characteristics, fast dynamic response, low noise, higher operations speed and higher efficiency. This article is on the development of a new converter which reduces the voltage stress of a buck converter being applied for BLDC drive. A Zero Current transition technique is implemented on the conventional Interleaved Buck Converter. A two winding coupled inductor is introduced to make the converter to operate in continuous conduction mode, thus lowering the current stress which occurs in discontinuous mode of operation. A TMS320C50 DSP processor is used to adjust the duty cycle at a fixed switching frequency. The proposed approach is validated by simulations in MATLAB and Prototype models.

Keywords: PMBLDC Motor Drive, Interleaved buck converter, TMS320C50 DSP processor, Voltage and current stress minimization

INTRODUCTION

Brushless DC (BLDC) motor drives invited the attention of electronics due to the improved power quality of which resulted in comprehensive good performance compared with other conventional drives. The BLDC motors are similar as that of synchronous motor having permanent magnet on the rotor and three phase winding on the stator [1]-[2]. In the absence of brushes and having the electronic commutation improve the performance and eliminates the problems like sparking, noise and electro-magnetic interference (EMI).

The BLDC motor has been progressively replacing the conventional DC drives in various applications such as electric vehicles and industrial automation. The advantages of motor with the absence of brushes are compact size, high efficiency, high power density, high ruggedness and low EMI problems [3]-[4]. These motors are highly useful in low and medium power applications in household appliance, medical instruments, air conditioning and transportation utilities.

A BLDC motor drive requires a 3-phase voltage source inverter (VSI) with constant DC link voltage for producing an electronic commutation [2]. An uncontrolled diode bridge rectifier (DBR) with high value of DC link capacitor fed from a single phase AC mains is used for maintaining the DC link voltage of the VSI for supplying the required energy to the BLDC motor. Such combination of DBR and DC link capacitor draws a peaky and highly distorted supply current from the AC mains which have more harmonics and total harmonic distortion (THD) of supply current as high as 60-80% [5]. Such supply current results in very low power factor of the order of 0.6-0.7 at the AC mains which is not acceptable under the limits of various international power quality standards such as IEC 61000-3-2 [6].

In order to minimize the effect of harmonics and to improve the performance of the BLDC Motor a proper control scheme has to be evolved. Many researchers have proposed various control schemes to minimize the harmonics and switching losses. The switching losses are reduced by using a concept of variable DC link voltage for speed control of BLDC motor [7]. The DC-DC converters have been suggested to reduce the switching losses and to attain high efficiency at increased frequencies [8]. In the case of resonant converters the voltage stress on power switches are subjected to very high voltage stress especially when these comments are used for high voltage applications [9]- [10].

Power factor correction (PFC) converters are proposed to achieve higher power in references [11-15]. A boost PFC converter is a widely adopts configuration for improving the power quality at AC mains of BLDC motor drives [13]. However, this configuration uses a high frequency pulse width modulation (PWM) pulses for controlling the speed of BLDC motor. Therefore, it has high switching losses associated with the VSI and requires two costly current sensors for PWM based current control of BLDC motor [13].

Many researchers have worked on ZVS and/or ZCS, so as to reduce the switching losses associated with the high-frequency switching. The objective is to reduce input current ripple, reverse recovery loss of the diode and to improve current sharing between the switches and overall efficiency. Nevertheless, fast soft switching, equal current sharing and high efficiency IBC design is still moving on a difficult task.

In this article, a TMS320C50 DSP processor based switching technique for interleaved buck converter (IBC) with zero current transition (OFF) and zero voltage transition (ON) are proposed. A two winding coupled inductor is introduced to make the converter to operate in continuous conduction mode, thus lowering the current stress which occurs in discontinuous mode of operation.

MATHEMATICAL MODEL OF BLDC MOTOR DRIVE SYSTEM

The study on the proposed interleaved converter has been done in the MATLAB platform by means of simulation and the development of prototype models. For the purpose of

simulation, a mathematical model is derived for a 3 phases, 4 poles, Y connected trapezoidal back-EMF type BLDC Motor. Trapezoidal back-EMF implies the mutual inductance between the stator and rotor by means of trapezoidal in shape. In order to simplify the equations involved the following assumptions are made,

1. Magnetic circuit saturation is ignored.
2. Stator resistance, self and mutual inductance of all phases are conisdered to be equal and constant.
3. Hysteresis and eddy current losses are eliminated. The semiconductor switches are ideal in nature.

The three phase voltage equations of BLDC Motor are as expressed as,

$$V_{as} = RI_a + L\frac{di_a}{dt} + e_a + V_{no} \quad (1)$$

$$V_{bs} = RI_b + L\frac{di_b}{dt} + e_b + V_{no} \quad (2)$$

$$V_{rs} = RI_c + L\frac{di_c}{dt} + e_c + V_{no} \quad (3)$$

Because of the interaction of the current in stator winding and the magnetic field from rotor magnets, an electromagnetic torque is produced and it can be expressed as

$$T_e = \frac{e_a i_a + e_b i_b + e_c i_c}{W_m} \quad (4)$$

Where, W_m is the mechanical speed of the rotor. Then the equation of motion is given by

$$\frac{dW_m}{dt} = \frac{T_e - T_l - BW_m}{J} \quad (5)$$

Where

T_L= Load torque in Nm,

B = Damping constant,

J=Moment of inertia of motor and load

For six- step motor control, at each step the instantaneous output power will be delivered from two phase in series, and is given by

$$P_0 = \omega_m T_e = 2V_{max} I_m \quad (6)$$

Where 'I' is the current amplitude and E is the induced Back EMF. From equations (4) and (6),the output torque can be also expressed as

$$T_e = 2K_t T_m \quad (7)$$

Where, K_t is the motor torque constant. The three phase voltage equations can be rewritten as,

$$0 = RI_a + L\frac{di_a}{dt} + e_a + V_{no} \quad (8)$$

$$V_{dc} = RI_b + L\frac{di_b}{dt} + e_b + V_{no} \quad (9)$$

$$0 = RI_c + L\frac{di_c}{dt} + e_c + V_{no} \quad (10)$$

$$V_{no} = \frac{1}{3}(V_{dc} - V_{max}) \quad (11)$$

$$T_e = \frac{e_a i_a + e_b i_b + e_c i_c}{W_m} = \frac{2I_m V_{max}}{W_m} \quad (12)$$

$$\frac{di_a}{dt} = \frac{V_{dc} + 2V_{max}}{3L_s} \quad (13)$$

$$\frac{di_b}{dt} = \frac{2(V_{dc} + 2V_{max})}{3L_s} \quad (14)$$

$$\frac{di_c}{dt} = \frac{(V_{dc} - 4V_{max})}{3L_s} \quad (15)$$

The time taken for i_a to from the initial value I_m is

$$t_1 = \frac{3L_s I_m}{V_{dc} + 2V_{max}} \quad (16)$$

The time taken for i_b to increase from 0 to I_m is

$$t_1 = \frac{3L_s I_m}{2(V_{dc} - V_{max})} \quad (17)$$

From the above equation, $i_a+i_b+i_c=0$, during commutation. Then the electromagnetic torque can be calculated as

$$T_e = \frac{2V_{max}}{W_m}\left(I_m + \left(\frac{V_{max} - 4V_{max}}{3L_s}\right)\right) \quad (18)$$

The relative torque ripple is given by

$$\Delta T_e = T_e - T_{e-pre}\left(\frac{V_{max} - 4V_{max}}{3L_s}\right)t \quad (19)$$

According Equation (7) and (14)-(18), the following conclusion can be drawn

1. If $V_{dc}>4V_{max}$, then $t_1>t_2$, and the torque keeps increasing during commutation.
2. If $V_{dc}<4V_{max}$, then $t_1<t_2$, and the torque keeps decreasing during commutation.
3. If $V_{dc}=4V_{max}$, then $t_1=t_2$, and the torque is constant during commutation.

PROPOSED BLDC DRIVE MODEL

The TMS320C50 DSP with its Analog Interface Chip provides a complete controller firmware for the converter design. The DSP board supports a graphical user interface that enables the user to navigate easily into program development process. The kit is interfaced with a standard PC through the serial communication port. The complete experimental layout is given in figure 1 and figure 2. The BLDC motor has a rotor with magnets and a stator made up of windings. In the absence of brushes, the commutation has been done by means of power electronics switches.

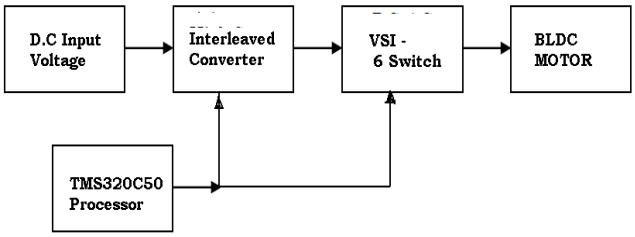

Figure 1. Proposed BLDC drive

Gate pulses are derived for 6-switch Inverter through current control technique. The torque ripple of BLDC motor drive is mainly depends on speed and phase current during commutation. Normally the commutation for 3 phase BLDC motor is performed by the six-step VSI, in which each phase voltage is energized for interval of 120 degree electrical based on the rotor (electrical) position. The DSP processor generates the gating pulses for the Interleaved Converter and six switch inverter.

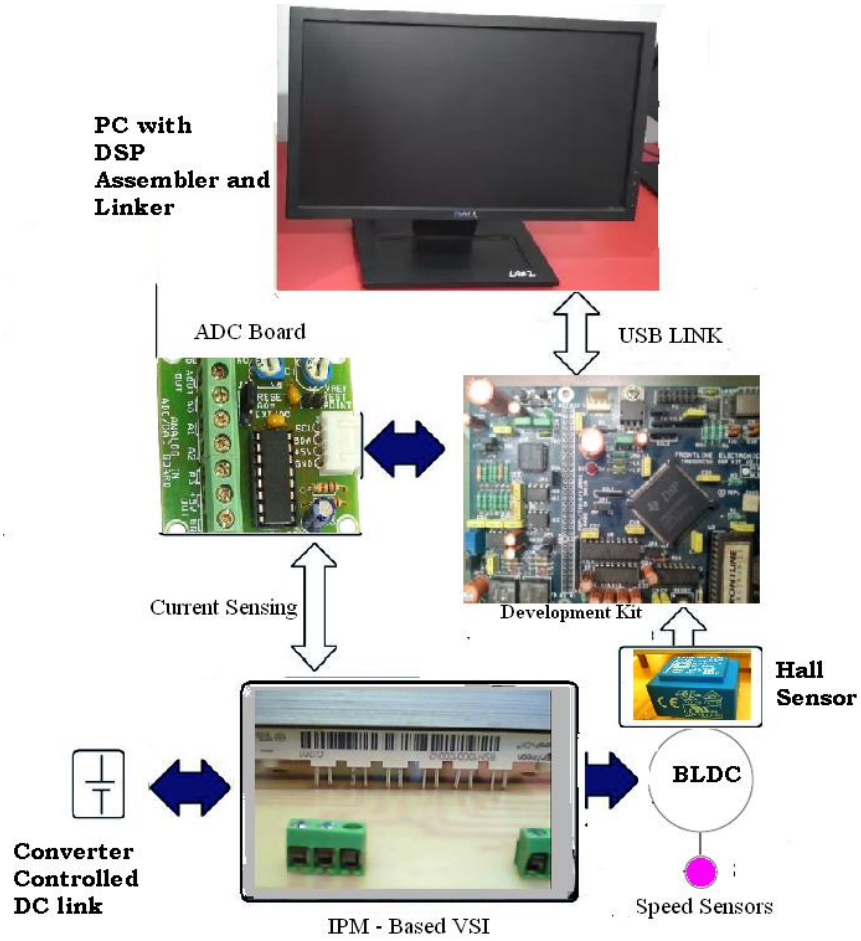

Figure 2. Experimental setup for Converter Fed Drive

In this paper, a new converter is proposed to achieve dc link voltage control and to keep phase current changing at the same rate during commutation. The specifications of PMBLDC Motor used in the investigation are given in Appendix Table-A1.

A. Hardware Implementation

Figure 1 shows the main DSP processor board used for the generation of gating pulses. The board supports interconnections like analog interface, and emulation interface. PC communication is achieved by the RS-232 port present in the same DSK board. The 32K bytes of PROM contain the kernel program for boot loading. This PROM portion is used only during booting and cannot be used thereafter. The TLC32040 AIC (Analog Interface Circuit) facilitates the connection between the DSP and the P.C. Two analogy connector provides by the same I.C. The Analogy In and Analogy Out pin are designed to be in the range of 0-3V. The AIC chip uses a 10MHZ master clock supplied by the C50. A gate driver IC with optical isolation is used to drive the VSI switches. Table 1 shows the different switching states of the VSI feeding the PMBLDC motor based on the Hall-effect position signals $H1$ to $H3$.

Table 1. Inverter switching states

Degree	Hall Effect Sensor			Switching State					
	H1	H2	H3	G1	G2	G3	G4	G5	G6
NA	0	0	0	0	0	0	0	0	0
0 - 60	0	0	1	1	0	0	0	0	1
60 -120	0	1	0	0	1	1	0	0	0
120 -180	0	1	1	1	0	1	0	0	1
180 - 240	1	0	0	0	0	0	1	1	0
240 - 300	1	0	1	1	0	0	1	0	0
300 - 360	1	1	0	0	1	0	0	1	0
NA	1	1	1	1	0	0	0	0	0

The PID controller algorithm was coded in the DSP processor and the program was written in assembly language. The assembler converts this assembly code into machine language objective files suitable for the C50 processor. The assembler also creates a listing file containing the list of errors which can be used for debugging. DSK Debugger is an interactive environment used to load the executable file into the DSP processor.

RESULTS AND DISCUSSION

The interleaved buck converter is tested with the given design parameters and observed that the simulation results are in line with the theoretical facts and are compared with the hardware results.

A. Performance of Converter with Resistive Load

The tuned constant for the PID controller were, Kp = 1.3, Ki = 5 and Kd = 0.03. The MATLAB model used in this study is presented in figure 3.

1. The following assumptions were made in developing the model.
2. Resistance of the Choke is neglected.
3. Output Capacitor Co is large enough to be assumed as a voltage source.
4. The Electrostatic resistance of the capacitor is neglected.
5. Switches are assumed to be ideal.

The results are also compared with that of the hardware results.

A PMBLDC motor used in practical application like washers, driers and compressors is subjected to varying loads and operates at different speed ranges. Therefore the designed converter is subjected to different load conditions and the output is shown in figure 4. It is observed that even when increasing the load current from 10A to 20A the output voltage level of the converter remains constant at 24 V D.C.

In order to show the reliability of the proposed method, another simulation also performed with reference voltage has been set at 23.5V DC. The experimental results are displayed in Fig. 5. In the study the input voltage of the converter is raised from 150V to 200V at time 0.005 Seconds. This change in input voltage does not affect the output voltage which is held constant at 23.5V.

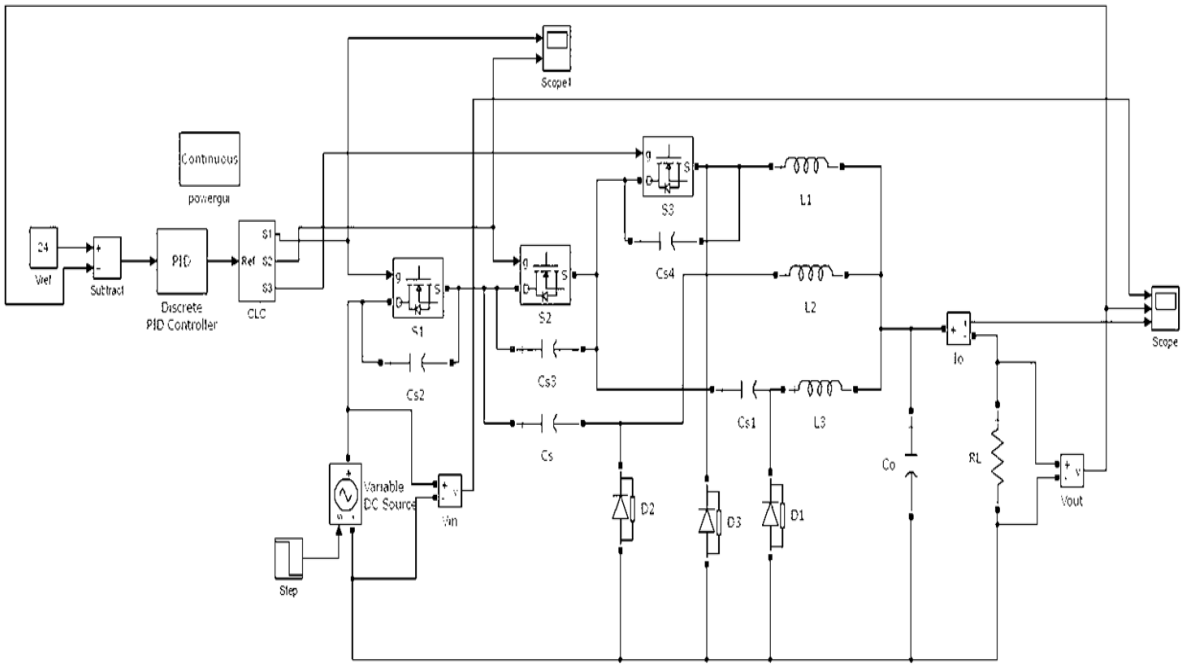

Figure 3. MATLAB Simulation Model with Resistive Load

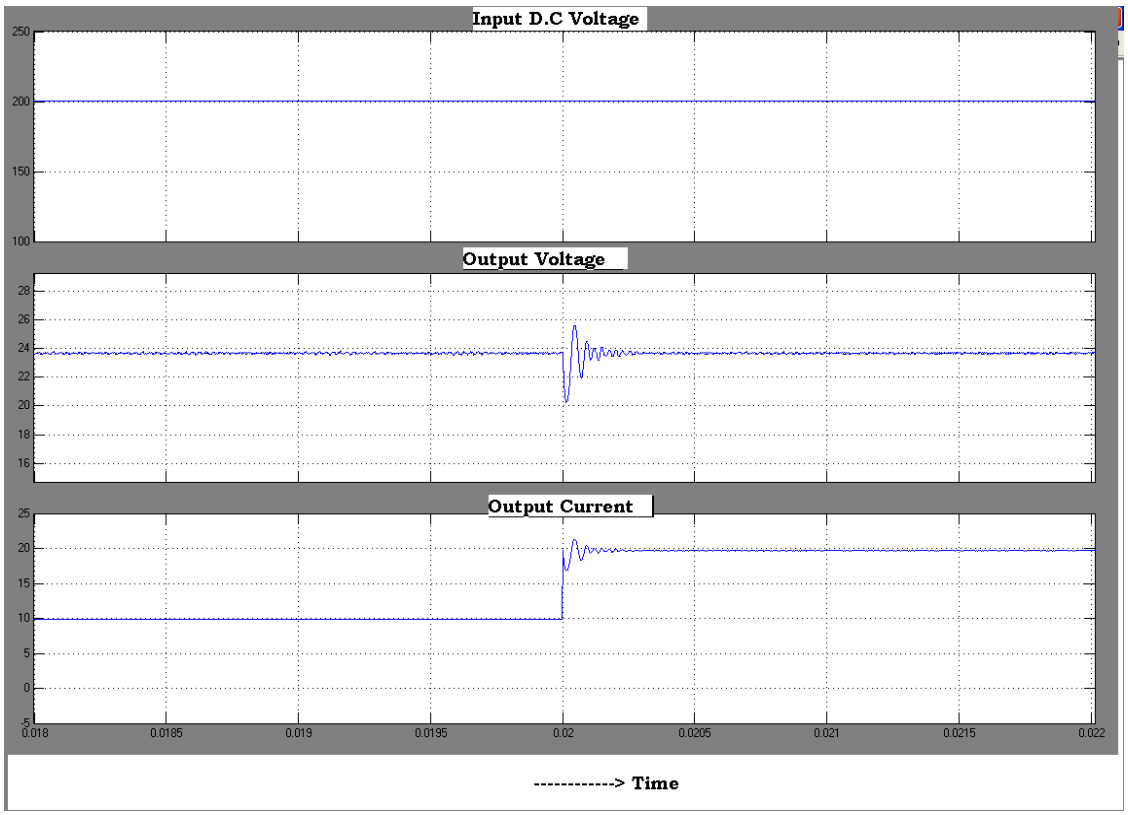

Figure 4. Converter Performance with change in load

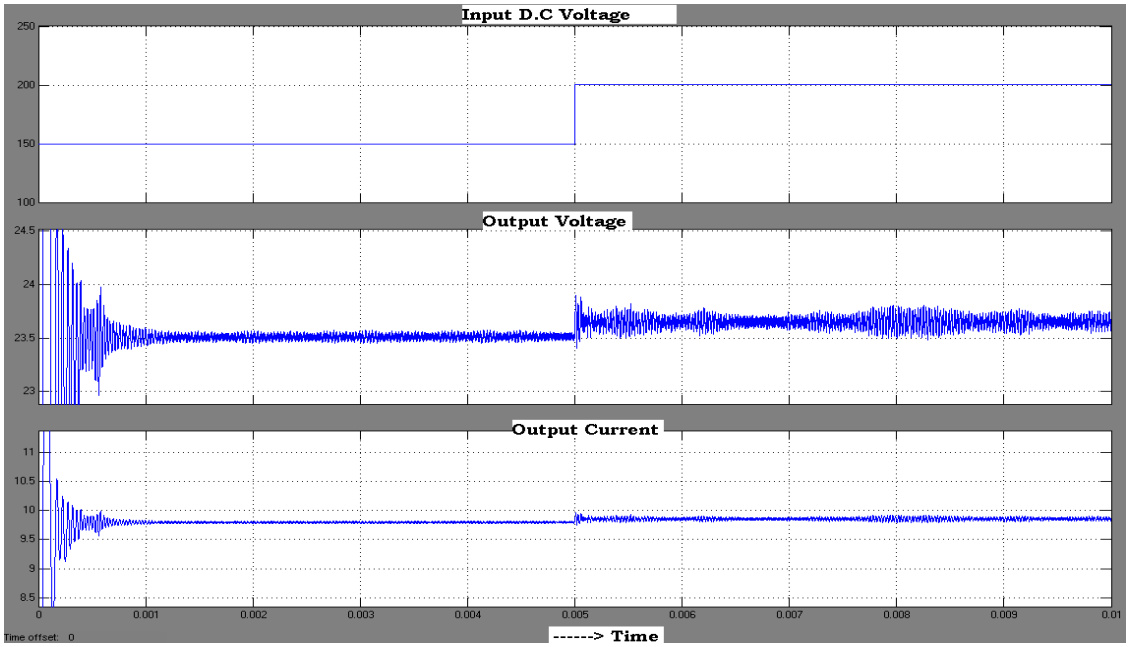

Figure 5. Converter Performance with step change in Input D.C Voltage

B. Performance of Converter with BLDC Motor

Simulation studies were carried out on the proposed converter fed to a PMBLDC drive. Three phase voltage of the PMBLDC motor for tunning at 1000rpm speed is presented in figure 6 and the corresponding current is shown figure 7. The motor pa

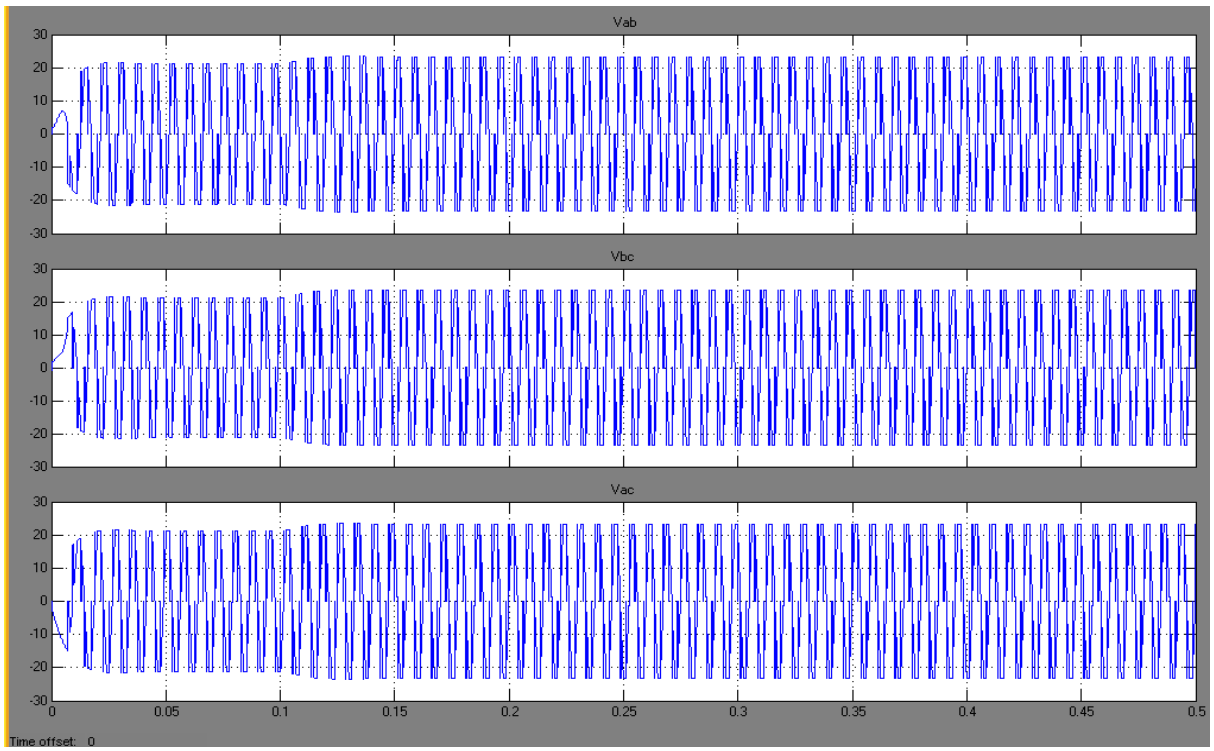

Figure 6. Three phase voltage feed to PMBLDC

At about 0.1 seconds the motor is loaded with a belt load setup and this causes the load current to reach 2.5 amps.

C. Efficiency under various load conditions

Efficiency of the converter is tested under different load conditions and the results are presented in table 2. It is observed that maximum efficiency occurs at 240 watts, i.e. at maximum load condition. During the full load condition the stored energy is used before the maximum storing capability is reached and the energy loss is low while driving heavy loads. From the results, it is seen that the proposed soft switching topology provides a maximum efficiency of 97.8%.

Table 2. Efficiency under varying load conditions

Load (W)	Efficiency (%)
20	94.1
40	94.8
80	95.1
120	95.7
160	96.4
200	96.8
240	97.8
280	97.3

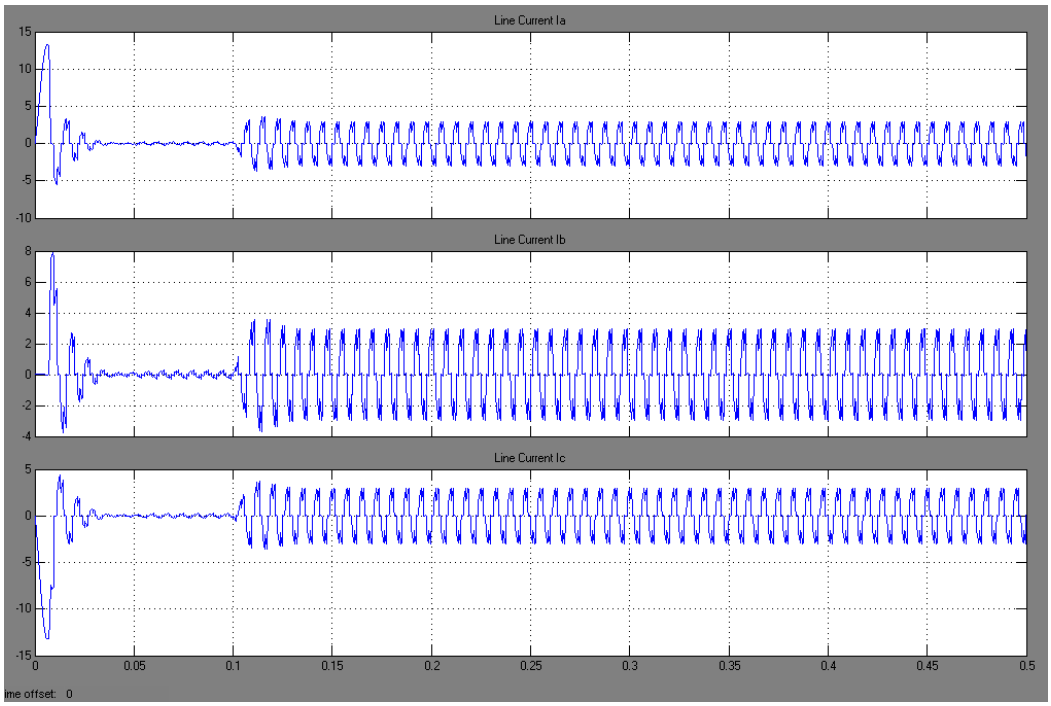

Figure 7. Three phase current feed to BLDC

D. Observation in this investigation.

1. The PCB tracks design for the IPM inverter were coated with Lead This ensures proper current low without any P.C.B track failures.
2. The IPM gating module is based on VLN504. This reduces design complexity and provides optical isolation. Surge protection is the built in feature of the VLN504 gate driver.
3. A gating module is applied with a negative 9V D.C supply during off time and this assures the proper turn-off IGBTS.
4. The voltage stress on the converter switches found to be lower compared to that of the output voltage.

CONCLUSION

PMBLDC drives finds have plenty of application in Process controls, machinery controls and conveyer categories. This article presents the design and implementation of BLDC motor drive using a low cost DSP processor. The performance of the proposed BLDC motor is evaluated over a wide range of speed and performed in MATLAB/Simulation environment. The simulation results across each element is presented. Specifically the ripples of phase current under various load currents are analyzed. The various steps involved in the implementation of the algorithm in a DSP processor are explained. The use of a high frequency MOSFET has lead to reduced switching losses. From the experimental outcome, it is obvious that low cost DSP processor can be used to have superior control performance in BLDC motors.

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APPENDIX

Table-A1. Parameters of BLDC Motor

Number of Poles	8
Voltage	24V
Current rated	2.18A
Output Power	52.5W
Speed	4000RPM
Rated Torque	1.25Kg-Cm
Phase to Phase Resistance	0.73