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Fractal Based Sigma Delta Modulation Scheme for Multilevel Inverter

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Abstract

This paper presents a novel vector quantization technique in Sigma Delta Modulation scheme for multilevel inverter which quantizes the instantaneous reference space vector directly by using a hexagonal quantizer with fractal features of space vector diagram of inverter in 60^0 coordinate system .The voronoi region for reference space vector in the proposed scheme is the triangle enclosing the reference space vector formed by its nearest three permissible switching states. The proposed scheme eliminates generation of impermissible switching states for n-level inverter compared to the existing direct space vector quantization technique in SDM. The proposed scheme is compared with existing direct vector quantization scheme in SDM for five-level and three-level inverter configurations and verified results are presented in this paper. The proposed scheme has better performance in terms of THD than the existing direct vector quantization technique in SDM. The proposed scheme is implemented to drive a 5hp open end winding induction motor for three-level configuration and the results are verified.

Keywords: Sigma Delta Modulator (SDM), Space vector, Direct vector quantization, Fractal structure

Abbreviations

ADC -Analog to Digital Converter, PWM -Pulse Width Modulation, RPWM -Random Pulse Width Modulation, RTI-Real Time Interface, SDM-Sigma Delta Modulation, STPWM -Sine Triangle Pulse Width Modulation, SVPWM- Space Vector Pulse Width Modulation, THD- Total Harmonic Distortion

INTRODUCTION

Multilevel inverter has better harmonic characteristics, lesser electromagnetic interferences and lesser voltage stress on switches than two level inverters. Multilevel inverters are used as an alternative for medium and high-power in industrial applications [1].The duty ratio of inverter switching signals are varied for attaining adjustable speed control drives. The commonly used modulation schemes for generating inverter switching signals for adjustable speed drives are STPWM and SVPWM. In STPWM the zero states of the inverter switching signal are not equally distributed [2] and hence a modified modulating signal is used which is obtained by injecting 20% of third harmonic to the sine wave [3]. Practically it is difficult to generate the modified modulating signal required in the STPWM. SVPWM gives better total harmonic distortion characteristics than STPWM and it is can be digitally implemented easily [4-5]. In SVPWM for multilevel inverter the locations and ON time of nearest three vectors of reference space vector are calculated using two-level modulation[6].The reference space vector of a multilevel inverter is mapped to two-level vector space in [7] to makes the computation of finding the nearest three vectors and ON time of these states easier.

The space vector diagram of any multilevel inverter has a fractal triangular structure. This fact is explored to get the three nearest space vectors of reference vector in SVPWM technique. At each triangularization the triangle is divided into four equilateral triangles [8-9].

For constant switching frequency PWM schemes the power spectrum is concentrated at the switching frequency and its harmonics and it produces acoustic noise, electromagnetic interference and torque pulsation [10]. In Random PWM (RPWM) the spectral energy is spread continuously [11]. The randomness is achieved by varying the slope of triangular carrier by frequency modulation in [12].

The switching signals for a multilevel inverter is considered as the output of an oversampling ADC and techniques used for generating the oversampling ADC are applied to generate the switching signals[13]. Sigma Delta Modulation (SDM) has randomly varying switching frequency and it spreads the spectrum. SDM are used to achieve higher resolution with lesser number of bits by spreading the quantization noise out of the signal band width. SDM is popularly used in oversampling ADC as it spreads the spectrum with reduced quantization noise [14].The switching signal for multilevel inverter is generated by mapping the multilevel space vector to two-level and applying SDM[15].For better computational efficiency the reference space vector is directly vector quantized [16-17].

The direct space vector quantizer in SDM quantizes the integrated error vector to the nearest vertex of parallelogram enclosing it [17]. At higher modulation index for n-level inverter the parallelogram enclosing the integrated error vector will have vertex formed by impermissible switching states of n-level inverter. It may results in quantizing the reference space vector to impermissible switching states. A hexagonal quantizer with fractal features of space vector diagram is proposed to directly vector quantize the reference space vector in SDM technique. For eliminating fractional arithmetic 60^0 coordinate system is used in the proposed scheme [18].

PRINCIPLE OF PROPOSED SCHEME

Fig.1 shows the block diagram of proposed SDM technique with hexagonal quantizer which has fractal features of space vector diagram. The reference space vectors V_a, V_b and V_c in 120^0 coordinate system is transformed to 60^0 coordinate system and it is normalized. The resolved normalized instantaneous reference space voltage vector (V_{ref}) along M axis and N axis are V_m and V_n respectively. Sigma delta modulation is applied each component of resolved instantaneous reference space voltage vector (V_{ref}). For first order SDM the difference between the actual value and quantized value is integrated and quantized to generate the sigma delta modulated signal [19].The input to the discrete time integrator is the difference between V_{ref} and the quantized space vector V_N (V_{Nm},V_{Nn}) and its output is the normalized integrated error vector $V_E(V_{Em}, V_{En})$ which is random in nature. $V_E(V_{Em}, V_{En})$ follows $V_{ref}(V_M, V_N)$. The space vector quantizer quantizes V_E to the nearest located space vector V_N (V_{Nm}, V_{Nn}) in the vector space diagram . In this scheme fractal triangularization is carried out in the sector of hexagonal quantizer in which the error vector lies to obtain the unit length triangle enclosing V_E .From the vertices of triangle determined, the vertex which is nearer to V_E is selected as the quantized space vector. The switching vector in 60^0 coordinate system is then converted to the inverter switching levels in three phases (S_a, S_b and S_c).

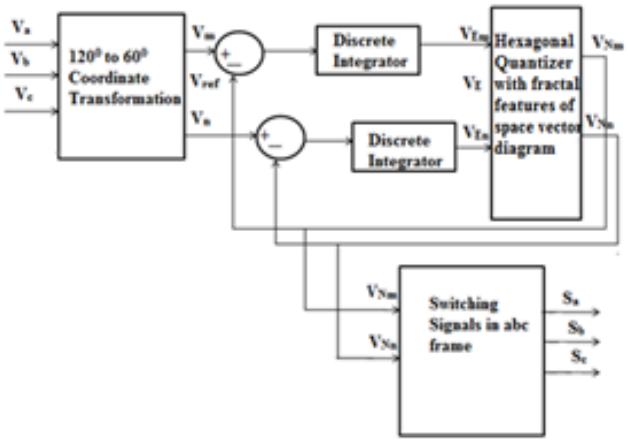


Figure 1. Block diagram of proposed fractal based SDM Scheme

Normalized Reference Space Vector in 60^0 Coordinate System

The three phase reference space voltage vectors V_a, V_b and V_c are normalized and are converted to 60^0 coordinate system V_{ref} (V_m,V_n). The reference space vector for an n-level inverter is normalized by multiplying it with $(n-1)/V_{dc}$, where V_{dc} is the dc voltage given to the inverter. In 60^0coordinate system the C-phase component is zero along M axis and A-phase component is zero along N axis. A-phase component and B-phase component are in phase and out of phase with M axis respectively. B-phase component and C-phase component are in phase and out of phase with N axis respectively [18].The normalized reference space vector V_{ref} (V_m,V_n) in 60^0 coordinate system can be expressed as

$$V_m = (V_a - V_b) * (n-1) \div V_{dc}(1)$$

$$V_n = (V_b - V_c) * (n-1) \div V_{dc}(2)$$

Fig.2. shows the normalized space vector diagram of five-level inverter in the 60^0 coordinate system. The coordinates of space vectors have integer values which makes the computation less complex.

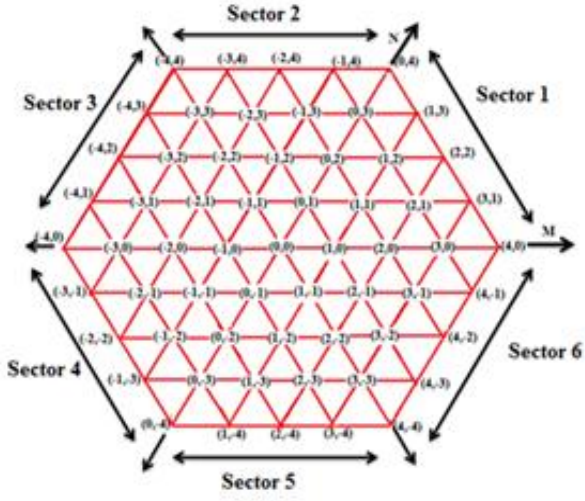


Figure 2. Normalized space vector diagram of five level inverter in 60^0 coordinate system

Proposed Space Vector Quantizer

The proposed space vector quantizer is a hexagonal quantizer with fractal features of space vector diagram. For n-level inverter the hexagonal quantizer has its boundary as that of the normalized space vector diagram of n-level inverter in the 60^0 coordinate system. Fig.3 shows the hexagonal quantizer for n-level inverter.

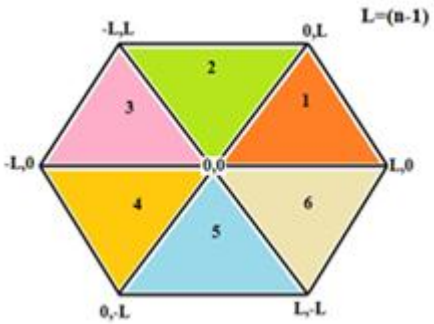


Figure 3. Hexagonal quantizer for n-level inverter.1-6 represents the sector.

The sector in which the error vector lies is identified and fractal triangularization is carried out in the identified sector to find the triangle enclosing the integrated error vector. Sector identification is carried out by selecting sector whose centroid is nearer to error vector. At each stage of triangulation the triangle is divided into four equilateral triangles by joining midpoints of vertexes similar to the

Sierpinski triangle. At each triangulation the vertices and centroid of the four newly formed triangles are determined .The triangle in which the integrated error vector lies among the four is determined by selecting the triangle which has minimum Euclidian distance between its centroid and integrated error vector. The triangularization is carried out till the triangle with unit length, enclosing the integrated error vector is determined. For a n-level inverter the hexagonal quantizer is of length n-1. Two to the power of number of iterations of triangularization gives the length of hexagonal quantizer. The number of iterations of triangularization required for n-level inverter to get triangle with unit length is given by equation

$$iteration = log_2(n-1) \qquad (3)$$

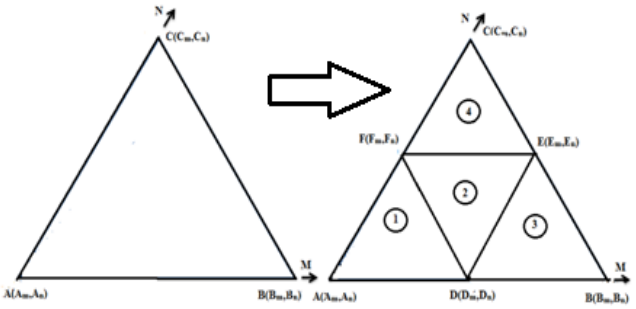


Figure 4. Fractal triangularization of sector 1 of space vector diagram.

Fig.4 shows single stage fractal triangularization of sector 1of space vector diagram. *A*, *B*and *C* are the vertices of the triangle selected (Fig.4 (a)).The coordinates of three new vertices *D*, *E* and *F* are determined by the following respectively,

$$D_m = (A_m + B_m)/2 \ , D_n = (A_n + B_n)/2 \qquad (4)$$

$$E_m = (B_m + C_m)/2 \, , E_n = (B_n + C_n)/2 \qquad (5)$$

$$F_m = (A_m + C_m)/2 \, , F_n = (A_n + C_n)/2 \qquad (6)$$

The centroids of the four newly formed triangles are determined along with vertices. If c_1,c_2,c_3 and c_4 are centroid of triangles marked as 1,2,3 and 4 (Fig.4(b)) respectively, then it is given by,

$$c_{1x} = (A_x + D_x + F_x)/3 \qquad (7)$$

$$c_{2x} = (D_x + E_x + F_x)/3 \qquad (8)$$

$$c_{3x} = (D_x + B_x + E_x)/3 \qquad (9)$$

$$c_{4x} = (F_x + E_x + C_x)/3 \qquad (10)$$

where x takes m and n respectively for the M axis and N axis.

The proposed direct vector quantization technique is explained by analyzing the example of a 5-level inverter. The fractalization of five-level inverter when the integrated error vector lies in sector 1 is shown in Fig.5.For 5-level inverter the number of iterations of triangularization carried out is two. During first triangularization the triangle *ABC* is divided into four triangles *ADF*, *DEF*, *DBE* and *EFC*, their vertices and centroids are calculated by using equations (4) to (10).The triangle whose centroid is at minimum Euclidian distance from integrated error space vector is selected and the triangle is renamed as triangle *ABC*. In the second Triangularization the above procedure is repeated for the newly obtained triangle *ABC*. After all the iterations are completed the vertex of triangle *ABC* which is nearer to V_E is selected as the quantized space vector $V_N(V_{Nm}, V_{Nn})$.

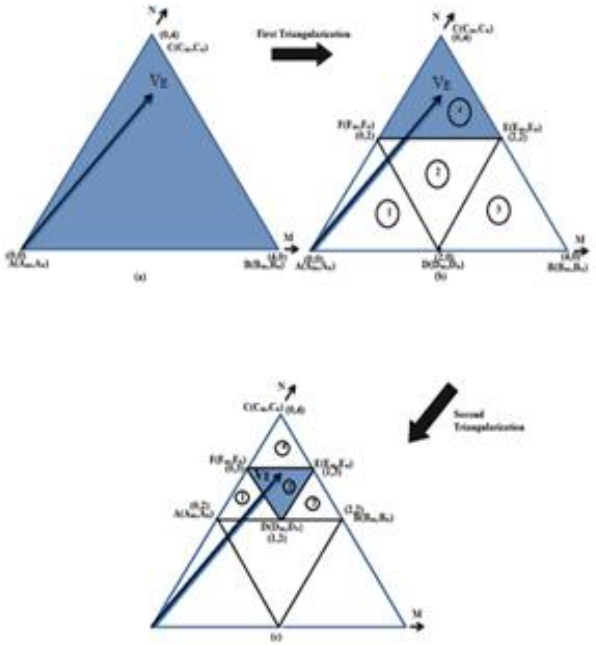


Figure 5. Determination of voronoi region of integrated error vector in a 5-level inverter

The proposed quantizer is 1-bit quantizer with a fixed step size of 1 irrespective of the level of inverter. The error produced by a quantizer in first order SDM is limited to a maximum of $\pm$ half the step size. The quantized space vector can be represented in time domain as

$$N[t] = V_E[t] \pm .5 \qquad (11)$$

The discrete integrator is realized by the transfer function $z^{-1}/(1-z^{-1})$. The integrated error vector is the proposed scheme can be expressed as

$$V_E[t] = V_{ref}[t-1] \mp .5 \qquad (12)$$

The quantized space vector can be expressed in terms of reference space vector as

$$N[t] = V_{ref}[t-1] \pm .5 \mp .5 \qquad (13)$$

At rated higher modulation index for a n-level inverter, the peak values of the integrated error vector will exceed the maximum permissible voltage range for n-level inverter. The proposed quantizer limits the error vector to switching states of n-level inverter by providing negative error to positive peak of error vector and vice versa as the boundary of quantizer is defined as per the level of inverter.

Determination of Switching Levels

The output of fractal based space vector quantizer gives the switching vector in 60^0coordinate system $V_N(V_{Nm},V_{Nn})$. This has to be mapped to inverter switching levels in abc frame (S_a, S_b and S_c).Fig.6 shows space vector diagram of 5-level inverter in abc frame. Here redundant states are not mentioned. Combining the occurrence of zero values of phases in different sectors with the 60^0 conversion equation (equation (1) and (2)) the switching levels in abc frame is determined. TABLE 1 shows the values of switching levels in abc frame [18].

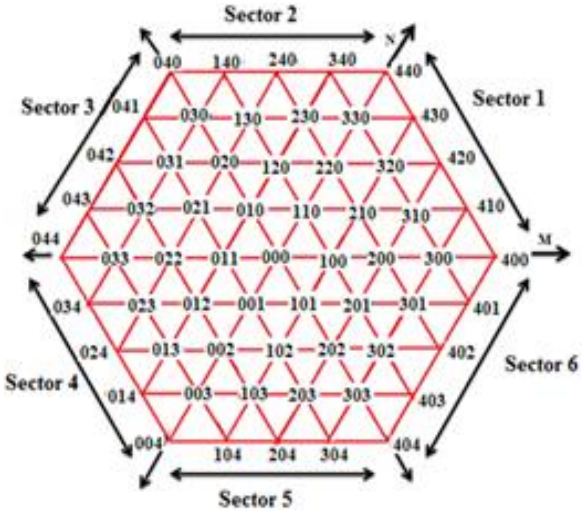


Figure 6. Space vector diagram of 5-level inverter in abc frame

Table 1. Determination of switching level in abc frame

Sector	Switching Level		
	S_a	S_b	S_c
1 and 2	$V_{Nm}+V_{Nn}$	V_{Nn}	*0*
3 and 4	*0*	$-V_{Nm}$	$-(V_{Nm}+V_{Nn})$
5 and 6	V_{Nm}	*0*	$-V_{Nn}$

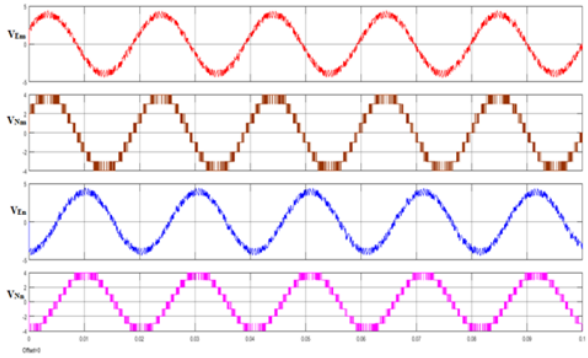


Figure 7. Resolved integrated error vector (V_{Em},V_{En}) and fractal based space vector quantizer output (V_{Nm},V_{Nn}) of 5 level inverter

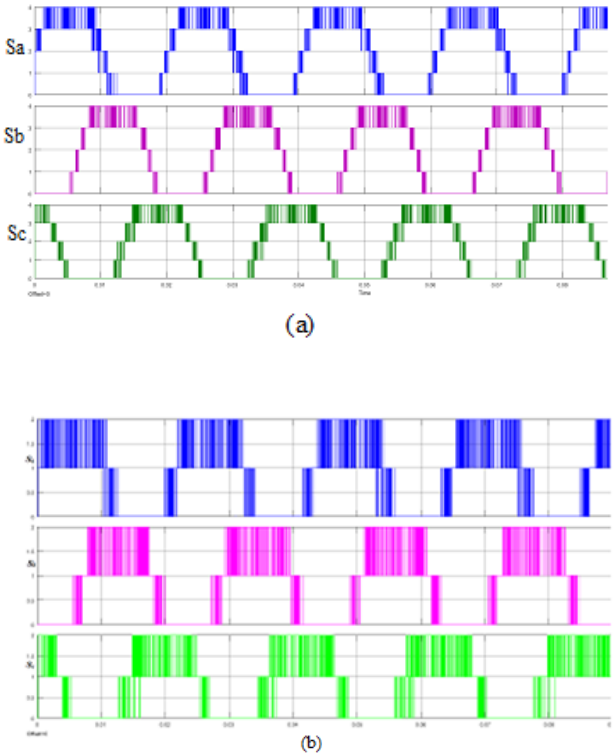


Figure 8(a) Switching levels of a 5-level inverter in abc frame for a modulation index of .85, **(b)** Switching levels of a 3-level inverter in abc frame for a modulation index of .8

SIMULATION RESULTS AND DISCUSSION

Fig.7 shows the integrated error vector and output of fractal based space vector quantizer along *M* axis and *N* axis for 5-level inverter. From Fig.7 it can be observed that V_N follows V_E. Fig.8(a) shows the simulated switching levels for a 5-level inverter in abc frame for modulation index 0.85 and Fig.8(b) shows the simulated switching levels for a three-level inverter in abc frame for modulation index 0.8. From Fig.8 (a) and Fig.8 (b) it can be observed that the simulated switching levels are like the effective pole voltages of five-level and three-level inverter respectively.

Fig.9 and Fig.10 shows the comparison of output of space vector quantizer in the existing method [16] and proposed method for a 5 level inverter at modulation index 0.85 and for a 3 level inverter at modulation index 0.8 respectively. The proposed space vector quantizer does not require any lookup table. From Fig.9 and Fig.10 it can be observed that at rated modulation index the existing direct vector quantization technique in SDM [16] generates $n+1$ switching levels for n-level inverter. The unwanted higher level switching is eliminated in the proposed technique. It can be also observed that the error in space vector quantizer of existing scheme is more for lower level inverter where as the proposed scheme effectively eliminate the error irrespective of level.

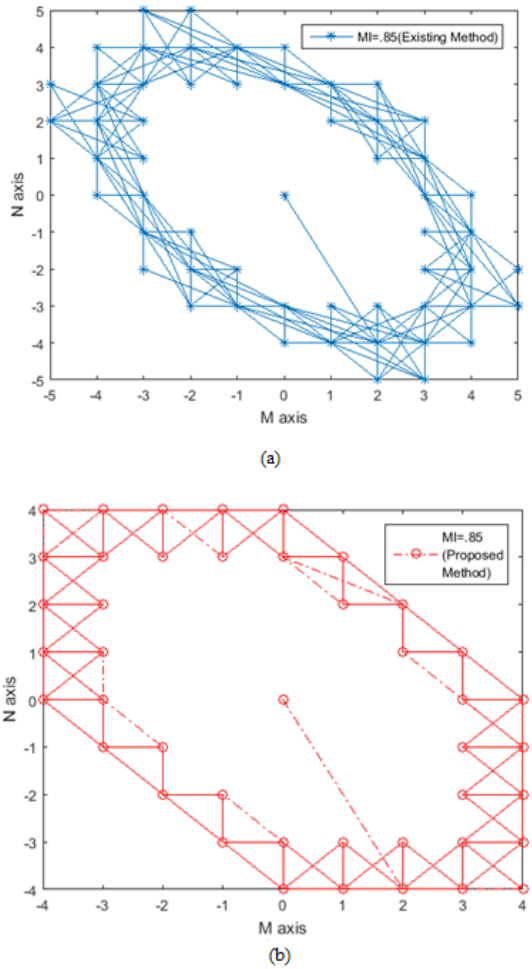
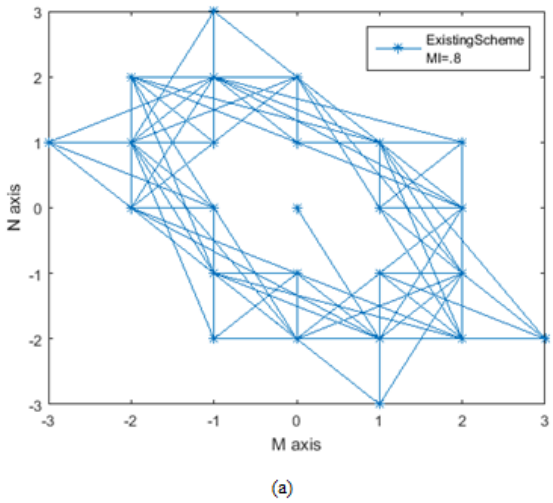


Figure 9. Output of Space vector quantizer for 5-level inverter at modulation index .85, (a) in existing method [16],(b) in proposed method



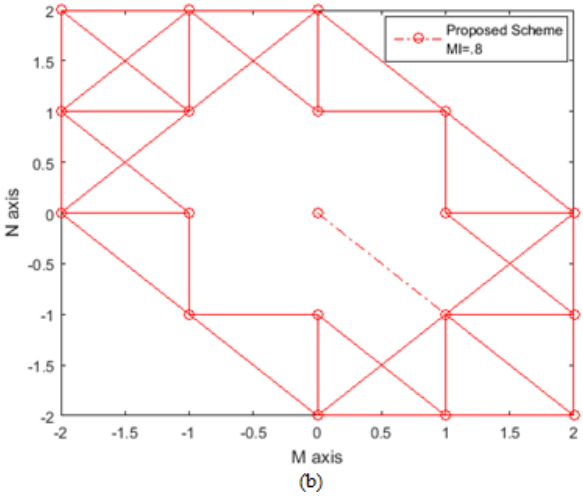


Figure 10. Output of Space vector quantizer for 3-level inverter at modulation index .8, (a) in existing method [16], (b) in proposed method

Fig.11 and Fig.12 shows the comparison of THD% of pole voltage obtained by the proposed scheme and existing direct vector quantization technique in SDM [16] for 5-level and 3-level inverter configuration respectively. It can be observed that the proposed scheme has less THD% compared to existing direct vector quantization technique in SDM [16].

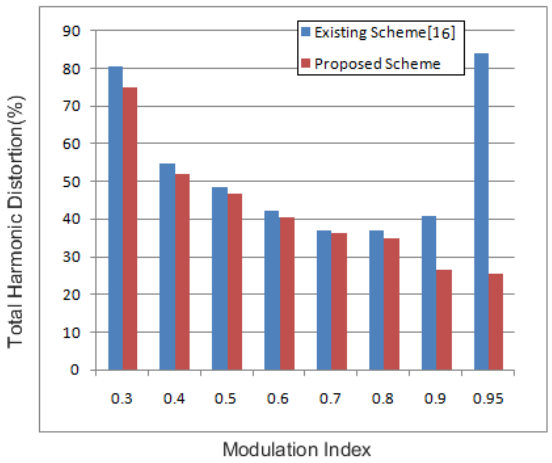


Figure 11. Comparison of THD characteristics of pole voltage of proposed scheme and existing scheme in SDM [16] for 5-level inverter

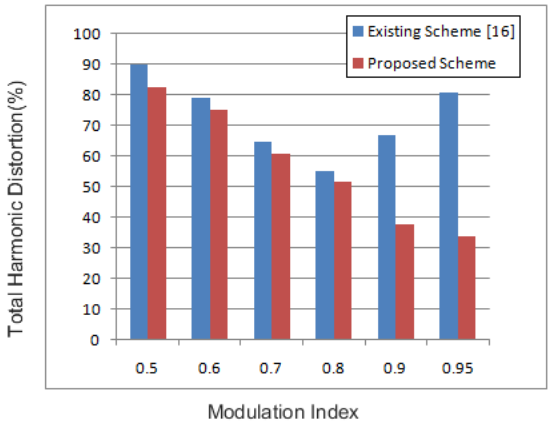


Figure 12. Comparison of THD characteristics of pole voltage of proposed scheme and existing scheme in SDM [16] for 3-level inverter

EXPERIMENTAL SETUP AND RESULT

Power Circuit

The proposed technique is implemented for three level configuration realized by open-ended winding induction motor as shown in Fig.13 [20]. It is used to drive a 5-hp three-phase induction motor for modulation index .8. dSPACE DS 1104 RTI platform is used to implement the proposed scheme at a sampling frequency of 20 kHz. Table 2 shows the switches that are ON for individual inverters during different voltage levels (for A-Phase) [20].

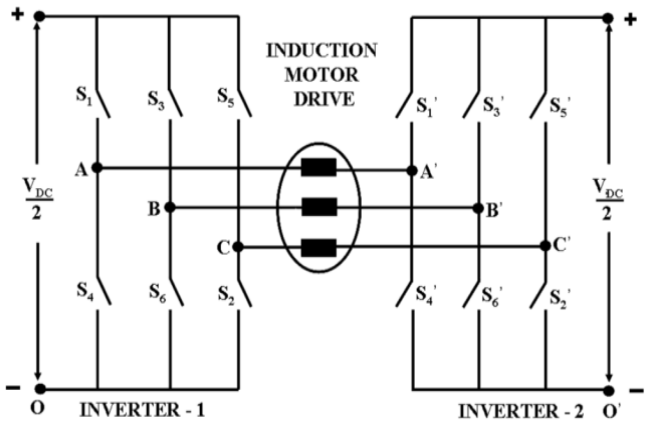


Figure 13. Three level inverter configuration driving an open end winding induction motor

Table 2. Switches turned ON for individual inverters during different voltage levels (for A - phase)

Switch turned ON in INVERTER-1	Switch turned ON in INVERTER-2	A-phase voltage	Switching Level
S4	S1’	$-V_{DC}/2$	0
S4	S4’	0	1
S1	S4’	$V_{DC}/2$	2

Experimental Result

Fig. 14 shows the pole voltages for the three-level inverter for modulation index m =0 .8. The upper, middle and lower trace shows the pole voltage of Inverter –I(V_{AO}),Inverter-II ($V_{A'O'}$) and the effective pole voltage ($V_{AO} - V_{A'O'}$) respectively.$V_{AO} - V_{A'O'}$ is similar to the pole voltage of a cascaded three-level inverter.

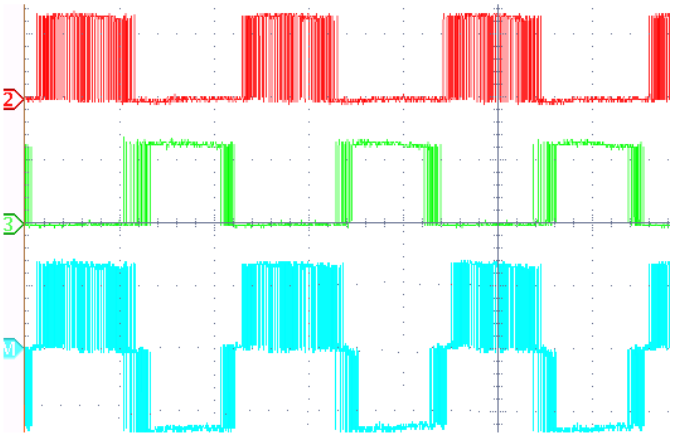


Figure 14. Three level-inverter pole voltages with modulation indexm =0 .8. (Upper trace) Pole voltage (V_{AO}) of INVERTER-1. (Middle trace) Pole voltage ($V_{A'O'}$) of INVERTER-2. (Lower trace) Effective pole Voltage ($V_{AO} - V_{A'O'}$). Scale: X-axis: 10 ms/div; Y -axis: 50 V/div.

The phase voltage($V_{AA'}$) and phase current(I_A) along A phase for the three-level inverter configuration for modulation index. 8 is shown in Fig.15.

In the proposed technique switching frequency varies randomly and this results in the spreading of spectrum. Fig.16 shows the phase voltage spectrum of the three level inverter for modulation index .8.

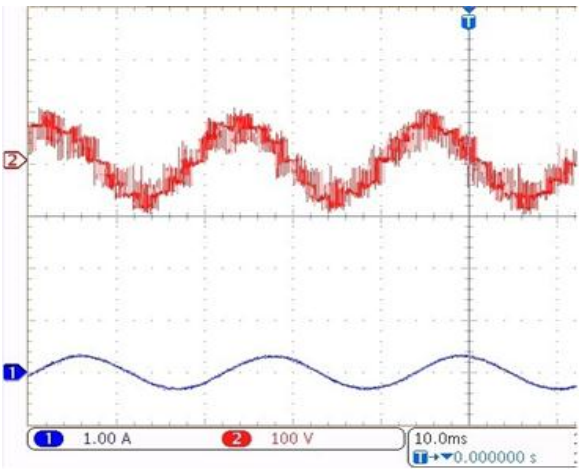


Figure 15. (Upper trace)A-phase voltage ($V_{AA'}$) of 3-level inverter at modulation index .8. Scale: X-axis: 10 ms/div; Y -axis: 50 V/div. (Lower trace) Motor phase current (I_A). Scale: Y -axis: 1 A/div

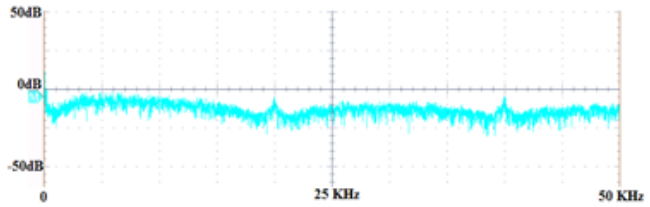


Figure 16. Experimental pole voltage spectrum of three-level inverter for the proposed scheme with modulation index m =0.8

CONCLUSION

A Sigma Delta Modulation scheme for multilevel inverter which quantizes the reference space vector directly using a hexagonal quantizer with fractal features of space vector diagram is presented in this paper. The scheme is compared with the existing direct vector quantization technique in SDM and verified that it eliminates the generation of impermissible switching states for n-level inverter. Simulation results for five-level and three-level inverter are verified and presented in this paper .The proposed scheme has better performance than existing direct vector quantization technique in SDM in terms of THD. The proposed technique is implemented to drive a 5hp open-ended winding induction motor in three level configuration at rated modulation index and the experimental results are verified.

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