
INTRODUCTION

Voltage controlled oscillators (VCOs) are widely used in mixed blocks in analog and mixed signal electronic circuits such as Phase Locked Loops (PLLs), analog to digital converters (ADCs), radio frequency integrated circuits (RFICs) and many other mixed circuits [1], [2]. VCO designs mainly comprises topologies such as LC tank oscillators and ring oscillator VCOs. Ring oscillator VCOs provide comparatively wider tuning range in PLL applications, occupy lesser silicon area as compared to LC tank oscillators and are better suited for silicon integration [3]. However, LC tank oscillator based PLL designs exhibit better phase noise performance as compared to ring oscillator VCOs [4], [5]. A commonly used ring oscillator based VCO topology is a current starved voltage controlled oscillator (CSVCO) which consists of several number of VCO stages comprising of current starvation stages and inverters [6]. As compared to CSVCO, Schmitt trigger based VCO needs a single VCO stage, a Schmitt trigger with hysteresis and a single inverter resulting in less number of transistors required for the circuit. In this paper we propose Schmitt trigger based voltage controlled oscillator that uses hybrid CMOS and CNFET approach. The proposed hybrid circuit is optimized to achieve better linearity and reduced power dissipation as compared to pure CMOS circuit. Simulations of the proposed VCO circuit are performed in HSPICE environment. CNFETs, owing to very high electron mobility, efficient transport of carriers and improved gate electrostatics carbon nanotubes serve as an excellent active channel of a transistor device [7], [8]. Apart from simple integrated circuits such as logic gates and ring oscillator, CNFETs have been extensively investigated for many analog and radio frequency (RF) circuits. Recent reports have shown that CNFETs are potentially promising candidates for highly linear RF circuits and applications. Researchers in [9] have demonstrated that CNFETs possess linearity that is comparable to that of conventional MOSFETs. Hybrid realization of electronic circuits utilizing conventional MOSFETs and emerging nano-electronic devices has been presented by several researchers. A hybrid 3D integration of CMOS-CNFTs circuit, voltage controlled oscillator, carbon nanotube field effect transistors, monolithic 3D integration.
Hybrid CMOS-CNFET Voltage Controlled Oscillator

Ring oscillator VCOs consists of n-number of stages with each stage contributing to the overall nonlinearity of the VCO. To overcome this issue the topology given in Figure 1 can be employed wherein a single current starvation stage followed by a Schmitt trigger with hysteresis is used. One of the applications of Schmitt trigger is an RC oscillator. Similarly a Schmitt trigger along with current sources can form a voltage controlled oscillator. The proposed design utilizes CNFETs for the construction of the Schmitt trigger. Also transistors M1 and M4 are CNFETs which act as current sources mirroring the currents in MOSFETs M5 and M6. The inverter is realized using conventional MOSFETs. The 32nm channel length CNFETs with chiral vector of (17,0) corresponding to a threshold voltage of 0.323V have been chosen. The number of tubes equal to 3 with inter CNT pitch of 4nm is used. PTM LP 32nm model is chosen for the MOSFETs. MOSFETs used in the hybrid implementation are sized with W/L=10.

![Figure 1: Hybrid CMOS and CNFET voltage controlled oscillator](image)

The Schmitt trigger circuit uses equally sized CNFETs with gate width of 40nm and channel lengths of 32nm. If $V_{SPH}$ and $V_{SPL}$ are higher switching point and lower switching point voltages respectively and $V_{THN}$ and $V_{THP}$ are threshold voltages of NCNFET and PCNFET respectively then we can write,

\[
\frac{V_{DD} - V_{SPH}}{V_{SPH} - V_{THN}} = \frac{W_1 L_{11}}{L_1 W_{11}}
\]

\[
\frac{V_{SPL}}{V_{DD} - V_{SPL} - V_{THP}} = \frac{W_{10} L_{12}}{L_{10} W_{12}}
\]

For equally sized CNFETs,

\[
\frac{V_{DD} - V_{SPH}}{V_{SPH} - V_{THN}} = 1
\]

\[
\frac{V_{SPL}}{V_{DD} - V_{SPL} - V_{THP}} = 1
\]

The oscillations produced by the circuit for VCO control voltage of 0.3V are shown in Figure 2. The Schmitt trigger hysteresis of 0.323V results in capacitor to charge and discharge between $V_{SPL}$ and $V_{SPH}$ producing sustained oscillations. The frequency $f_{osc}$ can be found with an expression.

\[
f_{osc} = \frac{1}{C V_{hyst} (\frac{1}{i_{DM1}} - \frac{1}{i_{DM4}})}
\]

![Figure 2: Output Waveform of Hybrid CMOS-CNFET voltage controlled oscillator](image)

![Figure 3: Frequency vs VCO control voltage for hybrid and CMOS VCOs](image)

One of the prime requirement of a VCO for PLL applications is wide and linear tuning range. Figure 3 shows the VCO oscillation frequency as a function of control voltage for CMOS implementations and a hybrid CMOS-CNFET implementation. The hybrid circuit exhibits a better linear response as compared to pure CMOS circuit. The nonlinear response in pure CMOS circuit is because of high $V_{th}$ devices being used for reduction in power dissipation. Use of high...
performance low $V_a$ devices yields in better linearity at the cost of higher power dissipation. The hybrid circuit compensates the nonlinearity produced by the transistor M5 which is under weak inversion (sub-threshold conduction) for control voltage below $V_{\text{TH}}$. The compensation is achieved by replacing CMOS transistors M1 and M4 by CNFETs and realizing a CNFET Schmitt trigger. Often a linearization technique based on a resistor and a wide CMOS device is used in the VCO designs. However the proposed hybrid circuit does not need a resistor or a wide device for achieving linear response.

Comparison of VCOs realized using different technology nodes with hybrid CMOS-CNFT VCO is shown in Table I (VCO control voltage varied from 0.3V to 0.8V).The hybrid VCO provides relatively smaller gain ($K_{\text{vco}}$) which is desired in low jitter PLL applications. Referring Table I, Figure 3 and Figure 4 it can be seen that the hybrid circuit dissipates less power and generates higher frequency for the same control voltage.

**Table I: A Comparison of Proposed VCO with Conventional CMOS VCOs**

<table>
<thead>
<tr>
<th>VCO</th>
<th>fmin (Hz)</th>
<th>fmax (Hz)</th>
<th>$K_{\text{vco}}$ (MHz/mV)</th>
<th>Min Power Diss. (μW)</th>
<th>Max. Power Diss. (μW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32nm</td>
<td>3.1MHz</td>
<td>2.5GHz</td>
<td>5.14MHz/mV</td>
<td>7.2μW</td>
<td>101.1μW</td>
</tr>
<tr>
<td>LP</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CMOS</td>
<td>858.4MHz</td>
<td>12.6GHz</td>
<td>148MHz/mV</td>
<td>126μW</td>
<td>480μW</td>
</tr>
<tr>
<td>32nm</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CMOS</td>
<td>389.9MHz</td>
<td>2.7GHz</td>
<td>4.61MHz/mV</td>
<td>94.1μW</td>
<td>298.9μW</td>
</tr>
<tr>
<td>50nm</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Hybrid</td>
<td>84.0MHz</td>
<td>1.6GHz</td>
<td>3.10MHz/mV</td>
<td>3.6μW</td>
<td>65.4μW</td>
</tr>
</tbody>
</table>

This gives a simple way to scale the VCO frequency at design time to satisfy VCO specifications for a PLL application. The thin gate oxide in a CNFET results in a higher transconductance and drive current[16], [17]. Figure 6 shows the effect of gate oxide thickness on the frequency and power dissipation in a hybrid VCO. For low power VCOs relatively higher gate oxide thickness can be used to reduce drive current and achieve reduced dynamic power consumption.

**Figure 4**: Power dissipation vs VCO control voltage for hybrid and CMOS VCO

**Effect of CNFET Parameter Variation on VCO Frequency and Power Dissipation**

The proposed circuit is investigated for the generated frequency and power dissipation under variations in parameters such as control voltage, number of tubes in the CNFETs, gate oxide thickness, CNFET chiral vectors (threshold voltage) and inter CNT pitch. The oscillator frequency varies linearly with increasing the number of nanotubes in a CNFET for a given control voltage (Figure 5).

**Figure 5**: Effect of number of tubes in CNFET on frequency and power dissipation for a hybrid VCO

**Figure 6**: Effect of CNFET gate oxide thickness on VCO frequency and power dissipation for a hybrid VCO.

For a fixed width CNFET increasing the nanotube density ie. Decreasing inter CNT pitch results in screening amongst parallel CNTs affecting gate to channel capacitance and current drive. The drive current remains constant for both middle and edge CNTs if inter CNT pitch is greater than 20nm. Decreasing the inter CNT pitch below 20nm results in reduced drive current with middle CNT current decreasing at a faster rate than that of the edge CNTs [18],[19]. Hence in our circuit decreasing the pitch causes the drive current to decrease, resulting in decreased oscillation frequency and reduced power dissipation (Figure 7). The hybrid circuit is also investigated for different CNFET threshold voltages. CNFET threshold voltage is inversely related to the diameter of the CNT. The diameter depends upon the chiral vector denoted by two indices (n, m). The diameter and the threshold voltage ($V_a$) of the CNFET can be calculated using eq. 9 and eq. 10.

$$D_{\text{CNT}} = \frac{a_n\sigma}{\pi}\sqrt{n^2 + nm + m^2}$$  \hspace{1cm} (9)
\[ V_{th} = \sqrt{\frac{\sqrt{a_0 V_t}}{3eD_{CNT}}} \tag{10} \]

Where \( a_0 \) (0.142nm) is the inter-atomic distance between each carbon atom and its neighbor, \( a \) (2.49Å) is the lattice constant, \( V_t \) (3.033eV) is the carbon π-π bond energy, \( e \) is the unit electron charge. Figure 8 shows frequency and power dissipation for the hybrid VCO at different CNFET threshold voltages for a VCO control voltage of 0.3V. The hybrid circuit is investigated for a set of chiral vectors/threshold voltages \((26, 0) / 0.220V, (23, 0) / 0.250V, (20, 0) / 0.289V, (17, 0) / 0.323V\) and \((14, 0) / 0.392V\). Higher the CNFET \( V_t \), oscillation frequency and power dissipated by the hybrid VCO decreases accordingly.

**REFERENCES**


