International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 9 (2017) pp. 1969-1973

A Low Power and Linear Voltage Controlled Oscillator Using Hybrid CMOS-CNFET Technology

S. B. Rahane
Matoshri College of Engineering and Research Center, Nasik,
Savitribai Phule Pune University, Pune, India.

ORCID: 0000-0003-4688-9557

A.K. Kureshi
Vishwabharati Academy's College of Engineering, Ahemadnagar,
Savitribai Phule Pune University, Pune, India.

ORCID: 0000-0002-3013-6377

Abstract
This paper presents a hybrid CMOS-CNFET voltage controlled oscillator (VCO) with low power dissipation and linear response over a wide control voltage range. The hybrid circuit is based on PTM 32nm low power CMOS devices and 32nm CNFET devices with different threshold voltages. The VCO frequency and power dissipation are investigated for CNFET parameters such as number of nano-tubes, gate oxide thickness, inter CNT pitch and chiral vectors. The linearization of VCO response is achieved using a hybrid CMOS-CNFET device combination without needing a resistor or a wide device. The circuit exhibits excellent linearity as compared to pure CMOS circuit over a tuning range from 84MHz to 1.6GHz corresponding to a control voltage range from 0.3V to 0.8V. The VCO power dissipation is confined within sub 15μW range for control voltages up to 0.6V.

Keywords*:* Hybrid CMOS-CNFET circuits, Voltage controlled oscillator, Carbon nanotube field effect transistors, Monolithic 3D integration.

INTRODUCTION

Voltage controlled oscillators (VCOs) are widely used building blocks in analog and mixed signal electronic circuits such as Phase Locked Loops (PLLs), analog to digital converters (ADCs), radio frequency integrated circuits (RFICs) and many other mixed circuits [1],[2]. VCO designs mainly comprises topologies such as LC tank oscillators and ring oscillator VCOs. Ring oscillator VCOs provide comparatively wider tuning range in PLL applications, occupy lesser silicon area as compared to LC tank oscillators and are better suited for silicon integration [3]. However, LC tank oscillator based PLL designs exhibit better phase noise performance as compared to ring oscillator VCOs [4], [5]. A commonly used ring oscillator based VCO topology is a current starved voltage controlled oscillator (CSVCO) which consists of several number of VCO stages comprising of current starvation stages and inverters [6]. As compared to CSVCO, Schmitt trigger based VCO needs a single VCO stage, a Schmitt trigger with hysteresis and a single inverter resulting in less number of transistors required for the circuit. In this paper we propose Schmitt trigger based voltage controlled oscillator that uses hybrid CMOS and CNFET approach. The proposed hybrid circuit is optimized to achieve better linearity and reduced power dissipation as compared to pure CMOS circuit. Simulations of the proposed VCO are performed in a HSPICE environment. CNFETs, owing to very high electron mobility, efficient transport of carriers and improved gate electrostatics carbon nanotubes serve as an excellent active channel of a transistor device [7],[8]. Apart from simple integrated circuits such as logic gates and ring oscillator, CNFETs have been extensively investigated for many analog and radio frequency (RF) circuits. Recent reports have shown that CNFETs are potentially promising candidates for highly linear RF circuits and applications. Researchers in [9] have demonstrated that CNFETs possesses linearity that is comparable to that of conventional MOSFETs. Hybrid realization of electronic circuits utilizing conventional MOSFETs and emerging nano-electronic devices has been presented by several researchers. A hybrid 3D integration of CMOS-CNFET inverter is proposed in [10].Stanford University researchers in [11] presented a RF cascade amplifier with co-integration of NMOS and PCNFET.A chemical sensing application utilizing hybrid CMOS-CNFET approach is reported in [12].A leakage control scheme using hybrid CMOS-CNEMS (Carbon nanotube nano-electromechanical switches) is reported in [13]. Replacement of CMOS sleep transistors by CNFETs for power gating is proposed in [14]. Future of the nano-electronic systems rely on novel monolithic 3D integration of heterogeneous circuits such as computational elements, memory, RF and analog building blocks. Such type of 3D integrated systems having futuristic applications have been reported in [15], wherein researchers reported vertically stacked integrated circuit layers involving hybrid co-integration of CNFET logic blocks and conventional silicon CMOS logic blocks. Proposed hybrid CMOS-CNFET VCO circuit consisting both CMOS and CNFET devices is a potential candidate for futuristic 3D integrated monolithic chips. Following sections in this paper cover description of the hybrid-CMOS CNFET VCO with relevant analysis and performance comparison with pure CMOS implementation. Effect of CNFET parameters on VCO frequency and power dissipation is also presented in the subsequent section.

Hybrid CMOS-CNFET Voltage Controlled Oscillator

Ring oscillator VCOs consists of n-number of stages with each stage contributing to the overall nonlinearity of the VCO. To overcome this issue the topology given in Figure 1 can be employed wherein a single current starvation stage followed by a Schmitt trigger with hysteresis is used. One of the applications of Schmitt trigger is an RC oscillator. Similarly a Schmitt trigger along with current sources can form a voltage controlled oscillator. The proposed design utilizes CNFETs for the construction of the Schmitt trigger. Also transistors M1 and M4 are CNFETs which act as current sources mirroring the currents in MOSFETs M5 and M6. The inverter is realized using conventional MOSFETs. The 32nm channel length CNFETs with chiral vector of (17,0) corresponding to a threshold voltage of 0.323V have been chosen. The number of tubes equal to 3 with inter CNT pitch of 4nm is used. PTM LP 32nm model is chosen for the MOSFETs. MOSFETs used in the hybrid implementation are sized with W/L=10.

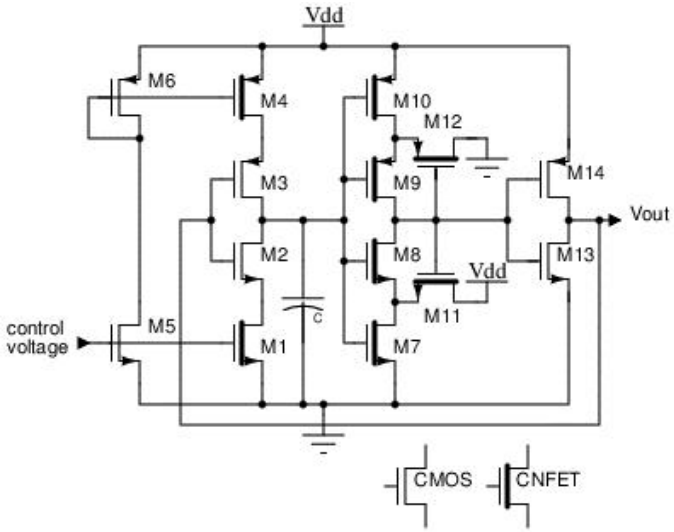

Figure 1: Hybrid CMOS and CNFET voltage controlled oscillator

The Schmitt trigger circuit uses equally sized CNFETs with gate width of 40nm and channel lengths of 32nm.If V_{SPH} and V_{SPL} are higher switching point and lower switching point voltages respectively and V_{THN} and V_{THP} are threshold voltages of NCNFET and PCNFET respectively then we can write,

$$\left[\frac{V_{DD}-V_{SPH}}{V_{SPH}-V_{THN}}\right]^2=\frac{W_7L_{11}}{L_7W_{11}} \quad (1)$$

$$\left[\frac{V_{SPL}}{V_{DD}-V_{SPL}-V_{THP}}\right]^2=\frac{W_{10}L_{12}}{L_{10}W_{12}} \quad (2)$$

For equally sized CNFETs,

$$\left[\frac{V_{DD}-V_{SPH}}{V_{SPH}-V_{THN}}\right]^2=1 \quad (3)$$

$$\left[\frac{V_{SPL}}{V_{DD}-V_{SPL}-V_{THP}}\right]^2=1 \quad (4)$$

$$V_{SPH}=\frac{V_{DD}+V_{THN}}{2} \quad (5)$$

$$V_{SPL}=\frac{V_{DD}-V_{THP}}{2}=\frac{1+0.323}{2}=0.6615V \quad (6)$$

$$V_{SPL}=\frac{V_{DD}-V_{THP}}{2}=\frac{1-0.323}{2}=0.3385V \quad (7)$$

The oscillations produced by the circuit for VCO control voltage of 0.3V are shown in Figure 2. The Schmitt trigger hysteresis of 0.323V results in capacitor to charge and discharge between V_{SPL} and V_{SPH} producing sustained oscillations. The frequency f_{osc} can be found with an expression.

$$f_{osc}=\frac{1}{C\,V_{hyst}\left(\frac{1}{I_{DM1}}-\frac{1}{I_{DM4}}\right)} \quad (8)$$

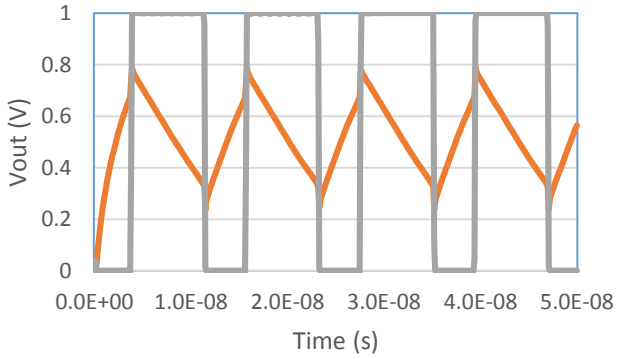

Figure 2: Output Waveform of Hybrid CMOS-CNFET voltage controlled oscillator

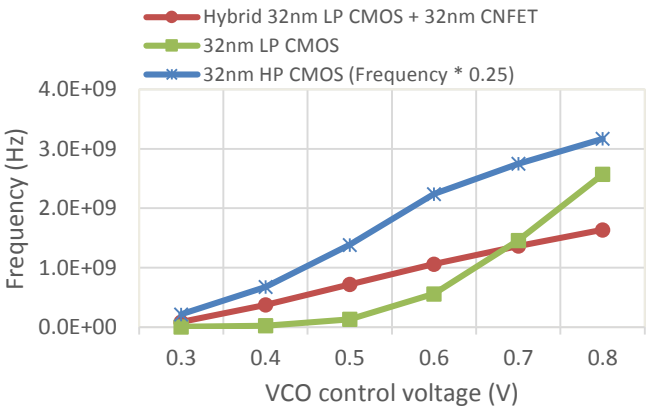

Figure 3: Frequency vs VCO control voltage for hybrid and CMOS VCOs

One of the prime requirement of a VCO for PLL applications is wide and linear tuning range. Figure 3 shows the VCO oscillation frequency as a function of control voltage for CMOS implementations and a hybrid CMOS-CNFET implementation. The hybrid circuit exhibits a better linear response as compared to pure CMOS circuit. The nonlinear response in pure CMOS circuit is because of high V_{th} devices being used for reduction in power dissipation. Use of high

performance low V_{th} devices yields in better linearity at the cost of higher power dissipation. The hybrid circuit compensates the nonlinearity produced by the transistor M5 which is under weak inversion (sub-threshold conduction) for control voltage below V_{THN}. The compensation is achieved by replacing CMOS transistors M1 and M4 by CNFETs and realizing a CNFET Schmitt trigger. Often a linearization technique based on a resistor and a wide CMOS device is used in the VCO designs. However the proposed hybrid circuit does not need a resistor or a wide device for achieving linear response.

Comparison of VCOs realized using different technology nodes with hybrid CMOS-CNFET VCO is shown in Table I (VCO control voltage varied from 0.3V to 0.8V).The hybrid VCO provides relatively smaller gain (K_{vco}) which is desired in low jitter PLL applications. Referring Table I, Figure 3 and Figure 4 it can be seen that the hybrid circuit dissipates less power and generates higher frequency for the same control voltage.

Table I: A Comparison of Proposed VCO with Conventional CMOS VCOs

VCO	fmin	fmax	Kvco	Min Power Diss.	Max. Power Diss.
CMOS 32nm LP	3.1MHz	2.5GHz	5.14MHz/mV	7.2µW	101.1µW
CMOS 32nm HP	858.4MHz	12.6GHz	148MHz/mV	126µW	480µW
CMOS 50nm	389.9MHz	2.7GHz	4.61MHz/mV	94.1µW	298.9µW
Hybrid	84.0MHz	1.6GHz	3.10MHz/mV	3.6µW	65.4µW

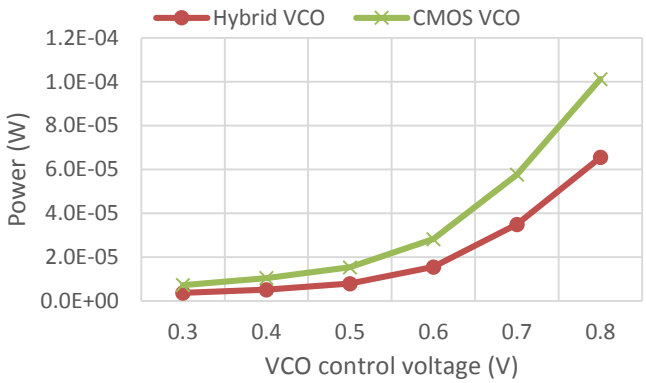

Figure 4: Power dissipation vs VCO control voltage for hybrid and CMOS VCO

Effect of CNFET Parameter Variation on VCO Frequency and Power Dissipation

The proposed circuit is investigated for the generated frequency and power dissipation under variations in parameters such as control voltage, number of tubes in the CNFETs, gate oxide thickness, CNFET chiral vectors (threshold voltage) and inter CNT pitch. The oscillator frequency varies linearly with increasing the number of nanotubes in a CNFET for a given control voltage (Figure 5). This gives a simple way to scale the VCO frequency at design time to satisfy VCO specifications for a PLL application. The thin gate oxide in a CNFET results in a higher transconductance and drive current[16], [17].Figure 6 shows the effect of gate oxide thickness on the frequency and power dissipation in a hybrid VCO. For low power VCOs relatively higher gate oxide thickness can be used to reduce drive current and achieve reduced dynamic power consumption.

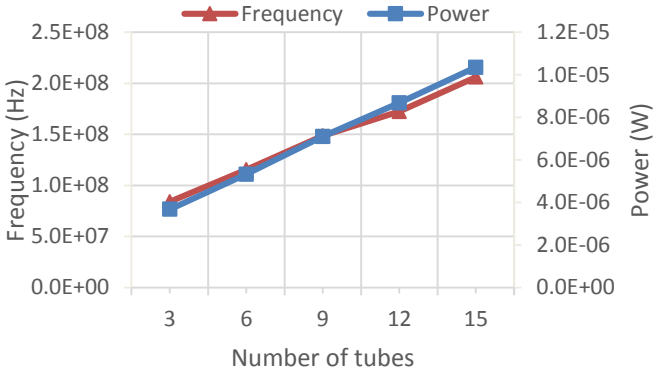

Figure 5: Effect of number of tubes in CNFET on frequency and power dissipation for a hybrid VCO

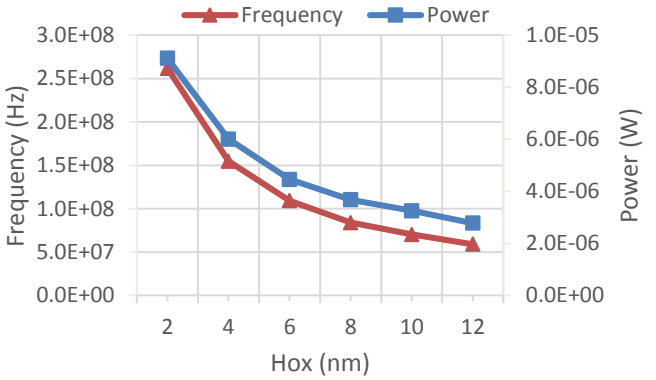

Figure6: Effect of CNFET gate oxide thickness on VCO frequency and power dissipation for a hybrid VCO.

For a fixed width CNFET increasing the nanotube density ie. Decreasing inter CNT pitch results in screening amongst parallel CNTs affecting gate to channel capacitance and current drive. The drive current remains constant for both middle and edge CNTs if inter CNT pitch is greater than 20nm. Decreasing the inter CNT pitch below 20nm results in reduced dive current with middle CNT current decreasing at a faster rate than that of the edge CNTs [18],[19]. Hence in our circuit decreasing the pitch causes the drive current to decrease, resulting in decreased oscillation frequency and reduced power dissipation (Figure 7). The hybrid circuit is also investigated for different CNFET threshold voltages. CNFET threshold voltage is inversely related to the diameter of the CNT. The diameter depends upon the chiral vector denoted by two indices (n, m). The diameter and the threshold voltage (V_{th}) of the CNFET can be calculated using eq. 9 and eq. 10.

$$D_{CNT} = \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + nm + m^2} \quad (9)$$

$$V_{th} = \frac{\sqrt{3}}{3}\frac{a\,V_{\pi}}{eD_{CNT}} \quad (10)$$

Where a_0 (0.142nm) is the inter-atomic distance between each carbon atom and its neighbor, a (2.49Å) is the lattice constant, Vπ (3.033eV) is the carbon π-π bond energy, e is the unit electron charge. Figure 8 shows frequency and power dissipation for the hybrid VCO at different CNFET threshold voltages for a VCO control voltage of 0.3V. The hybrid circuit is investigated for a set of chiral vectors/threshold voltages (26, 0) / 0.220V, (23, 0) /0 .250V, (20, 0) / 0.289V, (17, 0) / 0323V and (14, 0), 0.392V. Higher the CNFET V_{th}, oscillation frequency and power dissipated by the hybrid VCO decreases accordingly.

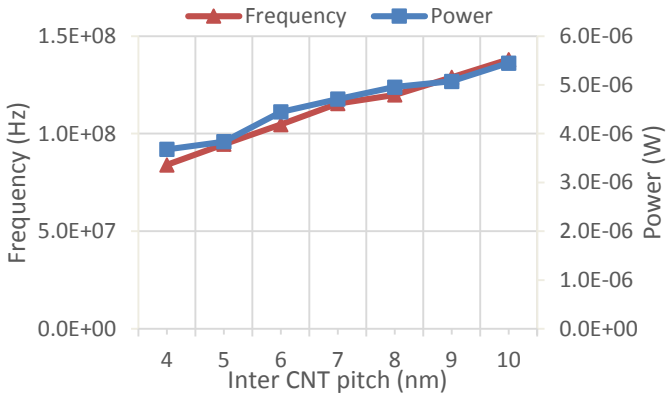

Figure 7: Effect of CNFET inter CNT pitch on VCO frequency and power dissipation for a hybrid VCO

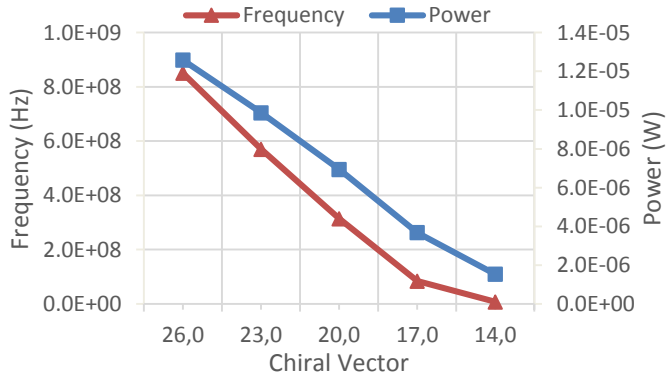

Figure 8: Effect of chiral vector (threshold voltage) on frequency and power dissipation for hybrid VCO

CONCLUSION

Hybrid CMOS-CNFET VCO using Schmitt trigger and current sources is presented in this paper. The VCO was optimized for minimum dynamic power consumption by suitably adjusting CNFET parameters such as threshold voltage (chirality), inter CNT pitch, gate oxide thickness and number of nano-tubes. The hybrid topology with 32nm LP CMOS devices and 32nm CNFETs having chirality of (17,0), inter CNT pitch of 4nm, gate oxide thickness of 8nm were found to be optimum for minimizing power dissipation. The VCO oscillation frequency can be tuned linearly with a gain of 3.1MHz/mV from 84MHz to 1.6GHz. The minimum and maximum power dissipation were 3.6µW to 65.4µW respectively. This type of hybrid co-integration of CMOS and CNFET devices can form a basis for the futuristic 3D integrated monolithic chips.

REFERENCES

[1] Wang,S. F., 2015, "Low-Voltage, Full-Swing Voltage-Controlled Oscillator with Symmetrical Even-Phase Outputs Based on Single-Ended Delay Cells," in IEEE Trans. on Very Large Scale Integration (VLSI) Systems, 23(9), pp. 1801-1807.

[2] SawS. K., and NathV., 2015, "Performance Analysis of Low Power CSVCO for PLL Architecture," Advances in Computing and Communication Engineering (ICACCE), Second International Conference on, Dehradun, pp. 370-373.

[3] Kamalinejad, P., Keikhosravy,K., Molavi,R., Mirabbasi, S., and Leung,V. C. M., 2014, "An ultra-low-power CMOS voltage-controlled ring oscillator for passive RFID tags," New Circuits and Systems Conference (NEWCAS),IEEE 12th International, Trois-Rivieres, QC, pp. 456-459.

[4] Li, G.,and Afshari,E., 2010, "A Low-Phase-Noise Multi-Phase Oscillator Based on Left-Handed LC-Ring," in IEEE J. of Solid-State Circuits, 45(9), pp. 1822-1833.

[5] Ling, Sun, et al., 2010, "CMOS ring VCO for UHF RFID readers," The J. of China Universities of Posts and Telecommunications, 17(3), pp.20-23.

[6] Kougianos, Elias, and Mohanty, S. P., 2009, "Impact of gate-oxide tunneling on mixed-signal design and simulation of a nano-CMOS VCO." Microelectronics J., 40(1),pp. 95-103.

[7] Yang, M. H. et. al., 2006, "Advantages of top-gate, high-k dielectric carbon nanotube field-effect transistors," Appl. Phys. Lett., 88(11), pp. 113507.

[8] Appenzeller,J., Knoch,J., Martel,R., Derycke,V., Wind,S. J., and Avouris,P., 2002, "Carbon nanotube electronics," in IEEE Trans. on Nanotechnology, 1(4), pp. 184-189.

[9] Alam,A. U., Rogers,C. M. S., Paydavosi,N., Holland,K. D., Ahmed, S., and Vaidyanathan,M., 2013, "RF Linearity Potential of Carbon-Nanotube Transistors versus MOSFETs," in IEEE Trans. on Nanotechnology, 12(3), pp. 340-351.

[10] Meric,I., Caruso,V., Caldwell,R., Hone,J., Shepard,K. L., Wind,S. J.,2007, "Hybrid carbon nanotube-silicon complementary metal oxide semiconductor circuits," J. Vac. Sci. Technol. B, 25(6),pp. 2577-2580.

[11] Akinwande,D., Yasuda,S., Paul,B., Fujita,S., Close,G., and Wong,H., 2008, "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications," IEEE Trans. on Nanotechnology, 7(5), pp. 636-639.

[12] Cho,T.S., Lee,K.J., Pan,T., Kong,J., Chandrakasan,A.P., 2007, "Design and characterization of CNT-CMOS hybrid systems," MTL Annual Research Report.

[13] Chakraborty et. el., 2007, "Hybridization of CMOS with CNT-based nano-electromechanical switch for low leakage and robust circuit design," IEEE Trans. on Circuits and Systems—I: Regular Papers, 54(11),pp. 2480-2488.

[14] Kim,K. K., Kim,Y.B., and Choi,K., 2011, "Hybrid CMOS and CNFET power gating in ultralow voltage design," IEEE Trans. on Nanotechnology, 10(6), pp. 1439-1448.

[15] Shulaker,M. M., Wu,T. F., Sabry,M. M., Wei,H., Wong, H. S. P., and Mitra,S., 2015, "Monolithic 3D integration: A path from concept to reality," 2015 Design, Automation and Test in Europe Conference and Exhibition (DATE), Grenoble, pp. 1197-1202.

[16] Dass,D., Prasher,R., and Vaid.R., 2013, "Impact of Scaling Gate Insulator Thickness on the Performance of Carbon Nanotube Field Effect Transistors (CNTFETs)." J. of Nano-and Electronic Physics 5(2), pp. 2014-1-2014-6.

[17] Kshirsagar,C., Li,H., Kopley,T. E. and Banerjee,K., 2008, "Accurate Intrinsic Gate Capacitance Model for Carbon Nanotube-Array Based FETs Considering Screening Effect," in IEEE Electron Device Letters, 29(12), pp. 1408-1411.

[18] Usmani, Ali, F., and Hasan, M, 2010, "Carbon nanotube field effect transistors for high performance analog applications: An optimum design approach." Microelectronics J., 41(7), pp.395-402.

[19] Deng, J., and Wong,H. S. P., 2007, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Non-idealities and its Application—Part I: Model of the Intrinsic Channel Region," in IEEE Trans. on Electron Devices, 54(12), pp. 3186-3194.