Abstract
As there are many drawbacks of CMOS technology such as short channel effects, high power densities, hot carrier affect, decreased gate control, high sensitivity to process variation etc. A new technology called CNTFET (Carbon Nano tube Field effect transistor) has been developed to overcome the drawbacks of CMOS, which was introduced by S.Iijima in 1991 in Nano scale technology. CNTFET and CMOS have the same structure but the channel between the drain and source is replaced with carbon Nano tube. In our study, we have designed a 14 transistor full adder circuit using CNTFET technology with GDI (Gate diffusion input) technique. The GDI approach replaces the wide range of complicated logic function with only few transistors i.e. reduce the count of transistors in the digital circuit. After the designing of the circuit, results of CNTFET and CMOS has been compared using different parameters such as power delay product, propagation delay and power consumption. Simulation result has been carried out using Cadence tool Design System with VIRTUOSO platform.

Keywords: CNTFET; GDI (Gate diffusion input); Power dissipation; Delay.

INTRODUCTION
With the growth in the technology the need for scaling down has increased. The count of transistor in an integrated circuit increases for every two years approximately, this statement is known as Moore’s law. There are many false effect of scaling down in CMOS such as high power densities, drain induced barrier lowering and short channel effect[1]. To overcome these effects a new technology has been developed called CNTFET (Carbon Nano tube field effect transistor)[2]. Carbon Nanotube field effect transistor (CNTFET) is the most promising technology to extent due to three reasons: the first one is that the operation principle and the device structure of both the devices (i.e. CNTFET and CMOS) are similar, therefore the CNTFET can use the fundaments of CMOS design. The second reason is that the fabrication process of CNTFET is similar to that of the CMOS. The last reason is that the CNTFET has the current carrying ability[3]-[5].

Based on CNTFET many works have been done, some of them are arithmetic circuits, multiple valued logic circuits and interconnection networks[6]. In many VLSI system such as nano systems, microprocessor and digital signal processing system. Full adder is the basic component which is used in arithmetic circuits[7]-[8]. and the behaviour of the full adder can affect the whole system. Due to extensive use of adder cell in arithmetic function, researchers have come up with the various kinds of distinct logic styles for designing the full adder cell.

CMOS technology is widely used to design a digital circuit, but because of the increase in the demand for high speed, a new technology was developed named pass transistor technology (PTL). The advantage of using PTL is that it uses less number of transistors which leads to low power dissipation, occupies lesser area, lesser interconnection effects and lesser delay[9]-[10]. However there are two main disadvantages of using PTL that is at low power the speed of the circuit is reduced and high rate of power consumption is found. To overcome the disadvantages of PTL a new technology called GDI technology has been introduced which is implemented for low power circuits. The GDI approach replaces complicated logic function by using few transistors i.e. reduces the count of transistors in the circuit.

In our paper we are designing a full adder using Carbon Nano tube FET technology with GDI technique. The simulation result of CNTFET and CMOS is compared (parameters like propagation delay, power consumption and power delay product is also compared).

CARBON NANOTUBE FIELD EFFECT TRANSISTOR
The Nano tube is made up of a graphite sheet which is rolled up in a cylindrical manner. Based on the number of sheets in the Nanotube, it is categorized into two types i.e. Single-wall CNT (SWCNT) and Multi-wall CNT (MWCNT). The property of SWCNT could be metallic or semiconductors which will depend on the chirality vector and is define by (n1, n2) indices. These are used to determine the carbon atom angle along the graphite sheet. It n1 - n2 is not equal to 3k (for all k equal to Z) then SWCNT is known as semiconductor and if
n1 – n2 is equal to 3k (for all k equal to Z) then SWCNT is known as conductor. The channel which is used in CNTFET is semiconducting SWCNT. [11] Fig 1 illustrates CNTFET device. The gap between the two carbon nanotubes from its centre is known as pitch and the diameter of the rolled nanotube sheet is denoted as Dcnt. In CNTFET the width of the gate is determined using below equation

\[ W_{gate} = \min (W_{min}, N \times \text{pitch}) \]  

(1)

Where, \( W_{min} = \) gate minimum width

\( N = \) Number of Nanotubes

From equation (2) and (3) it is clear that by changing the diameter and wrapping vector i.e. chirality indices (n1, n2), the band gap and threshold voltage of CNTFET will differ.

\[ V_{th} = \frac{e\pi}{2e} = \frac{\sqrt{3}a\pi}{2eD_{\text{cnt}}} \approx 0.43 \frac{\text{eV}}{D_{\text{cnt}}(\text{nm})} \]

(2)

Where,

\( a = 0.249\text{nm} \) (carbon to carbon atomic distance)

\( V_{\pi} \approx 3.033\text{ eV} \) (carbon \( \pi-\pi \) bond energy)

\( e = \) unit electron charge

\( D_{\text{cnt}} = \) diameter of CNTs

The diameter of CNTs can be calculated using below equation

\[ D_{\text{cnt}} \approx \frac{\pi n_{1}^{2} + n_{2}^{2} + n_{1}n_{2}}{\pi} \approx 0.0763\sqrt{n_{1}^{2} + n_{2}^{2} + n_{1}n_{2}} \]

(3)

The three different types of CNTFET are as follows, shown in fig 2

(a) SB-CNTFET

(b) MOSFET-like CNTFET

(c) T-CNTFET

SB-CNTFET is defined as a device where the electrons are tunnelled through SB. Fabrication of CNTFET is done using direct contact of the semiconducting nanotube and metal. One of the most important disadvantages of this type is that, the ON state transconductance of the CNTFET will not be allowed by the energy barrier at SB and reduces the current delivery capability, which is directly proportional to the speed of a device.

SB-CNFETs have ambipolar property, due to which these devices are not used in CMOS logic families. This type of CNTFET is suitable for high-performance applications. To overcome the drawbacks of SB-CNFET, a new type is developed called MOSFET-like CNTFET (fig 2(b)) which would operate like normal MOSFETs but gives high performance. This type of CNTFET works on the principle of barrier height modulation by the application of the gate.
potential. One of most important advantage of MOSFET-like CNFET is that the source channel junction has no SB and therefore, it has higher ON current. As a result, MOSFET-like CNFETs is appropriable for ultra-high-performance of digital devices. The third type of CNFET is called the partially gated CNFET (Fig 2c), has very low current and high cut off characteristics which is suitable for low power applications [12]-[13]. Depending upon the mentioned merits and demerits of CNFETs, different type of CNTFETs is used.

BACKGROUND OF GDI STRUCTURE

Gate Diffusion input (GDI) a new technique of low-power digital circuit design. The GDI approach replaces the wide range of complex logic function with only few transistors i.e. reduce the count of transistors in the digital circuit. It has a simple structure which has less delay and power consumption in digital circuit. Figure 3 shows the basic cell of GDI.

![Basic cell of GDI](image)

In the structure of GDI, there are three inputs. Node G is the common input for the gate of PCNT and NCNT, node P is the input source for PCNT and N node is the input source for NCNT. Moreover output node is the drain output for both the gates i.e. PCNT and NCNT. GDI cell is known to be the most efficient methods for implementing high speed and low power logic functions and reducing the chip area[14]-[15]. Various logic function of GDI cell for different input configurations is shown in Table 1.

<table>
<thead>
<tr>
<th>N</th>
<th>P</th>
<th>G</th>
<th>Out</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>’0’</td>
<td>B</td>
<td>A</td>
<td>A’B</td>
<td>F1</td>
</tr>
<tr>
<td>B</td>
<td>‘1’</td>
<td>A</td>
<td>A’ + B</td>
<td>F2</td>
</tr>
<tr>
<td>’1’</td>
<td>B</td>
<td>A</td>
<td>A + B</td>
<td>OR</td>
</tr>
<tr>
<td>B</td>
<td>’0’</td>
<td>A</td>
<td>AB</td>
<td>AND</td>
</tr>
<tr>
<td>C</td>
<td>B</td>
<td>A</td>
<td>A’B + AC</td>
<td>MUX</td>
</tr>
<tr>
<td>’0’</td>
<td>’1’</td>
<td>A</td>
<td>A’</td>
<td>NOT</td>
</tr>
</tbody>
</table>

PROPOSED FULL ADDER CELL

1- Bit Full adder cell with three inputs A, B and C and two outputs Sum and Carry as output can logically defined as follow,

\[
\text{Sum} = ABC + AB'C' + A'BC' + A'B'C
\]

\[
= A(BC + B'C') + A'(B'C + BC')
\]

\[
= A(B \oplus C) + A'(S \oplus C')
\]

\[
\text{Sum} = A \oplus B \oplus C \tag{4}
\]

\[
\text{Carry} = AB + BC + AC
\]

\[
= AB + BC(A' + A) + AC(B' + B)
\]

\[
= AB + A'BC + ABC + A'B'C + ABC
\]

\[
= AB(1 + C) + C(A'B + AB')
\]

\[
\text{Carry} = AB + C(A \oplus B) \tag{5}
\]

![Proposed full adder cell](image)

According to the equation (4) and (5), the full adder cell can be designed using two XOR gates, two AND gates and one OR gate, which gives sum and carry collateral. The proposed Full adder cell is shown in the Figure 4.

The design consists of seven connecting pairs of GDI cell which produces carry and sum signals. In which GDI based XOR gates are connected serially to generate the sum signal. Carry is generated using the OR gates, AND gates and XOR gates.
SIMULATION RESULTS

The proposed full adder design is evaluated and compared with the CMOS based full adder. All the designs are simulated using spectre simulation model parameters with a supply voltage of 0.6V. The simulation result of CNTFET based full adder is shown in Figure 5.

Figure 5: Simulation result of proposed design

PERFORMANCE EVALUATION

The proposed circuit is simulated using 0.8V. To evaluate the performance of circuit, it is compared with CMOS circuit in term of delay, power consumption and power delay product.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>CMOS</th>
<th>CNTFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power dissipation</td>
<td>20289.6 uW</td>
<td>0.00151 uW</td>
</tr>
<tr>
<td>Delay</td>
<td>0.031 ns</td>
<td>0.0059 ns</td>
</tr>
<tr>
<td>Power delay product (PDP)</td>
<td>$6.29 \times 10^{-15}$ J</td>
<td>$8.91 \times 10^{-11}$ J</td>
</tr>
</tbody>
</table>

CONCLUSION

In this paper a new full adder circuit has been designed using CNTFET. The various parameters such as propagation delay, power delay product and power consumption are calculated for this proposed design and compared with CMOS. This has resulted in significant reduction in the propagation delay and power consumption of the full adder cell when compared to the existing model.

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REFERENCES

