A Novel Control Algorithm for DSTATCOM Based on Three-Phase Dual SO-SOGI-PLL under Non-Ideal Grid Voltage Conditions Including DC-Offset

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Abstract
This paper introduces a Novel control algorithm based on three-phase Dual Second Order - SOGI (SO-Second Order Generalized Integrator) based phase locked loop for the generation of reference source currents for DSTATCOM (Distribution Static Synchronous Compensator). In a distribution system, DSTATCOM always serves as an optimal choice for power quality compensation. The power quality (PQ) compensation under non ideal grid voltage conditions relies on the control algorithm employed. In this controller, estimation of peak value of load currents and unit template generation are done based on three-phase dual SO-SOGI. This makes the controller simpler, effective and ease of implementation in real-time applications. The proposed algorithm for DSTATCOM is aiming to perform with dynamic compensation and low computational burden under distorted / step changes in load currents, presence of harmonics, unbalance and to provide good compensation even under grid harmonic conditions, magnitude variations, frequency variations and including DC offset introduced due to A/D conversion or signal conditioning system in real-time practice. In this paper, Dual SO-SOGI-PLL is adopted because of its dynamic performance, speed and tracking accuracy under all varying and distorted conditions. The effectiveness of the proposed controller developed and tested using MATLAB/Simulink and the results found feasible and effective.

INTRODUCTION
The power generated by the conventional energy is decreasing day to day due to the depletion of resources such as coal, gas and oil etc. In the recent times, the development of non-conventional energy sources based Distributed Generation (DG) systems has fulfilled the shortage of fossil fuels. A variety of energy sources such as wind turbines, micro/pico hydro-turbines, photovoltaic arrays and battery energy storage systems are using in DG systems [1]. All these sources combine and form a DG and several such interconnections of DGs are forming as microgrids. Hence, a microgrid is a local grid comprising of several DG’s with battery energy storage and various loads operating in grid connected mode or islanded mode [2]. Various power quality issues are raised due to integration of RES to grid along with linear/nonlinear or power electronic based converter loads [3].

In distribution systems, the application of non-linear loads such as variable speed drives, fluorescent lamps and arc furnaces etc. are increasing widely and introducing harmonics and various other power quality issues into the distribution systems. The most common method of reducing harmonics and improving power factor in the system is by using passive filters. But, these are not preferred due to the drawbacks of fixed compensation, bulkiness and resonance [4]. Therefore, Custom power devices (CPD’s) such as DVR (Dynamic Voltage Restorer), DSTATCOM and UPQC (Unified PQ Conditioner) are more superior to passive filters and provide the best solution for power quality issues [5].

The magnitude of the grid voltage varies because of non-linear loads such as variable frequency drives, large motors, reciprocating compressor and arc furnaces etc. The fundamental frequency of the grid voltage also varies because of the major loss of a generating station or tie line or major
loads [6]-[7]. Due to these variations, the grid gets polluted. There are various standards which describes the characteristics of grid voltage. The Indian electricity grid code (2010) has specified a band of frequency range of 49.5 Hz to 50.2 Hz during 100% of time. Similarly, the IEC 61727 standard defines for a grid-tied PV system has a range of 49 Hz to 51 Hz and should be disconnected if the limits are exceeded [8]. IEEE 1547 standard defines for a microgrid frequency range which should not exceed 0.1% while reconnecting to the grid [9]. Standard C37.118.1 is defined for a P-Class PMU with a frequency range of 48-52 Hz and M-Class PMU of 45-55 Hz [10]. The testing frequency for power quality measurement is defined in IEC standard 61000-4-30 of a frequency range of 42.5 Hz to 57.5 Hz for a standard 50 Hz system [11]. PQ disturbances such as voltage flicker, swell, interruptions and sags are also defined in the IEEE 1159 and 1453 standards [12]. Therefore, an effective and robust computational technique is required to meet all the above mentioned standards including power quality analysis.

The aim of shunt active power filter is to compensate the harmonic current obtained by the non-linear loads. For effective control, fast and accurate tracking of fundamental and step changes in the current should be done. Therefore, a proper control strategy should be adopted and two such loops are identified. In the first loop, injected reference current should be calculated by extracting the currents and the second loop should guarantee the filter following the reference current adequately. Keeping accuracy and reliability in view, many PLL techniques are proposed in literature such as SRF-PLL, DDSRF-PLL [13], EPLL [14] and SOGI-PLL [15] etc. Every PLL has its own advantages and disadvantages and SOGI-PLL has found satisfactory under distorted conditions and has low computational burden with only one control gain associated with it. SOGI-PLL has gained much attention in grid connected systems such as grid synchronization and further SOGI-Quadrature signal generation has further enhanced as SOGI-PLL for frequency estimation [16] and for harmonic extraction MSOGI-PLL is used [17] and for symmetrical component extraction Dual SOGI-PLL’s are used and SOGI-PLL based control algorithm for shunt active power filter was developed [18]. But all these methods produce error if there is a presence of DC offset or inter-harmonics that are caused due to local loads. Therefore, A SO-SOGI PLL was proposed to eliminate DC offset and unknown harmonic frequencies (Inter-Harmonics) present in the grid voltage signal [19]

In this paper, a Dual SO-SOGI-QSG’s are used for design and development of control algorithm for three-phase DSTATCOM is implemented for harmonic mitigation, power factor correction, reactive power compensation, load balancing under unbalanced and linear /non-linear loads and under adverse grid conditions including DC offset. Three-phase PLL was designed using SO-SOGI and implemented for DSTATCOM application.

The proposed control structure has following advantages:
1. SO-SOGI is capable of detecting the grid voltage / current under balanced and unbalanced conditions.
2. Higher ability to extract the fundamental components even under adverse grid conditions and its response is faster and accurate compared to conventional SOGI-PLL.
3. The performance of the PLL is not affected with the ripple frequency, Inter-harmonics, DC offset, distortions or noise and also robust w.r.t transient and steady state disturbances.

However, the Dual SO-SOGI-PLL implementation for a three-phase DSTATCOM is reported in this paper. Various tests are carried out to test the functionality using MATLAB / Simulink.

**PROPOSED CONFIGURATION AND CONTROL ALGORITHM**

The DSTATCOM shown in Fig. 1 is a Three-leg VSC consisting of 6 IGBT switches. An interfacing inductor $L_f$ is connected across the source and load at the PCC (Point of Common Coupling). The proposed SOGI based control algorithm for DSTATCOM is capable of maintaining the THD % (Total Harmonic Distortion) within the IEEE limits. The proposed DSTATCOM is capable of handling Load balancing, power factor correction and harmonic compensation under adverse grid conditions. The ratings of the proposed system are listed in appendix. To test the dynamic performance under adverse grid and load conditions, Non-linear load (Steady increase in load) and grid disturbances (sag, swell, unbalance, DC offset and harmonics) conditions are also tested.

*Figure 1. Line Diagram of the Proposed System.*

The performance of the DSTATCOM depends on the value of DC bus capacitor. For reliable operation, the reference value of DC bus voltage should be 1.6 times more than the peak value of PCC voltage.
The proposed SOGI based controller mainly contains of peak amplitude extraction and reference source current generation using unit templates produced by the proposed PLL. Dual SO-SOGI-PLL is used to enhance the power quality under adverse grid conditions and distorted load conditions.

A. SO-SOGI-PLL

This subsection introduces a basic SO-SOGI functionality and its application in the proposed controller. If the grid voltage signal has distortions, harmonics and noise, then a filter is required to eliminate the effect in the phase tracking. The SO-SOGI acts as an adaptive filter which generates orthogonal signals even under grid distortions. The block diagram of SO-SOGI quadrature signal generation and PLL are shown in Fig.2 and 3 respectively.

\[ W = \text{Input Sinusoidal Frequency} \]
\[ \zeta = \text{Damping Factor} \]

In general, two low-pass filters are used to eliminate the ripple produced across the DC link voltage and at estimating the peak currents. These two filters are also eliminated because of using SO-SOGI-PLL for estimation.

B. Estimation of Unit Voltage Templates

Fig.3 shows the closed loop block diagram of Dual SO-SOGI-PLL. Three-Phase PLL is used to generate required in-phase and quadrature templates separately. The output phase angles (U_a, U_b, U_c) that are generated from the SO-SOGI-PLL are considered as unit templates.

C. Reference Current Generation

The peak amplitude of active component of current is calculated similarly as shown in fig. 3. I_{Lab} is supplied to SO-SOGI based quadrature signal generation for estimation of peak load current. The voltage (V_{dc}) across the DC bus capacitor is compared with the V_{dc*} (reference DC bus voltage) and the error signal is passed through a Proportional-Integral Controller to regulate the DC bus voltage. The error of the signal is given by:

\[ V_{loop}(n) = V_{dcref}(n) - V_{dc}(n) \]

The error is then supplied to PI controller to regulate the voltage of DC bus of DSTATCOM. The output of the PI controller is given by:

\[ I_{of}(n) = I_{of}(n-1) + k_p [V_{loop}(n)] + k_i V_{dcref}(n) \]

Where, k_p and k_i are gains of PI controller.

The average magnitude of current (I_p) and the output of the PI controller (I_d) are summed up (I_p=I_p+I_d). Finally, the resultant active component of current is multiplied with the unit templates (U_a, U_b, U_c) that are generated by the grid voltage to generate three reference source currents. These three estimated three-phase reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) are compared with the source currents sensed at the point of common coupling (i_{sa}, i_{sb}, i_{sc}) to estimate the error in currents. The error currents generated are supplied to a PWM controller to generate PWM gating pulses for DSTATCOM as shown in Fig. 4.

\[ i^*_{sa} = I_p^* U_a, i^*_{sb} = I_p^* U_b, i^*_{sc} = I_p^* U_c \]
SIMULATION RESULTS AND DISCUSSION

In this section, the improved control algorithm is evaluated and tested using MATLAB/Simulink on a three-phase distribution system loaded with linear and non-linear loads as shown in Fig. 1. Fixed time step of 10µs with ode1 (Euler) solver is chosen for simulation.

In the test cases mentioned below, the load currents and source voltages are distorted and unbalanced. If the source voltages become distorted then the unit templates generated by the distorted signals produce erroneous outputs. To overcome this limitation, a SO-SOGI based PLL is used which acts as adaptive filter in distorted conditions and produce an exact result within the shortest period of time. Once the outputs generated by the SO-SOGI are obtained, the commands are then supplied to generate reference source currents as shown in Fig. 4.

Some of the below test cases are chosen in the simulation. Source Voltages, Source Currents, Load Currents, Injected Currents, Estimated Peak Current and DC link Voltage are observed.

1. Performance of the proposed system with ideal grid conditions and with DSTATCOM under balanced Non-linear Load (Fig.5).
2. Performance of DSTATCOM with ideal grid conditions and Un-balanced linear non-linear loads (Fig.6).
3. Ideal grid conditions with sudden increase of loads (Fig.7).
4. Un-Balanced Voltage sag is introduced in the grid voltage (Fig.8).
5. Harmonics injected (5th & 7th) into the grid voltage (Fig.9).
6. DC offset (10%) is produced in the grid voltage (Fig.10).
7. A Frequency step of 5 Hz is introduced in the grid voltage (50Hz to 55Hz) (Fig.11).

Figure 4 Proposed Control Algorithm based on Dual SO-SOGI

Figure 5 A Steady Non-Linear Load is applied.
Figure 6 Unbalance in Load is applied.

Figure 7 Sudden Increase in Load is applied.
Figure 8  Un-Balanced Voltage Sag is applied.

Figure 9  Harmonics injected into the grid voltage.
Figure 10. DC offset is produced in the Grid Voltage

Figure 11. Frequency Step (50 to 55 Hz) is introduced in the Grid Voltage

CONCLUSION
In this paper, a simple and effective DSTATCOM is implemented for three-phase distribution system with an improved control algorithm based on Dual SO-SOGI PLL has been analyzed, presented and validated using MATLAB / Simulink. This theory is adopted to work in ideal and adverse grid voltage conditions. The source current is maintained within IEEE limits 519-1992. This algorithm is tested under load current and grid voltage conditions including grid harmonics, frequency step change and dc offset and found satisfactory under reactive current and harmonic compensation. The DC bus voltage is also regulated within the limits under varying and distorted conditions to avoid unbalancing problems and power losses.
REFERENCES


### APPENDIX (Table-II)

<table>
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<th>AC supply source &amp; Frequency</th>
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<td>diode bridge rectifier</td>
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<td>Linear Load</td>
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<td>PWM Switching frequency</td>
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<td>Interfacing inductance</td>
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<td>DC bus gains of PI controller</td>
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### THD (%) of Test Cases (Table-I)