Compact Design of Buck Based FPGA Topology for Battery Charging System

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Abstract
This paper describes compact design of buck based FPGA topology for battery charging system. It comprises different blocks like flyback converter, buck converter, FPGA, ADC. Flyback converter uses 230V as input and gives 36V at the output. Output of flyback converter used as input for LM2596 buck converter to produce 12V output for charging battery. Buck converter is triggered by pwm pulses supplied by cyclone IV EP4CE22F17C6 FPGA. FPGA enhances computation capability of digital controller. Current sensor measures battery charging current through one of the eight ADC channels. Battery operates in three modes such as trickle current, constant current and constant voltage with different protections like over voltage, under voltage, over current, short circuit protection and thermal protection. Simulated waveforms of buck converter and RTL schematic in FPGA for ADC and pwm are given.

Keywords: CC-CV, CLB, EV, FPGA, PWM

Introduction
Nowadays, portable personal telecommunication systems have increased such as mobile telephones and laptop computers, electric vehicles etc. demands various batteries. These equipments often used secondary batteries due to its cost effectiveness over the lifetime of the product. Battery charger accuracy is very much important in manufacturing because charging process decides battery quality. If the same quality batteries are charged at 1A for an hour using a charger with 1% accuracy, there is a difference of 30~40 seconds in charging time. In this case, quality of battery cannot be classified [1]. Determining battery state is the first stage to minimize charging time. For this, memorizing of battery charging and discharging history, measurement of internal impedance are the methods to be followed as these methods are not practical [4].

Conventionally, charger system design was proposed by microprocessor based digital control scheme. Advantages of these schemes were flexibility, higher reliability and lower cost. FPGAs are utilized because microprocessors suffer from tremendous computation load due to excess demand for advanced charging algorithm. The high speed hard-wired logic of FPGA can enhance the computation capability of the digital controller. Advantages of FPGA are elegant hardware, higher computation speed and short period of timing for prototyping. In addition, the circuit is very compact because whole system may be implemented in only a single FPGA chip [5].

To meet all these requirements, FPGA based battery charger is developed which is compact and efficient. This charger system consists of different blocks like fly back converter, buck converter, FPGA, ADC. Fly back converter takes 230V AC supply and produces 36V output which is given as input to buck converter. Buck converter is triggered by pwm pulses from Cyclone IV EP4CE22F17C6N FPGA to give desired buck output for battery charging. Battery operates in three modes i.e. trickle charge, constant current and constant voltage. Over voltage, under voltage, over current are different protections would be obtained along with short circuit protection and thermal protection from proposed system.

This paper organizes as, section I- introduction, section II- Circuit Description, section III- Result, section IV- Conclusion and section V- References.

Proposed System
Figure1 shows the block diagram of buck based fpga topology battery charging system. It uses different blocks like Power supply, Bridge rectifier, Switched Mode Power Transformer, Large filter capacitor, Startup resistors, Power FET, Run DC circuit, Diode and filter capacitor, Sampling/Error detection circuit, Optoisolator feedback and most important FPGA.

![Block Diagram of the proposed buck based FPGA topology battery charging system.](image)
Design and Analysis

The schematic of proposed charger system is shown in figure2. It consists of 36V DC 50W, a trivial low-cost off-line SMPS switching power supply circuit. It provides a nominal 36V DC output at more than 4A load. This output gives an input to step-down (buck) converter, capable of driving 3A load and produces 30VDC. Buck converter is triggered by pwm pulses given by Cyclone IV FPGA. Battery is connected to buck converter which operates in three modes like trickle current, constant current and constant voltage. Line and load regulation is better than 0.5%. The unit has over current, over temperature and overvoltage protections, as well as passive inrush current limiting. Output ripple are approximately 0.2 V peak to peak in the range 0 to 20 MHz.

Table 1: Parameters for 12V DC-DC switching converter

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>36V</td>
</tr>
<tr>
<td>Vref</td>
<td>1.23V</td>
</tr>
<tr>
<td>Vout</td>
<td>30V</td>
</tr>
<tr>
<td>Iload</td>
<td>3A</td>
</tr>
<tr>
<td>R1</td>
<td>1kΩ</td>
</tr>
<tr>
<td>R2</td>
<td>( R_2 = R_1 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) )</td>
</tr>
<tr>
<td>L</td>
<td>((\text{Vin} - \text{Vout}) / (D/Fsw) / \text{Iripple}))</td>
</tr>
<tr>
<td>C</td>
<td>(C = (\Delta I \Delta T) / [\Delta V - (\Delta I \text{ESR})])</td>
</tr>
</tbody>
</table>

Experimental Setup

Buck converter is modeled in simulink as below and its simulated waveform shown in figure 4.

Figure 2: Schematic of proposed buck based FPGA topology for battery charging system.

Figure 3: Model for buck converter

When the switch (MOSFET) in the buck regulator is on, Vin - Vout is the voltage that appears across the inductor. The current in inductor will rise at a rate of \((\text{Vin} - \text{Vout})/L\), using the inductor equation. This time the diode does not conduct because it is reverse biased. The inductor works to keep the same current flowing, a current must still flow when the switch opens. So current is flowing from the inductor and load. Idiode equal to Iout is formed as return path with diode, D when current flowing through it. The current through the inductor decreases with a slope equal to \(-\text{Vout}/L\) because polarity of the voltage across the inductor has reversed due to switch in open position.

Figure 4: RTL schematic of PWM in FPGA.

Figure 5: RTL schematic of ADC in FPGA

Figure4 and Figure5 show the Register Transfer Level schematic of pwm and adc respectively in FPGA which is also often referred as preoptimized design. After the synthesis process of the synthesis phase, the HDL schematic is generated.

Figure 6: Hardware setup of proposed system
Observation

Figure 7: Simulated current waveform for compact design buck converter.

Figure 8: Simulated voltage waveform for compact design buck converter.

Figure 9: Simulated waveform for PWM

Simulated waveform for pwm is shown in figure9. It takes 50MHz internal clock with period of 20ns. Output of pwm pulses shown with 50% duty cycle.

Figure 10: Simulated waveform for ADC

To measure the output of current sensor eight ADC channels are used and its results are shown in figure10. Using 50MHz clock, when signals iGO = 1 and iRST = 0, output data is generated and its output will display on led.

Conclusion

A compact design of buck based FPGA topology for battery charging system for batteries was presented. In order to monitor the operating parameters during charging/discharging processes, a verilog program was also developed. The proposed charger system can operate in trickle current, constant current and constant voltage charging mode; the voltage or duty cycle command can be set by the user using the designed program in FPGA. The proposed charger system features the following advantages such as compact design, low output voltage/current ripple, high efficiency and digital programmability. Moreover, FPGA solutions are especially suitable for situations where time to market, cost and size are important constraints. Through recording the battery voltage, current and temperature, the influence of the previous battery charge and discharges in the battery capacity; the influence of the charging strategy and the actual battery charge state in the efficiency and speed of the charge process can be further investigated.

References


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