Abstract
Inductors are a necessary building block in many circuits, including LNA and oscillators largely used in Receivers and various other systems. Because planer inductors can occupy a large amount of area in integrated-circuit (IC) designs, the search has been on for smaller, tunable inductors suitable for monolithic fabrication. In this paper, a method, which is to implement an active inductor by CMOS active devices, has been presented. For this purpose, four designs are presented using various topologies along with their simulation results. Few designs gave low to moderate values of inductance, associated capacitance and also noise figure obtained is well within the range of 1 dB with low offered resistance.

Keywords: CMOS, Active Inductor, Tunable Inductor, parasitic.

Introduction
Present day communication need for good designs and high quality of results. For this purpose inductors and capacitors are applied as an integral part of circuit which in turn provides satisfactory tuning of frequency. Planer inductors occupy large silicon area and since metal layers are used for their design they dissipates energy which is undesirable. Hence potential of Active Inductors can be used to remove these problems. The main advantages of active inductors include the higher quality-factor, reducing chip area, and potentially tunable characteristics as a need for high quality, various inductor designs are compared. Subsequent sections describes various active inductor topologies with their advantages and remedies in design, if any. Section 4 gives the list of measurements done followed by detailed discussion on simulation results and conclusion.

To differentiate between various inductors for RFIC applications, categorization of inductors can be done in following way:

a) Spiral Inductor
b) Active Inductor

Spiral Inductor
Passive spiral inductors are mainly used in the VCO component design because spiral inductor have a high Q factor, which will let the VCO have a better phase noise performance. Passive spiral inductors are implemented using the two highest metal levels available from the process technology file. An equivalent lumped model of the spiral inductor can be seen as follows.

From figure 2 it can be explained that Rs and Ls represent the series resistance and inductance of the metal line, which can be determined directly by real part and imaginary part of measured one-port S-parameter. The Cp represents the coupling capacitance between port 1 and port 2, and the Cox illustrates the parasitic capacitance from metal line to silicon substrate. The rest components, Csub and Rsub, stand for the substrate parasitic effects.

Calculations of inductance alone are not sufficient to represent the inductors. It is also imperative to consider the...
associated parasitics in the inductor, to fully represent them. Even though passive spiral inductors have a high Q factor, they take up a lot of chip area and are very complicated to design.

**Active Inductor**

**1. Inductor Topologies (Design and Calculations)**

*a) Tunable Active Inductor-1*

Active inductor has low-Q on-chip as compared to spiral inductors. For monolithic RFIC applications, the design of the active inductor using gyrator is practiced and shown in Figure.Here $g_1, g_2, C_1,$ and $C_2$ are parasitic conductance and capacitance, respectively. $Gm_1$ and $Gm_2$ represent transconductors and are connected back-to-back to form a gyrator.

![Figure 3: Gyrator Circuit](image)

The input admittance of the gyrator circuit, $Y_{in}$, is shown as follows:

$$Y_{in} = 1/Z_{in} = g_1+sC_1+(G_{m1}G_{m2})/sC_2+g_2$$

The active inductor reported in [1] is implemented in this paper and modified according to the available tools and analysis. The circuit diagram is given in figure 4.

The third term in above equation of $Y_{in}$ behaves as an inductor with resistive loss. Based on (1), the active inductor can be modeled as a resonator. The inductance can be tuned by varying $C_2$, while $Q$ of the active inductor can be tuned by varying $C_3$. This inductor is used in [1] for IRLNA, thus it can be used for LNA and VCO also, which will effectively reduce the occupied area.

*b) Tunable Active Inductor-2*

This design uses the effective ground provided. Also the design uses internal parasitic of the applied transistors, and has very good response in terms of sensitivity and Q-factor at high frequency.

![Figure 5: Grounded Active Inductor](image)

![Figure 6: GAi with resistive feedback](image)

The input impedance is given as

$$Z_{in} = (1/r_{o1}+s(C_T+C_{gd2}))/((A.s^2+B.s+C)$$

Where

$$A = C_T (g_{st1}+C_{gs2})+C_{gs1}C_{gd1}$$

$$B = C_T (1/r_{o1}+1/g_{m1}+g_{m2})+g_{m2}C_{gd2}+C_{gd1}/r_{o2}+C_{gs1}/r_{o1}$$

$$C = g_{m2}/r_{o2}+g_{m1}/r_{o1}+g_{m1}/r_{o2}$$

and $C_T = C_{gs2}+C_{gd1}$. 
Adopting an assumption, \( s(C_T + C_{gd2}) > g_m >> 1/r_o \), above equation can be simplified the input impedance of GAI as following equations. From this, we can conclude intuitively that the inductance and \( Q \)-factor of the conventional GAI is determined by the typical parameters of transistor \( M_1 \) and \( M_2 \). Therefore

\[
Z_{in} = \frac{s(C_T + C_{gd2})/g_m}{g_m} = sL
\]

And \( Q = \frac{\omega L}{R} = \frac{\omega [C_T + C_{gd2}]/(C-w2A) - (B/r_o)]}{[\omega 2(B+C_{ds2}+(C-w2A)/r_o)]}
\]

It can be seen that \( Q \)-factor is proportional to \( g_{m1} \), although the inductance value is inversely proportional to \( g_{m1} \) and that \( Q \)-factor can be decreased by increasing \( C_{gs2} \). We can find that \( Q \)-factor is changed dynamically by the effect of parasitic capacitance of \( M_2 \) at high frequency.

c) Tunable Active Inductor (Improved)

Active inductors are implemented based on the well known gyra-C architecture consisting of two transistors in feedback generating inductive impedance. The grounded active inductor topology is a common topology used to implement high-\( Q \) CMOS tunable active inductors (TAls). To enhance the inductance and \( Q \) of this active inductor, the introduction of a tunable feedback resistance, \( R_f \), has been shown in Figure below. The tunable feedback resistance increases the effective inductance, \( L_{eff} \), and decreases the equivalent series resistance simultaneously, which enhances its \( Q \). The tunability has also been improved as all the 3 parameters: \( L_{eff} \), \( Q \) and the frequency with maximum \( Q \), \( f_Q \), can be tuned independently. Detailed analysis of the grounded TAI suggests a direct trade-off between the achievable range of tunable inductance, quality-factor and the output noise that calls for an optimization guideline. From the gyrator-C architecture and the noise analysis, the dependence of \( L_{eff} \), \( f_Q \), and the output noise on the design parameters is given as

\[
L_{eff} \propto \frac{R_f}{g_{m1}g_{m2}}, \quad f_Q \propto \frac{1}{\sqrt{R_f}} \quad \text{and} \quad \text{Noise Voltage} \propto \sqrt{g_{m1}g_{m2}R_f}
\]

Where \( g_{m1} \) and \( g_{m2} \) are the small-signal transconductances of the transistors \( M_1 \) and \( M_2 \) shown in Figure below. Since \( g_{m1} \) and \( g_{m2} \) are related to each other from the expression for the effective dependence on \( g_{m1} \) can be eliminated. Higher feedback resistance also decreases the frequency of maximum \( Q \), i.e., the frequency of operation. On the other hand, the range of tunable inductance increases with the range of the tunable feedback resistance [1]-[2]. This leads to a direct trade-off between the range of tunable inductance and the frequency of operation on one hand, and low-noise performance on the other. Thus, to achieve wide tunability and high frequency operation along with low output noise, the design parameters need to be optimized.

d) Tunable Active Inductor - R tuned

Here the resistance \( R_f \) is controlled by a pair of MOSFETs. Transistor \( M_2 \) is used to enhance the Quality factor, Inductance etc.

e) Differential Active Inductor
It is a differentially configured gyrator-C active inductor in a simplest geometry, and the same structure is chooses in this paper. Lower Transistors are biased in the triode region and behave as a voltage controlled resistors whose resistances are controlled by the gate voltage \( V_{b2} \). All other transistors are biased in the saturation.

**Different Measurements**
Different measurements carried for the characterization of Active Inductors are as follows:-

(a) Resistance  
(b) S11, S22  
(c) RMS Value of Noise Voltage  
(d) Noise Figure  
(e) Inductance  
(f) Capacitance

All these measurements were carried using Micro Wave Office from AWR. Different parameters were evaluated and plotted. These results evaluate the performance of designs.

**Simulation Results**

**(A) Active Inductor -1**

![Figure 10: Simulation Results for Active Inductor-1](image)

**(B) Tuned Active Inductor -2**

![Figure 11: Simulation Results for Tuned Active Inductor-1](image)

**(C) Tuned Active Inductor (Improved)**

![Figure 12: Simulation Results for Active Inductor-Improved](image)
D) Active Inductor – R Tuned

Figure 13: Simulation Results for Active Inductor-R Tuned

Summary of Results

Table 1: Summary of Results for various Topologies

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AI 1 This Work</th>
<th>Ref</th>
<th>AI 2 This Work</th>
<th>Ref</th>
<th>Improved This Work</th>
<th>Ref</th>
<th>R Tuned This Work</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise Figure (dB)</td>
<td>High</td>
<td>With LNA</td>
<td>1.085</td>
<td>-</td>
<td>1.0944</td>
<td>-</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>Capacitance (pF)</td>
<td>1.4785</td>
<td>Do</td>
<td>6.22</td>
<td>-</td>
<td>3.007</td>
<td>0.131</td>
<td>6</td>
<td>-</td>
</tr>
<tr>
<td>Inductance (mH)</td>
<td>Low</td>
<td>Do</td>
<td>Moderate</td>
<td>High</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>V High</td>
</tr>
<tr>
<td>S11/S22 (dB)</td>
<td>-1.596e-10/-562</td>
<td>Do</td>
<td>-1.06/-0.075</td>
<td>-</td>
<td>-0.5/-0.55</td>
<td>-</td>
<td>-0.129</td>
<td>High</td>
</tr>
<tr>
<td>RMS Noise Voltage (v/√Hz)</td>
<td>1.596e-10</td>
<td>Do</td>
<td>4.4e10-11</td>
<td>-</td>
<td>4.7e10-11</td>
<td>-</td>
<td>-</td>
<td>3e-09</td>
</tr>
<tr>
<td>Resistance (Ohm)</td>
<td>V low</td>
<td>Do</td>
<td>0.22</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>250</td>
<td>1K</td>
</tr>
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</table>

Conclusions

It can be seen that with the use of CMOS Technology, here 0.18um, active inductor can be designed for various receiver circuits. The results shows that considerably low noise figure is obtained in association with low and moderate values of inductance and capacitance. Active inductor design – Improved gives the satisfactory results, which was the goal of this research paper. Future work includes the preparation of layouts for suitable design and comparison of pre and post layout simulations.

References