Implementation and Reconfiguration of Basic Digital Modulation and Demodulation Techniques on FPGA

B. K. V. Prasad\textsuperscript{1}, P. Satish Kumar\textsuperscript{2}, B. S. Charles\textsuperscript{3}, R. Sai Priya\textsuperscript{4}

\textsuperscript{1}ECE Department, KL University, Vijayawada, Vaddeswaram, Green Fields-522502, Andhra Pradesh, India.

Abstract
In modern communication systems the Autonomous modulation and demodulation technique is done using proper signal detection schemes and prominent receiver structure. The implementation of BPSK, FSK, ASK modulation and demodulation techniques are created in Simulink which is converted into Xilinx core and this further undergoes changes using system generator module. The modulated signals obtained from these simulations are compared with the obtained signals after implementation. The FPGA was programmed with the help of ARM processor to compile the bit files to select the best modulation that has best channel support. The interface is done between the controller (STM32) and FPGA (xc3s500e-256) using JTAG. The XSVF format and synopsis programmed files are stored in the SD-card of the microcontroller. The HyperTerminal displays the output corresponding to the selected modulation. The optimum modulation is selected based on available bandwidth, bit-error-rate and signal to noise ratio. Hence, Among available tools for FPGA design, System Generator is a system-level modeling tool that provides better quality of service, system complexity, power efficiency, bandwidth efficiency and cost effectiveness, more secure, reliable and efficient compared to the analog communication.

Keywords: Xilinx, BPSK (Binary phase shift keying), ASK (Amplitude Shift Keying), FSK (Frequency Shift Keying), Simulink, System Generator, FPGA (Field Programmable Gate Array).

INTRODUCTION
Digital Communication Signals
It is the process of varying the properties of a periodic waveform known as carrier signal with a modulating signal that typically contains information to be transmitted\cite{1}. It is the process of super imposing the information contents of a modulating signal on a carrier signal by altering its characteristics according to the given modulating signal. Digital modulation is the process by which symbols are transmitted into wave forms that are compatible with channel characteristics\cite{1}. A Base band signal is converted in to band pass signal by modulation. To recognize the signal at the end demodulation process is used. This paper utilizes MATLAB simulink and system generator for simulation and implementation on spartran-3e FPGA board which involves flexibility for designing and testing that makes development very easy. It also provides flexibility of increasing the design and testing speed with in limited given time.

TYPES OF DIGITAL MODULATION
BPSK:-
In Binary Phase Shift Keying (BPSK) only one sinusoidal wave is taken as the basis function. Modulation is obtained by changing the phase of this basis function depending on the given message bits. If 1 was transmitted the modulated signal remained unchanged i.e, the same as carrier i.e, with 0\degree initial phase. If 0 was transmitted the modulated signal changed 180\degree phase. This modulation is the most robust of all the PSKs since it takes the highest level of noise or distortion to make the demodulation reach a wrong or invalid decision. Thus it, however, can modulate only at 1 bit/symbol and so is unsuitable for high data-rate applications

\[
\begin{align*}
S_0(t) &= A \cos(\omega t + 0) \quad \text{represents 0} \\
S_1(t) &= A \cos(\omega t + \pi) \quad \text{represents 1}
\end{align*}
\]

Demodulation must be accomplished by recognizing the signals at the receiving end. To demodulate the signal at the receiver side, it is necessary to reconstruct the carrier. This process is made in the Carrier Recovery Circuit. Next, the BPSK modulated signal is multiplied with the carrier, pass through an integrator and then decision circuit will give the modulating signal at the end.

Figure 1: BPSK modulation.
ASK:-
Amplitude-shift keying (ASK) is a type of amplitude modulation that involves representation of digital data as the changes in the amplitude of a carrier wave. In an Amplitude Shift Keying modulator, the binary symbol 1 is represented by transmitting a fixed-amplitude carrier wave and fixed frequency for a bit duration of N seconds. Here the strength of carrier signal is varied to represent binary 1 or 0. Both frequency & phase remain constant while amplitude changes, commonly, the amplitude decreases when zero transmits.

FSK:-
It is a type of frequency modulation that involves representation of digital data as the changes of frequency of a carrier wave. To transmit a message signal for a certain long distance its frequency is modulated using carrier wave. Here both the phase and amplitude of the modulated wave remain unchanged and the respective frequencies for different logic values gets changed. In case of positive ASK for logic 1 of message signal modulated wave gets more frequency and for logic 0 its frequency decreases.

To design a demodulator with maximum and minimum frequency of fMAX and fMIN, respectively (which is same as that of modulator), the following steps are required: 1. Use the same value of R1 and C1 as that of modulator. 2. While using PC1, the capture range depends on the LPF (R3-C2) characteristics and can be made as large as the lock range. For PC2, capture range is equal to lock range and is independent of the LPF. 3. Since leakage current can affect the VDEMOUT, a load resistor (R5) from this pin to GND in the range of 50 kΩ to 300 kΩ is recommended.

METHODOLOGY
System Generator is a DSP tool from Xilinx based on the Matlab/Simulink environment and is used for FPGA design. System Generator is actually a library in Simulink which translates a Simulink model into a hardware realization of the same model. It also maps the system parameters defined in Simulink into entities and architectures, signals and ports in the hardware realization Only the subsystems and blocks from the Xilinx Block set are translated by System Generator into hardware realization.

In order to program the FPGA, two distinct software packages are used: Matlab and Xilinx ISE. Matlab/Simulink is the software where the system functionality is verified and where the programming takes place and ISE is where the program will be configured to run on the FPGA. The connection that is involved between the two packages is System Generator, a part of Matlab, which converts the Simulink math code into VHDL code that is recognized by the ISE software.

Simulink Blockset
Pulse Generator: It involves a train of pulses.
Sine Wave: It generates sine functions.
Scope: Oscilloscope used to compare and see the results.

System Generator Blockset
Mcode: It calls a Matlab. m file and executes it.
Gateway In: It makes an approach to the representation of a signal behavior in hardware.
Gateway Out: it returns an approach of the signal behavior in hardware to that of simulation mode.
Mult: It performs the multiplication of its two inputs.
System Generator: It provides control of the system and simulation parameters. It is used to call and execute the generated code.
FDATool: Filter Design and Analysis tool.
Resource Estimator: in the simulation of circuit the resources used are represented.
Figure 5: System generator.

**Modules of System generator**

**DDS Compiler:**
This block is used for generating the carrier waveform multiplexing in order to modulate the given message signal. Depending on the type of modulation there properties varies; like in case of BPSK 2 DDS compilers each with a phase difference of 180 degrees are generated. Multiplex depending on the input supplied to the selection line it selects whether a positive or negative sine should be supplied as a carrier.

**Random source:**
As the message signal is an analog source in real time in this system generator it is supplied using random source generator. Rounding function is a module that is used for cutting off the amplitude decimals.

**Scope:**
Here for the purpose of viewing the generated output and in order to compare it with the supplied inputs a two way scope is considered.

**AWGN :**
As the real time transmission lines are not error free. This awgn module is added in the system generator for making the signal obtained after multiplexion as noise effected.

**Digital filter design:**
After the process of completion of transmission the filter is used for purpose of removing the signal noise. Depending on the type of filter more error free signal can be obtained.

**Mcode:-**
This block is used for the purpose of converting the transmitted analog in to digital signal and after which digital signal recorded can be displayed on the scope.

**DESIGN MODELS AND SIMULATION HARDWARE IMPLEMENTATION**

Figure 6: DDS Compiler

Figure 7: Hardware Implementation
RESULTS

**BPSK Implementation:**

![BPSK Modulation](image1)

*Figure 8: BPSK Modulation.*

![Software output waveform](image2)

*Figure 9: Software output waveform*

![Hardware output waveform](image3)

*Figure 10: Hardware output waveform*

**BPSK Demodulation Implementation**

![BPSK Demodulation](image4)

*Figure 11: BPSK Demodulation.*

![Software output waveform](image5)

*Figure 12: Software output waveform*

![Hardware output waveform](image6)

*Figure 13: Hardware output waveform*
**ASK Modulation Implementation**

**Figure 14:** ASK modulation

**Figure 15:** Software output waveform

**Figure 16:** Hardware output waveform

**ASK Demodulation Implementation**

**Figure 17:** ASK demodulation

**Figure 18:** Software output waveform

**Figure 19:** Hardware output waveform
FSK Modulation Implementation:

Figure 20: FSK modulation

Figure 21: Software output waveform

Figure 22: Hardware output waveform

FSK Demodulation Implementation:

Figure 23: FSK demodulation

Figure 24: Software output waveform
These figures show the hardware and software waveforms for BPSK, ASK, and FSK modulations and demodulations using Xilinx System Generator.

**HARDWARE CO-SIMULATION**

After connecting all the required blocks for modulation in system generator VHDL is automatically generated for the designed block diagram. Using JTAG the generated blocks can be implemented on the Spartan 3e kit and the inputs to this are the same inputs supplied in the block design. Using this hardware block is generated for the software block design made. Both the results can be cross checked and will be same and can be viewed using the scope connected as outputs for the JTAG block.

**Implementation and Results of Reconfiguration Process**

Matlab Simulink with the Xilinx System Generator is a system level modelling tool that facilitates FPGA hardware design. System Generator extends Matlab/Simulink in order to provide a powerful modelling environment that is well suited to hardware design by providing logic cores that may be directly implemented in logic. The tool also provides access to FPGA resources through lower level abstractions, allowing to rapidly implement and test highly efficient real-time FPGA designs.

Using Xilinx block set the construction of different blocks for various modulations is done. The generation of verilog code done and then this is interfaced with the hardware kit FPGA &STM32 by JTAG. The output signal from FPGA is fed as input digital to analog converter (DAC) and the respective reconfigured output is observed in the memory card as output.
Figure 29: Hardware output

Figure 30: ASK modulation reconfigured output

Figure 31: ASK modulation reconfigured output from CRO

Figure 32: FSK modulation reconfigured output

Figure 33: FSK modulation reconfigured output from CRO

Figure 34: BPSK modulation reconfigured output
CONCLUSION

Digital modulation is less complex, more efficient and most secure in very long distance transmission. The noise detection and correction is more efficient in digital modulation than analog. Only one FPGA chip is used for implementation without the need for reconfiguration process which increases the detection time. Because of the usage of FPGAs, the design can have low power consumption, small size and involves less cost. In this project, BPSK and ASK systems with modulators has been designed and tested. While testing the detector, the delay in the recovered data at the output of the detector is observed, and it is found that the delay is due to the computational delay of multiplier block (mux). The results given by the development board (hardware) exactly matches with the results obtained from simulation setup (software). From the above results it may be concluded that the entire result given by the development board is same as that of the result obtained from the simulation setup implemented. Simulink tools and System Generator involves a simplified environment for the simulation of the systems in general. The results obtained in hardware are since dependent on the design of it in software, it is much easier to carry out changes in these results by means of the software in case if necessary, even after having finished design and its implementation. This statement considered as one of the most important factor in the development of this type of design.

REFERENCES


