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Reconfigurable With Multiprecision Multiplier For Fir Filter For Fetal Ecg Implementation

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Abstract

This paper is a realization of reconfigurable with multiprecision multiplier to act as a major component in Finite Impulse Response (FIR) filter for the real time implementation of fetal Electrocardiogram (ECG) segregation from maternal ECG. As the accuracy and precision are the important parameters in the design process of filtering. A reconfigurable multiplier is designed with single as well as double precession. The Multiplier is able to perform one 16-bit X 16-bit multiplication and three 8-bit X 8-bit multiplications with the help of control mode. A divide and conquer approach is applied to the multiplier architecture for the multiplication of higher bits values. The proposed multiplier has been designed in ModelSim Altera 10.1 and parameters are compared with help of Cadence Encounter 6.1.5 the results shows an area reduction 22% then the conventional multiplier. An FIR filter is designed with the proposed multiplier for real time application. A real time ECG wave of fetal and maternal is extracted and segregation of the both is performed with the designed FIR filter. The results are significant the designed filter is able to extract the wave then the conventional filter and is less complex in implementation then the existing ones.

Keywords— Cadence Encounter, ECG, fetal, maternal.

I. INTRODUCTION

Fetal Electrocardiogram (ECG) is information of fetal heart rate and abstraction of this piece of information requires the ECG of the maternal (mother). As the maternal

ECG compromises of both mother and fetal ECG, segregation of both the ECG requires filtering process. Filtering process will be digital as the current trend of the century is digital processing of signal (DSP). DSP is incomplete without multipliers as they come in use in almost every application; all the arithmetic computation in DSP requires multipliers. Since power consumption and performance becomes the bottle neck for VLSI designer.

A real time implementation of an ECG requires accuracy and precision these are the two most important parameters in the design. Precision multipliers deal with the word length optimization [1]. [1] Least Mean Square (LMS) equalizer has been used for optimal word length implementation for each modulation, In order to achieve power/performance ratio scaling, transistor level technique was proposed. Though the technique of using variable data width solution achieved an optimal word length implementation with good power efficiency, it also contributed to performance penalties.

Power consumption in multipliers is also contributed due to switching activity. As dynamic switching takes most of the power in the multiplier [2], a latch adder technique with leap frog structure has been implemented to overcome the spurious switching. The circuit adds delay even with array based architecture. In order to overcome the problem, [3] pipelined architecture with truncation method has been used to avoid unnecessary transition problem. Here Least Significant part [LSP] is eliminated and the product is obtained with the most significant part [MSP] and mid-point significant part [MMP]. Here trading of precision take place with power optimization. The multipliers not only have power optimization related issues, they also have word size optimization problem. So far realisation of a multiplier is done with truncation of least significant product where precision is compromised.

For intelligent reuse of architecture reconfigurable circuits are designed. In [4] a multiprecision (MP) reconfigurable multiplier is designed with Dynamic Voltage Scaling (DVS) with error correction mechanism. Although the multiplier severs the purpose for low power application, realisation is complex. Filtering of signals requires efficient multiplier as stated the real time implementation such as ECG estimation requires efficient design which requires accuracy and precision. Many filters have existed till now to extract the information of fetal ECG, in [5] Adaptive Noise cancelling (ANC) technique with neural network FIR filter extracts the fetal ECG from Maternal ECG, it lacks in robustness. Further approaches to this adaptive filtering is using mean square method which can be least or recursive, as these methods are efficient for bio signal and wireless signal extraction. An efficient hardware and software implementation of QR-decomposition recursive least square (QRD-RLQ) algorithm has been used in [6] & [7] with folding technique in the architecture, the architecture provides low power and cost. The realisation is computationally complex.

In this paper we are proposing a multiplier which is reconfigurable and multiprecision and is realised on an FIR filter to extract the fetal ECG from the maternal ECG. The multiplier designed here provide three 16-bit products and one 32-bit product, with the use of control signal we can obtain either products. Intelligent reuses of the circuit provide reconfigurabilty which has a major role in FIR filter at

the time of convolution. The realised circuit is tested with real time signal such as maternal ECG which requires separation of mother and fetal ECG. The paper has following section II Overview of the circuit and operation, III Reconfigurable and Multiprecision multiplier, followed by IV Implementation of realised multiplier in FIR filter, then real time implementation of the realised circuit for V Fetal ECG extraction from maternal ECG, VI Conclusion.

II. OVERVIEW OF THE CIRCUIT AND OPERATION

Fetal ECG extraction from maternal ECG requires different modules inorder to obtain desired waveform.

A. Reconfigurable and Multiprecision Multiplier

The multiplier is designed to provide two different bit multiplication products with a reconfigurable architecture with the help of mode of control signals. The architecture has a processing element (PE) module to speed up the calculation process, inorder to make the multiplication fast.

B. Impelmentation of Multiplier in FIR filter

The multiplier is implemented in FIR filter with 6 tap to check the functionality of the circuit. As the multiplier plays an important part of the filter, the idea is to reduce the computation of the circuit with efficient results.

C. Realisation of real time ECG signal

The designed FIR filter is tested with real time signal. So far the circuit are tested with test signal to check the overall functionality of the circuit. Here we are taking a real ECG signal and checking whether the designed architecture is able to segregate the Fetal ECG from the maternal ECG. Fig 1 shows the overall architecture required for the segregation of the ECG signal.

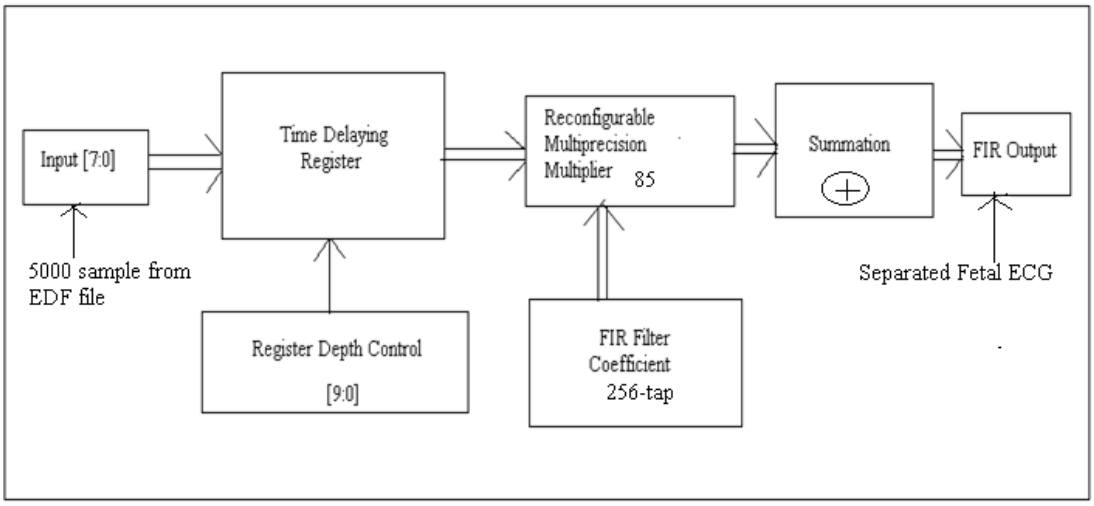

Fig. 1 FIR filter with reconfigurable with multiprecision multiplier architecture.

III. RECONFIGURABLE AND MULTIPRECISION MULTIPLIER

The multipliers which are present today offer challenging task for the designers in term of power consumption, speed and area the overall functionality of the design. In order to maintain the compactness and functionality many architectures and algorithms are presented. The most common multiplication existing today is "add & shift" algorithm. In order to speed up the multipliers operation partial product has been reduced.

In Fig. 2 a reconfigurable structure of multiplier is present which provide one 16 X16 bit multiplication and three 8 X 8 multiplications. Using three PE modules we are able to obtain three 16-bit products and with divide conquer approach we are able to obtain one 32 bit product. The multiplier has no garbage values. Since the precision has to be maintained we can obtain precision values of 16 bit and 32 bit.

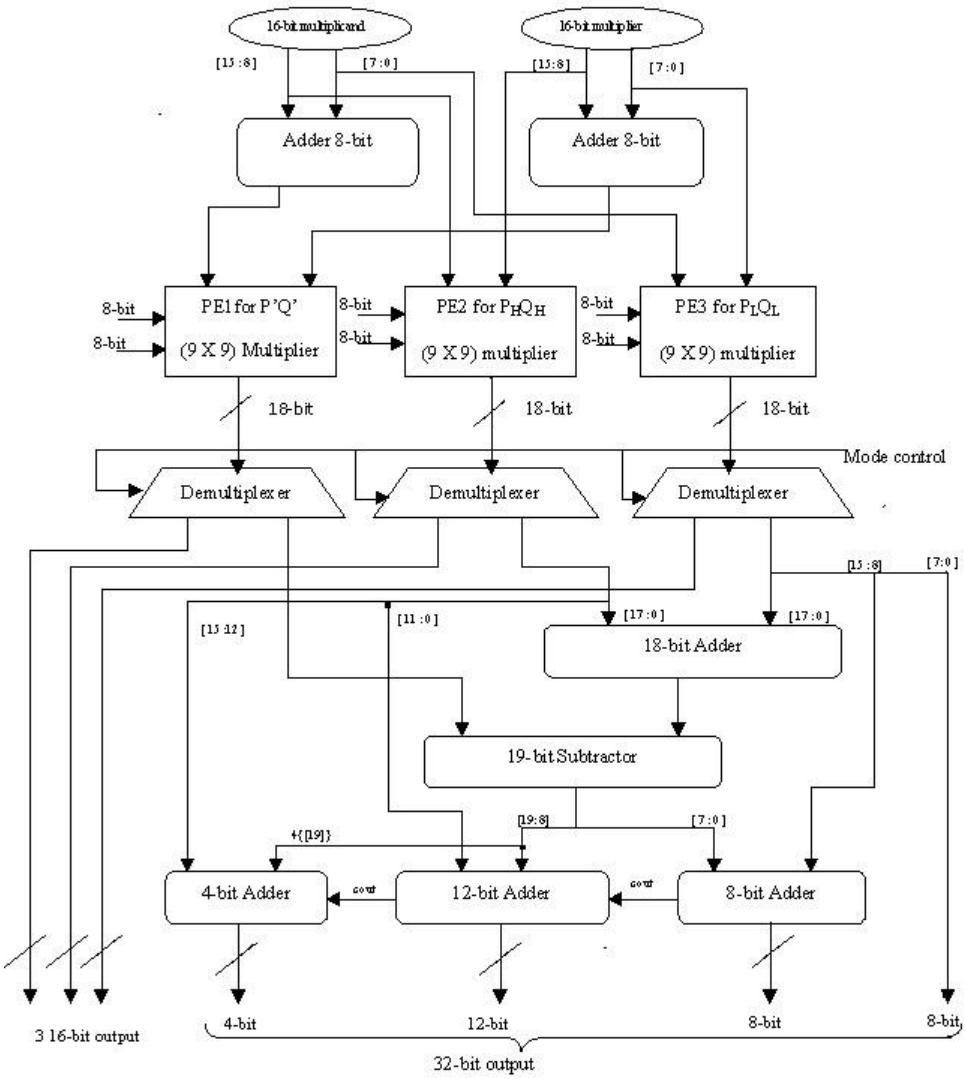

Fig. 2 Reconfigurable with Multiprecision multiplier architecture.

Inorder to evaluate the reconfigurability and MP, we consider the multiplicand A and the Multiplier B each with 2n bit wide in terms of wordlength [4], the 2n-bits wide multiplicand P and 2n-bits wide multiplier Q, where P_HQ_H is their respective most significant bits (MSB) and P_LQ_L are the least significant bits (LSB) and P_HQ_H , P_HQ_L, P_LQ_H , P_LQ_L these are the respective crosswise products of the multiplication. The product can be given by

$$\text{Product} = (P_HQ_H)\, 2^{2n} + (P_HQ_L + P_LQ_H)\, 2^n + P_LQ_L \quad (1)$$

From equation (1) it can realised that in order to implement the product for 2n-bit reconfigurable multiplier we require four n-bit X n-bit multiplier to compute P_HQ_H , P_HQ_L, P_LQ_H , P_LQ_L and three 2n-bit adders, If we define [8],

$$P' = P_H + P_L \quad (2)$$

$$Q' = Q_H + Q_L \quad (3)$$

From eq. (2) & (3) we can re-write eq. (1) as the by multiplying eq. (2) & (3) and rearranging the product term of eq. (1) we can obtain

$$\text{Product} = (P_HQ_H)\, 2^{2n} + (P'Q' - P_HQ_H - P_LQ_L)\, 2^n + P_LQ_L \quad (4)$$

Now if we compare equation (1) and (4), eq. (4) allows us to remove the multiplication and addition of P_HQ_L and P_LQ_H with the removal of one n X n multiplier and one 2n-bit adder. We are using two n-bit adder for $P_H + P_L$ and $Q_H + Q_L$ and one subtractor 2n+2 bit for $P'Q' - P_HQ_H - P_LQ_L$. For further reduction in the calculation process we are going to use three PE blocks which uses booth Radix 4 Wallace tree structure.

A. ***Processing Element (PE)***

- The entire architecture uses three processing elements (PE). Each PE has booth radix-4 multiplier with Wallace tree structure [8].
- The multiplier has a booth encoder (BE) and booth selector (BS).The BE decodes the multiplier signal and the output of it is given to BS to generate the partial product. The partial products are then added with Wallace tree structure. The Wallace tree structure is a carry save adder (CSA), the final sum is given to carry look ahead adder (CLA).
- The algorithm is well suited for booth signed and unsigned number multiplication. Here k-bit binary number is interpreted as k/2-digit Radix-4 number.
- The BE has precoded values which are then multiplied with the multiplicand to generate partial product.
- Wallace tree makes the accumulation of the partial products to speed-up. Wallace tree compromises of three CSA and one CLA. The Wallace structure

consists of 3:2 compressor techniques, which means that it will take 3 inputs and 2 outputs.

These three PE produces 9 X 9 bit multiplication product of P'Q', P_HQ_H, P_LQ_L, which goes further into the architecture for final output. It also takes separate 8 X 8 bit inputs for producing an output of 16 bit product from each PE with help of demultiplexer by giving a mode of control signal. With mode of signal '0' we can obtain three 16 bit products and with mode of signal '1' we can obtain one 32 bit product. The reconfigurablity of this architectures helps to get different bit products from the demultiplexer. The multiplier is designed in ModelSim Altera 10.1 and the parameters are analyzed in Cadence Encounter 6.1.5. The parameters evaluated are given in Table I. The results obtained shows 22% of reduction in area.

TABLE I AREA AND POWER COMPARISON OF THE EXISTING AND PROPOSED MULTIPLIER

Architecture	**Power (mW)**	**Logic cell**
Existing Multiplier (Fixed 32-bit width)	0.08	1267
Proposed Multiplier (32-bit width)	1.06	980
Proposed Multiplier (16-bit width)	1.06	980

IV. IMPLEMENTATION OF REALISED MULTIPLIER IN FIR FILTER

An FIR filter is designed with the proposed multiplier, to check the functionality of the multiplier to work within a filter. The FIR filter is designed to perform a real time application such as fetal ECG extraction from the Maternal ECG. As the signal strength of fetal ECG is weaker than that of maternal ECG and the frequency is greater for child than the mother, it is therefore required to have a filter which can segregate the signals effectively. Fig 3 shows the architecture design of FIR filter.

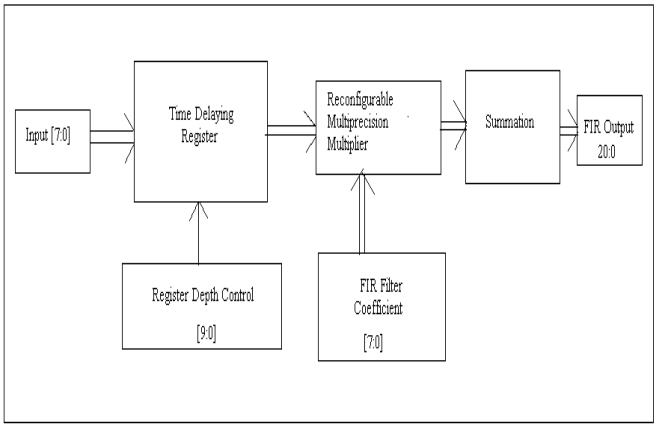

Fig. 3 FIR filters architecture with the proposed reconfigurable with multiprecision multiplier.

The reconfigurable and multiprecision multiplier is used in 6-tap FIR filter. To evaluate the simulation and verify the performance ModelSim Altera 10.1 tool has been used and the parameters are analysed in Cadence Encounter 6.1.5. The FIR filter has been designed for 256 tap also, as the segregation of signal requires more than 256 tap for experimental purpose we can obtain the results with 256-tap, the simulation and verification is performed in ModelSim Altera 10.1 and parameter analysis is performed in Cadence Encounter 6.1.5. Table II contains the parametric results from Cadence.

TABLE II AREA AND POWER COMPARISON OF 6-TAP FIR FILTER AND 256 TAP FIR FILTER

Architecture	Power (mW)	Logic cell
6-Tap FIR Filter	2.8	7391
256-Tap FIR Filter	81.5	314410

V FETAL ECG EXTRACTION FROM MATERNAL ECG

The application of the designed FIR filter with reconfigurable multiplier is to be used in fetal ECG extraction. So far there are many circuits proposed like [5],[6]&[7] . Each of which has its own advantages in extracting the signal and disadvantages like lack in robustness and realization is also computationally complex. The designed FIR filter takes real time ECG signals not any test signals, as the whole idea is to realize a real time signals.

Extraction of Fetal ECG involves extracting a real signal from the database of European Data File (EDF) and converting those signals into a binary format which can be used by ModelSim Altera 10.1 as inputs. The Conversion of the EDF file is done with the help of MATLab tool. This EDF file is the input to the FIR filter. The Database mentions that there are 3,00,000 samples in the EDF file which has been taken from 6 channels which are the electrodes connected to the mother for obtaining the ECG signal. The ECG of the mother is dominant then the fetal ECG signal. These different channels are there to get the better signal from anyone of the electrode.

The file is converted into binary format with the help of MATlab. With the help of Filter Design and Analysis (FDA) tool, we can obtain the filter coefficients for the filter. The filter is designed with low pass filter for 256-tap with f_{PASS} 1000 H_Z and f_{stop} 1500 H_Z. The generated text has been used in Modelsim. The input ECG signal extracted from the EDF file in MATLAB is shown in Fig.6. The input waveform is stored in binary format in a form of text file which can be called in ModelSim.

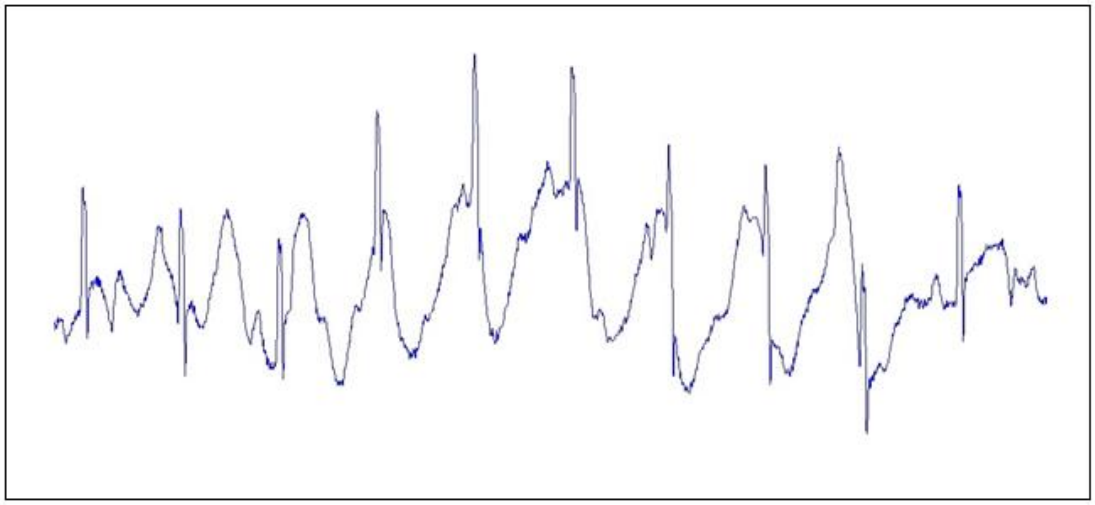

Fig 6 Input ECG signal of mother and child extracted from the EDF file.

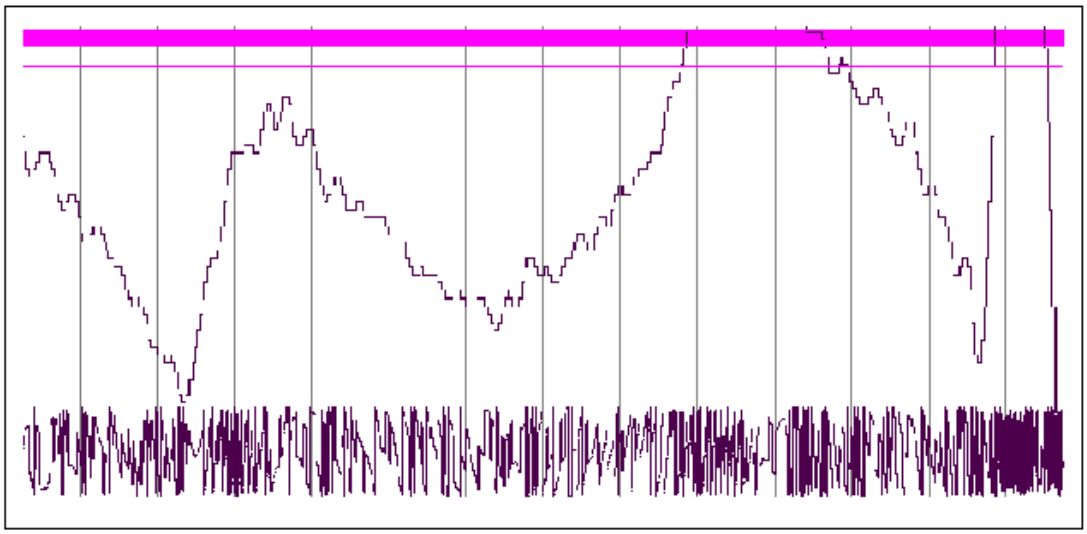

Fig 5 Segreated Fetal ECG from Maternl ECG.

The FIR filter is used to segregate the fetal ECG from maternal ECG from 256 tap FIR filter . To get the exact analysis we need 700 to 1000 –tap FIR filter for expeimental analysis we got it through 256-Tap FIR filter. The Filter inputs are the 5000 samples taken from channel 1 of the EDF file and the filter coefficients are the 256 values obtained from FDA tool. The designed FIR filter is able to extract the fetal ECG with the given input values. Fig 5 shows the segregated fetal ECG from the base Input signal.

VI CONCLUSION

A reconfigurable and multiprecision multiplier is designed for an FIR filter. The Multiplier uses three PE having Booth Radix-4 with Wallace tree structure and divide and conquer approach for obtaining the higher bits multiplication product. The proposed multiplier has an area reduction of 22% by compromising the power for precision. The proposed multiplier is used in the FIR filter. The filter is designed for 6-tap to check the functionality and 256-tap to be used for real time implementation. The FIR filter takes a real time signal of maternal ECG from which the fetal ECG has to be extracted, as the maternal ECG is dominant to fetal ECG. The FIR filter with reconfigurable multiprecision multiplier is able to extract the fetal ECG from maternal ECG.

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