International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 8 (2015) pp. 20475-20488

http://www.ripublication.com

Multiple Parametric Faults Detection In Linear Analog Circuits Based on Test Vectors and Statistical Threshold

G. Puvaneswari[1], S.UmaMaheswari[2]
[1]*Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore-641 014, India. puvana1977@gmail.com*
[2]*Department of Electronics and Communication Engineering, Coimbatore Institute of Technology, Coimbatore-641 014, India.*

Abstract

A method for multiple parametric faults detection in analog circuits using test vectors and statistical threshold is proposed in this paper. The circuit under test (CUT) is simulated using Modified Nodal Analysis (MNA) method and from the knowledge of circuit topology and component values, the test vectors associated with each component are derived. The test vectors are generated for nominal value, upper bound and lower bound values of the components to solve tolerance issues and sensitivity of the test vectors to component values in real time faults detection. A simple mean based statistical threshold technique is used to detect faulty components in the circuit under test. Simulation results of benchmark circuits illustrate the proposed method and validate its effectiveness in identifying multiple parametric faults in linear analog circuit.

Keywords: analog circuits – modified nodal analysis- test vector – fault diagnosis – tolerance – threshold

Introduction

Testing of analog circuits became an important task due to non availability of standard models and procedures. Various proposed research works in the field of analog circuit testing show that the factors like nonlinearity of circuit components, tolerance and the number of test nodes to locate the faulty elements, limit the development of standardized methods for testing. Generally faults are classified as soft (parametric faults) and hard (catastrophic) faults. The soft or parametric faults are due to variation in component values and the hard faults are due to open and short circuits. Hard faults lead to complete change in system performance which could be easily detected where as soft faults do not cause complete change and difficult to detect. Different methods have been proposed to detect single and multiple soft faults in analog circuits. In [1], a mathematical model based on normalization algorithm to

reduce the dimension of the fault samples and to improve the accuracy and efficiency of fault diagnosis is proposed. Neural network based fault diagnosis method is proposed in [2]. The structure and training methods of LVQ neural networks are presented and it has been proved to be a simple and effective practical method. In [3], neural network based parametric fault diagnosis in analog circuit using Polynomial Curve Fitting is proposed to cover faults as small as 10% or less. A polynomial of suitable degree is fitted to the output frequency response of an analog circuit and the coefficients of the polynomial attain different values under faulty and non faulty conditions. Using these features of polynomial coefficients, a BPNN is used to detect the parametric faults.

A method to detect and identify the faults, taking into account the deviations of the circuit parameters within their tolerance ranges is developed in [4]. The method uses fault dictionary for preliminary identification of the faults and the verification is based on the linear programming approach. Regarding to the complexity and diversity of analog circuit fault, a principal component analysis(PCA) and particle swarm optimization(PSO) support vector machine(SVM) analog circuit fault diagnosis method is proposed in [5]. It uses principal component analysis and data normalization as preprocessing, then reduced dimension fault feature is put into support vector machine to diagnosis, and particle swarm optimization is used to optimize the penalty parameters and the kernel parameters of SVM, that improve the recognition rate of the fault diagnosis. In [6], test point selection approach based on the fault pair Boolean Table technique is proposed. With this a near optimum test point set selection was achieved and it is applicable for both soft and hard fault cases. The soft faults and hard faults are located using slope fault model. The node equation between two nodes is expressed by a point-sloe form equation in which the point is determined by the nominal voltage values on the two selected nodes, and the slope which is invariant, is used as the fault model. The parameter tolerance is also taken into account while testing. In [7], single fault diagnosis is performed with multiple test frequencies. Testing is done with the consideration of component's tolerance. The CUT is simulated using modified nodal analysis and the equations are solved using the linear system solver with Lower and Upper triangular decomposition. Testability vectors are found for all the circuit components. The testability vectors form the fault dictionary to diagnose the faults in the CUT. Single faults are injected into the CUT and the faulty circuit is simulated. The tool calculates the fault variable for each test frequency and finds the average, standard deviation and coefficient of variation of the real and imaginary parts of the elements. The sum of the cumulative coefficients of variation for each element is calculated and the lowest one indicates the diagnosed faulty element. The proposed approach generates test vector as in [7] but provides solution for real time testing and a method to detect multiple soft faults.

In the following sections, detailed procedure to detect multiple faults has been explained. Section 2 describes the mathematical fundamentals for generation of test vectors. Section 3 illustrates the test procedure. Section 4 deals with the results obtained from the proposed work on the bench mark circuits. Section 5 explains the challenges in real time fault diagnosis and proposed solution & Section 6 deals with the discussion on the proposed approach. Section 7 concludes. .

Mathematical Fundamentals

Analog circuit test procedure begins with the simulation of the CUT and deriving the diagnosis variables such as node voltages and branch currents. The simulation of an electronic circuit involves formulation of the circuit equation and solving it for the unknowns. To simulate the CUT, Modified Nodal Analysis (MNA) is used. MNA uses the voltage, current relationship of the circuit components and the KCL [9, 10]. It handles voltage sources effectively by an unknown current through it and adds it to the vector containing unknown node voltages. MNA for linear systems results in the system equation of the form

$$AX = Z \tag{1}$$

where A is the coefficient matrix, X is the unknown vector consists of circuit variables (node voltages and few branch currents) and Z is the excitation matrix. The circuit coefficient matrix is formed by the sub matrices,

$$A = \begin{bmatrix} G & B \\ C & D \end{bmatrix} \tag{2}$$

G is the conductance of the components in the CUT and the values of G are determined by the interconnections of the circuit components. B and C matrices consist of 0, 1,-1 and the values are based on the interconnections of the voltage sources. The D matrix is developed with zeros for independent sources and has nonzero values for dependent sources. The X matrix with variables useful for the diagnosis is formed by the node voltages and the unknown currents through the sources. The right hand side matrix (Z) consists of the values of independent current and voltage sources. The unknown vector is found by decomposing the coefficient matrix using singular value decomposition and then solving the set of equations. Faults in the CUT are simulated using Fault Rubber Stamp (FRS) [7- 10]. FRS is based on the MNA stamp of the components of a CUT. The MNA stamp of a component C_n connected in between the nodes j and j' (V_j , V_j'- respective node voltages) ,in the coefficient matrix is,

$$X = \begin{bmatrix} V_n \\ I_v \end{bmatrix} \tag{3}$$

$$Z = \begin{bmatrix} I \\ V \end{bmatrix} \tag{4}$$

$$\begin{array}{c} \\ j \\ j' \end{array} \begin{array}{c} \begin{array}{cc} V_j & V_j' \end{array} \\ \begin{bmatrix} +C_n & -C_n \\ -C_n & +C_n \end{bmatrix} \end{array} \tag{5}$$

If this component is assumed to be faulty, its value changes from C_n to $C_n \pm \Delta$. This deviation causes the current through that faulty component to deviate from its nominal value. This current deviation called fault variable (ϕ) is introduced in the faulty circuit unknown matrix as an unknown branch current. To indicate the current deviation through the faulty component, the faulty component is represented as a parallel combination of its nominal value and the deviation (Δ) (fig.1). V_j and V_j' are the node voltages at the nodes j and j' respectively. i_f is the current deviation through the faulty component.

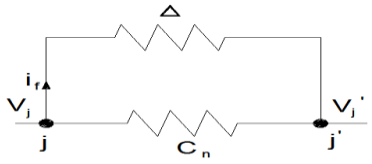

Figure 1: Faulty Component Representation

The fault rubber stamp [12] for the component C_n is,

$$\begin{array}{c} \\ j \\ j' \\ \\ f \end{array} \begin{array}{c} \begin{array}{cccc} V_j & V_j' & & i_f \end{array} \\ \left[\begin{array}{cccc|c} +C_n & -C_n & \vdots & & 1 \\ -C_n & +C_n & \vdots & & -1 \\ \cdots & \cdots & \cdots & & \cdots \\ \hline 1 & -1 & \vdots & & -\Delta^{-1} \end{array}\right] \end{array} \tag{6}$$

The bottom row line is the faulty component equation and the right most column corresponds to the extra fault variable. As seen in (6), for each faulty component there is an additional column at the right side and row at the bottom of the coefficient matrix is introduced. The faulty system with the FRS in matrix form is,

$$\begin{bmatrix} A & c \\ r & \Delta \end{bmatrix} \begin{bmatrix} X_f \\ \phi \end{bmatrix} = \begin{bmatrix} Z \\ 0 \end{bmatrix} \tag{7}$$

where c and r are the additional column and row introduced corresponding to a faulty component. The additional column c indicates the location of the faulty component. The additional row r is the faulty component equation with its node voltages. The value of Δ depends the faulty value of the component. It can be observed that a new variable called fault variable (ϕ) is also introduced as unknown into the unknown vector matrix (X_f) of the faulty circuit. It can also be noted that this fault variable is the unknown branch current. As seen in (7), the coefficient matrix (A) of the nominal circuit is retained in forming the faulty system equation without any modification in the values of it. Thus from (7), the faulty circuit equations are written as,

$$AX_f + c\phi = Z \tag{8}$$

$$rX_f + \Delta\phi = 0 \tag{9}$$

replacing $Z = AX$ from (1),

$$AX_f + c\phi = AX \tag{10}$$

$$A(X - X_f) = c\phi \tag{11}$$

$$X - X_f = A^{-1}c\phi \tag{12}$$

$$X - X_f = T\phi \tag{13}$$

$$\phi = (X - X_f)/T \tag{14}$$

$$T = A^{-1}c \tag{15}$$

The product $A^{-1}c$ is a complex column vector and it is called testability vector [7]. As c describes the location of a component in the CUT, the testability vector is associated to that component and the values are independent of the faults. Thus the fault variable which can be obtained by the element wise division of the difference vector (difference between the nominal and the faulty solutions) and the test vector is also associated to a specific component in the CUT. It is also observed that the element wise division leads to same values in the column of the fault variable matrix. This is shown in fig. 3 for a Sallen key BPF. But it can also be observed that the test vector depends on the circuit component values which limit the applicability of this method in real time. Hence a method to solve this issue is proposed in this paper.

Test Procedure

The test process begins with the development of test vector and then the diagnosis. The test vectors for all the components in the CUT are obtained by (9-15). The CUT with the nominal component values is simulated and the solution vector (X) is obtained. Faults with different values are injected into the CUT and the solution vector (X_f) is found. The fault variable matrix ϕ is obtained from (14) and found to have same column value for the faulty element.

Diagnosis Variables Selection & Ambiguity Set Determination

The diagnosis variables used for identification of faulty elements are selected based on the test vector values. The diagnosis variables with same test vectors must be avoided as this limits the diagnosability of the components. The ambiguity sets can be determined as in [7]. Two or more circuit components belong to same ambiguity set if a fault cannot be resolved between them. Ambiguity sets can be located with test

vectors. Two elements belong to same ambiguity group if and only if their test vectors are equal. This leads to the requirement of careful selection of test variables.

Illustrations

The efficiency of the proposed work is validated through benchmark circuits like Sallen key band pass filter and Linear Voltage Divider circuit. The operational amplifiers and the sources used are assumed to be fault free.

Sallen Key Band Pass Filter

The CUT with its nominal value is shown in fig. 2. The circuit equations are assembled using MNA as mentioned above. A column vector (c) corresponding to the location of each component is derived and the test vector as in (15) is calculated for all the components.

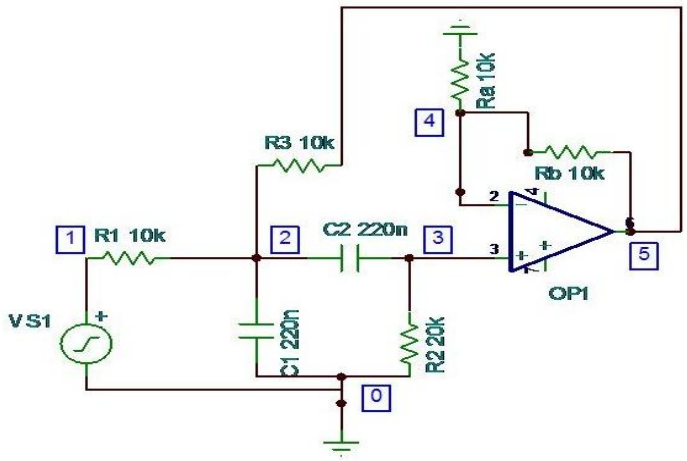

Figure 2: Sallen Key Band Pass Filter

Testing is performed at the frequency 1 KHz with the signal strength 10V. The components are assumed to be with 5% tolerance. Multiple faults with different values are injected into the CUT using a fault generator and the fault variable matrix is found. Testing is done with the diagnosis variables V_5, Ii, Io, (output voltage at node 5, current at node 1 and current in the amplifier output node 5). The diagnosis variables are selected as per the discussion in section 3.1. Result for four fault case is shown in fig.3. The column values (Y-axis) are in logarithmic scale.

Four fault case

Four faulty components, with the values are R_2 = 20011Ω, R_3 = 10120Ω, R_a = 10064Ω, R_b = 9788Ω injected into the CUT. The results are displayed in the figure 6. From figure 3, it can be understood that the diagnosis variables are same in values for R_2, , R_3, R_a,, R_b. Hence these elements are faulty elements.

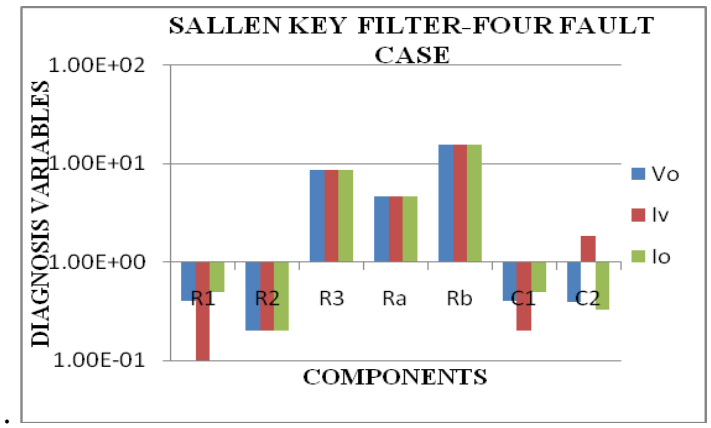

Figure 3: Fault variables (Four fault)

Real Time Fault Detection

Figure 3 shows the result for four faults case and it can be observed that the column values are same for faulty elements. But from equation (15), it can be observed that the test vector is sensitive to the circuit component values (A is the circuit component matrix). In real time fault diagnosis, the nominal value of the component itself is not the same as simulation due to tolerance and this leads to variation in column values and affects the fault diagnosis procedure. To solve this issue, a new approach has been proposed. Assuming that the circuit topology and knowledge on the component values and tolerances is known, the test vectors are generated for nominal values, upper bound and lower bound values of the components of the circuit under test.

The test procedure consists of two phases. In the first phase or pretesting stage, the test vectors are generated for the nominal, upper bound and lower bound values of the components of CUT and stored. Figures 4 to 6 show the test vectors for the corresponding diagnosis variables of Sallen key BPF & figures 8 & 9 show the test vectors for Linear Voltage Divider. Figure 7 shows the Linear Voltage Divider with the nominal values. The second phase begins by applying test signal, measuring the diagnosis variables and estimating the difference between the diagnosis variables with nominal values and the diagnosis variables of the CUT. The CUT is said to be fault free if this difference is a zero vector else faulty. To identify faulty components, the fault variable matrix as explained in (14) is estimated. The fault variables corresponding to the diagnosis variables are extracted. The mean deviation is obtained for each column (associated with the components in CUT) and mean value (threshold) is found from all the columns. A component is said to be faulty if the estimated mean deviation is less than or equal to the threshold. The flow diagrams (figures) 10 & 11 explain this.

In the testing stage, multiple faults with different strength is injected into the CUT and the diagnosis variables corresponding to the fault case are measured (X_f). The fault variable matrix associated to the specified fault condition is obtained by (14) with nominal, upper bound and lower bound test vectors. The mean value of

magnitudes of fault variable matrix is estimated and deviation from the grand median (overall median) is also obtained. The threshold value is obtained. Tables (I & II)show the results for Sallen key BPF and Linear voltage divider circuit. Table shows the deviation value only for faulty elements. The threshold obtained and the mean deviation values are scaled by 0.001.

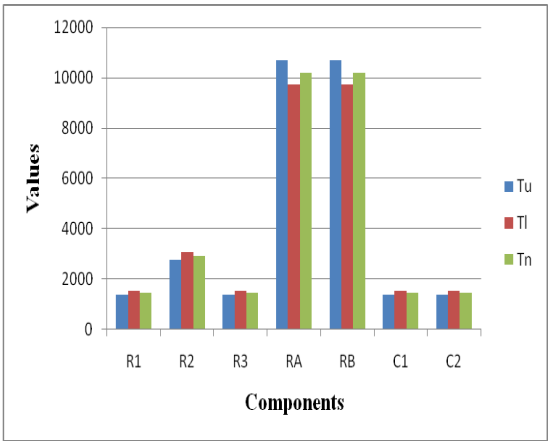

Figure 4: Test Vectors of Sallen Key BPF(V_5)

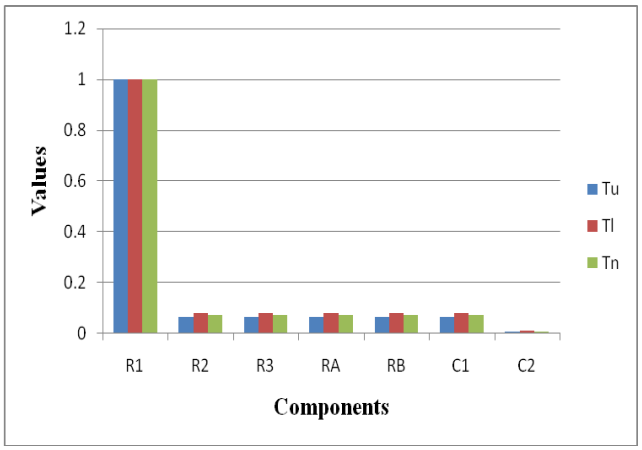

Figure 5: Test Vectors of Sallen Key BPF(Ii)

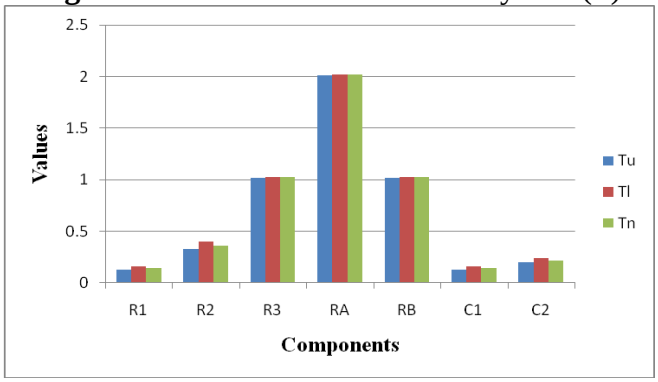

Figure 6: Test Vectors of Sallen Key BPF(Io)

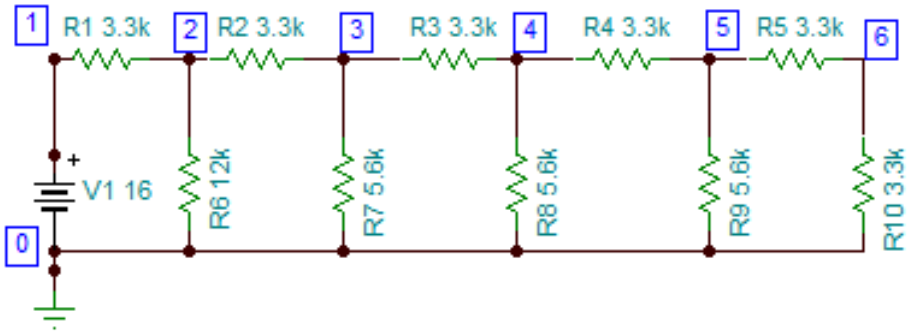

Figure 7: Linear Voltage Divider

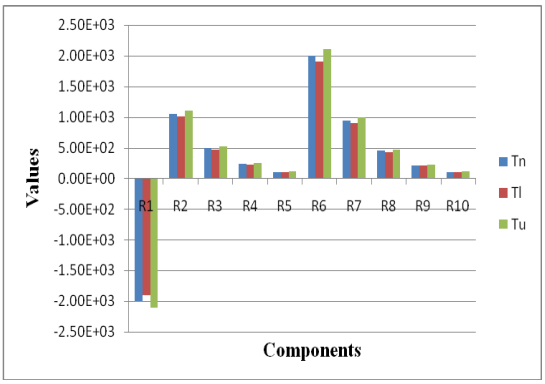

Figure 8: Test Vectors (V_6)

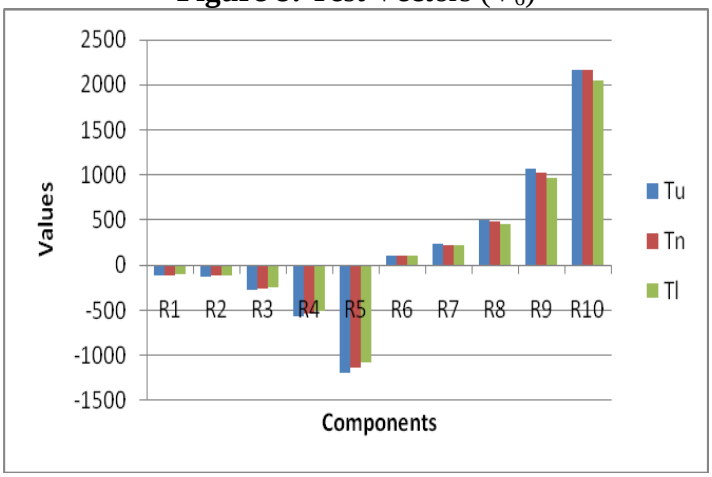

Figure 9: Test vectors (V_2)

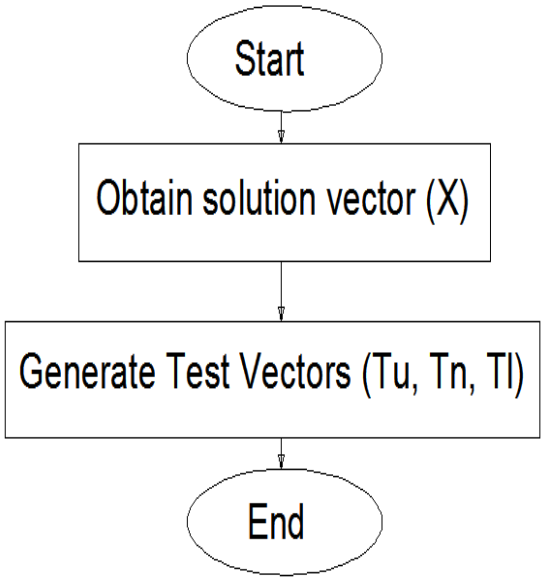

Figure 10: Pre-testing stage (real time diagnosis)

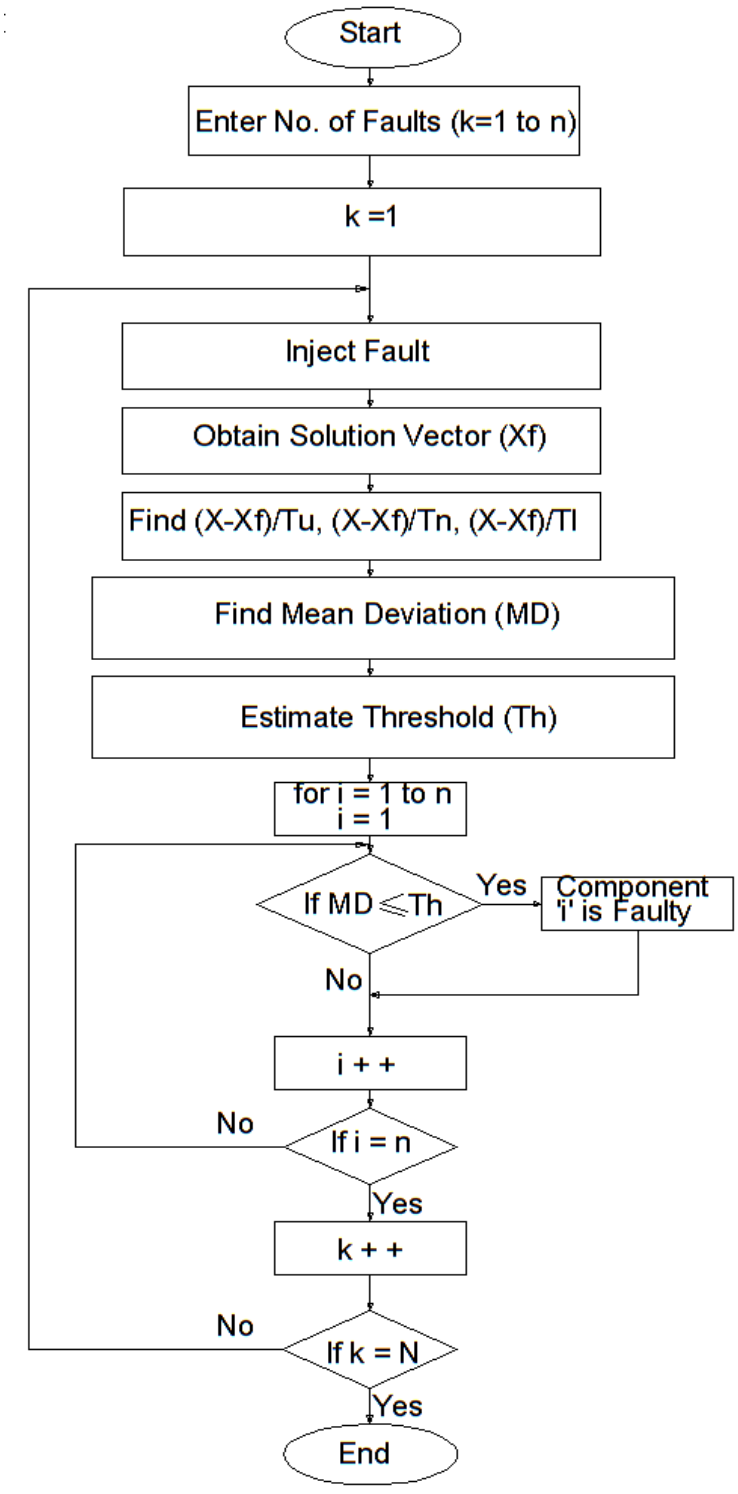

Figure 11: Testing stage

Table 1: Results for Sallen Key BPF

CUT	**Faulty Component & Value**	**Magnitude of diagnosis variables**	**Threshold**	**Mean Deviation obtained for faulty components**
Sallen Key BPF $V_{5,N}$ = 1.44V $Ii_{,N}$ = 1mA $Io_{,N}$ = 72.2 µA	R_1 (10730Ω) R_3 (10820Ω) C_1(330nF)	V_5 = 0.898V Ii = 0.9mA Io =0.0449mA	0.167	0.0145 0.167 0.153
	R_1 (5kΩ) R_a (17k Ω) R_b (6k Ω) C_2 (110nF)	V_5 = 1.93V Ii = 1.98mA Io =83.9µA	9.41	0.779 9.39 9.31 9.37
	R_1(17k Ω) C_1(350nF)	V_5 = 533.04mV Ii =587.82 µA Io =26.64 µA	2.53	0.0878 2.37
	R_2 (30k Ω) R_3 (4500 Ω) R_a(3k Ω) C_1 (400nF)	V_5 =1.31 Ii =1.01mA Io =131.06 µA	-0.069	-0.069 -0.145 -0.65 -0.169
	R_3(22k Ω) C_2(100nF)	V_5 =1.42 Ii =994.84 µA Io =71.12 µA	0.031	0.031 -0.98

Table 2: Results for Linear Voltage Divider

CUT	**Faulty Component & Value**	**Magnitude of diagnosis variables (volts)**	**Threshold**	**Mean Deviation obtained for faulty components**
Linear Voltage Divider $V_{2,N}$=8.2128 $V_{6,N}$=0.44019	R_2 (7kΩ) R_4 (6 kΩ)	V_2 = 9.3 V_6 = 0.244	-0.523	-0.736 -0.695
	R_1(9kΩ) R_3 (1.4kΩ)	V_2 = 4.83 V_6 =0.335	2.72	-2.05 2.27
	R_1(8 kΩ) R_2 (9 kΩ)	V_2 = 6.85 V_6 = 0.192	0.8	-2.35 -1.25
	R_1(7.5kΩ) R_2(7kΩ) R_6(20kΩ)	V_2 = 7.52 V_6 = 0.253	0.36	-1.69 -1.09 0.35
	R_6(20kΩ) R_7(10kΩ) R_9(3kΩ)	V_2 = 9.1608 V_6 =0.42575	-0.86	-4.5 -3.4 -2.07
	R_4(1500Ω)	V_2 = 7.13	0.66	0.56

	R_6(9kΩ) R_7(10kΩ) R_8(9k)	V_6 =0.359		0.205 0.36 0.546
	R_3(7000Ω) R_6(5kΩ) R_8(7k) R_9 (4.5kΩ)	V_2 = 7.122 V_6 =0.304	0.5635	0.259 0.333 0.49 0.225

Discussion

A method based on threshold to detect multiple faults using test vectors is proposed. The approach uses MNA to simulate the CUT. Faults are generated using a random fault generator and injected into the CUT. The algorithm checks for the columns in the fault variable matrix with the mean deviation value lesser than the threshold to identify faulty components. The diagnosis variables with unequal test vector values are selected so that all of the circuit components are covered. But in case of linear voltage divider the components R_5 & R_{10} are not covered because the test vectors are same except for the input current. But the current value deviation in the test vector is too less for both the components and the fault variable values are found to be approximately same. Hence the proposed approach fails to detect these two components variation. And in case of Sallen Key BPF three diagnosis variables are found to be the requirement for all component coverage. It has been found that the approach is able to detect up to four components failure with higher offline calculation. It has been found that the approach is able to identify successfully the multiple faults with larger deviation as well as smaller deviation.

Conclusion

A method for locating multiple faults in analog circuits is proposed. The tolerance effect in real time testing, with the simulated test vector affects the practical possibility of implementation of test vector based testing. As explained this problem can be solved by generating the test vector for upper bound, lower bound and nominal values of the CUT. Multiple faults of size four with different magnitudes can be found successfully.

References

[1] L.Huang & C.Yao, “Data Processing method of fault samples in analog circuits”, Future Communication, Information and Computer Science-Sheng(Ed.), Taylor & Francis Group, London, 2015.

[2] Shiguan Zhou, Guojun Li, Zaifei Luo, Yan Zheng, “ Analog Circuit Fault Diagnosis Based on LVQ Neural Network”, Applied Mechanics and Materials, 2013,Vols.380-384, pp 828-832.

[3] Ashwani Kumar and A P Singh, " Neural Netwok based Fault Diagnosis in analog Electronic Circuit using Polynomial Curve Fitting", International Journal o Computer Applications 61(16):28-34, January 2013.

[4] Michal Tadeusiewicz, Stanislaw Halgas and Marek Korzybski, "Multiple catastrophic fault diagnosis of analog circuits considering the component tolerances", International Journal of Circuit Theory and Applications, volume 40, Issue 10, pages 1041-1052, October 2012.

[5] Jian Sun , Chenghua Wang1, Jing Sun , and Lei Wang, "Analog Circuit Soft Fault Diagnosis based on PCA and PSO-SVM", Journal Of Networks, Vol. 8, No. 12, December 2013.

[6] Chenglin Yang, Shulin Tian, Bing Long, and Fang Chen, " Methods of handling the

[7] Tolerance and Test point Selection problem for analog circuit fault diagnosis", IEEE Transactions on Instrumentation and Measurement, 2011, vol. 60, no.1, pp 176-185.

[8] Jose A. Soares Augusto and Carlos Beltran Almeida, " A Tool for Single-Fault Diagnosis in Linear Analog Circuits with Tolerance Using the T-vector Approach", Hindawi Publishing Corporation, VLSI design, 2008, pp 1-8.

[9] J.W.Bandler and A.E.Salama (1985), Fault diagnosis of analog circuits, Proceedings of the IEEE, vol.73,no.8, pp 1279-1325.

[10] C.-W.Ho, A.Ruehli and P.Brennan (1975), The modified nodal approach to network analysis, IEEE Transactions on Circuits and Systems, Vol.22, no.6, pp.504-509.

[11] Jiri Vilach and Kishore Singhal, Computer methods for circuit analysis and design, Van Nostrand Reinhold Company, 1983.