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Unconventional Approach to Low Energy Universal Shift Register and Up/Down Counter for Digital Circuits

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Abstract

In this paper, a new class of universal shift register and Up/Down Counter are implemented using CP^3L and CSP^3L. It is experimentally assessed in 180nm cadence technology. Large amount of the power is consumed by FFs and latches in microprocessors and VLSI systems. In this class of Universal Shift Register and Up/Down Counter, energy efficient latches are used. The class of Universal Shift Register and Up/Down Counter implemented with energy efficient latches shows improvement in energy efficiency compared to the existing topologies. Three circuit implementations of Universal Shift Register and Up/Down Counter are discussed. Measurements show that the proposed universal shift register and Up/Down Counter, using CP3L and CSP3L performs better than the universal shift register and Up/Down Counter using TGPL. This leads to increase in cost and area in overall typical systems but it is very less. Thus, the class of universal shift register and Up/Down Counter are suited for VLSI systems that require energy efficiency.

Keywords— Energy Efficiency, Energy Delay Product, Flip-Flops (FFS), Pulsed Latches, Shift Register, Counter, VLSI Systems.

1. INTRODUCTION

Today energy efficiency of FFs and latches is more demanding than in the past. Improving the energy efficiency can in turn increase the speed [2], [8], [9]. Pulsed

latches typically show the best energy efficiency compared to all other latches [10]-[15][20]. The transmission gate pulsed latch (TGPL) used in various Intel microprocessors is the most energy-efficient FF in a rather wide portion of the Pareto-optimal curve, ranging from high-speed (i.e., points with minimum ED^j product with $j>1$) to energy-efficient designs (i.e., points with minimum ED)[1]. Skew-tolerant FF (STFF) performs better than the transmission gate flip-flop (TGFF) for extremely high-speed design targets [16] (i.e., points with minimum ED^j for $j \geq 5$). In this region, the STFF speed provides an advantage in terms of D–Q delay and is typically about 10%, at the cost of a 2× more energy [11]. Hence, although STFF leads TGPL in terms of pure performance, but has significantly worse energy efficiency. This makes it not much competitive as TGPL in applications where energy efficiency is a concern [20]. Hence, TGPL is adopted as a reference for high-speed energy-efficient designs. When slower design targets are considered, master-slave FFs exhibits better energy efficiency. The traditional TGFF is the most efficient among designs with balanced energy-delay (i.e., minimum ED) [17]. Toshiba ACFF, is one of the most efficient designs among ultralow energy designs (i.e., minimum E^jD with $j > 1$) [18][20].

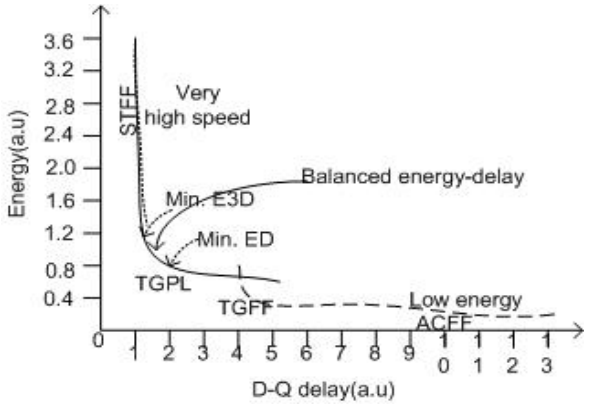

Fig. 1. Pareto-optimal energy-delay curve of existing FF topologies for a load of 16 minimum inverters (energy per cycle and *D–Q* delay are in arbitrary units) [20]

A novel class of pulsed latches CP^3L and CSP^3L(conditional push–pull pulsed latch and conditional shareable push–pull pulsed latch) using a push–pull output stage, is driven by two split paths for rise and fall output transitions, reduces both the path effort and the parasitic delay [19]. This performs better than the transmission gate pulsed latch (TGPL) [20]. The capacitance at the output of the first stage is further reduced by considering half-latches in the split paths and moving the cross-coupled inverters to the output node. The CP3L and CSP3L have1.3×–2.3× better energy efficiency compared to TGPL, as well as 1.5×–2× D–Q delay improvement even in the presence of process variations but a 1.15×–1.35× larger area than TGPL, which results in an increase in the area of practical VLSI systems but it is less than 1%[20].

In the class of Universal Shift Register and Up/Down Counter, energy efficient latches are used. Three circuit implementations (Universal shift register and Up/Down Counter using TGPL, CP3L and CSP3L) are discussed. Analysis show that the Universal shift register and Up/Down Counter using CP3L and CSP3L performs better than the universal shift register and up/down counter using TGPL. This arrives at the cost of increase in overall area in typical systems but it is very less. This paper is organized as follows. In section II TGPL, CP3L and CSP3L circuit diagrams are described. In section III results of transient and energy analysis of TGPL, CP3L and CSP3L are shown. In section IV universal shift register circuit diagram is described. In section V results of transient and energy analysis of universal shift register using TGPL, CP3L and CSP3L are shown. In section VI Up/Down counter circuit diagram is described. In section VII results of transient and energy analysis of Up/Down counter using TGPL, CP3L and CSP3L are shown. Conclusions are reported in section VIII.

2. ENERGY EFFICIENT LATCHES

A. TGPL

The following Fig.2 shows the circuit diagram of TGPL.

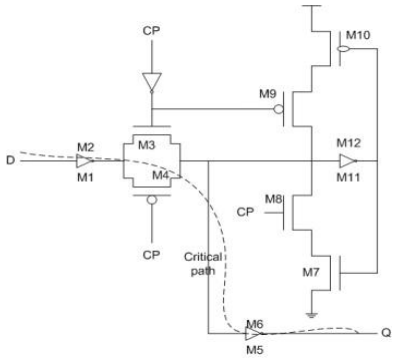

Fig. 2. Transmission Gate Pulsed Latch circuit diagram (TGPL) [20].

TGPL is triggered by a pulse clock waveform which is generated by the pulse generator (Fig.3).

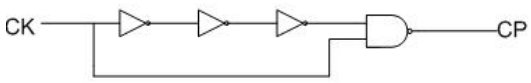

Fig. 3. Pulse generator circuit diagram [20]

B. CP^3L

The following Fig.4 shows the circuit diagram of CP^3L.

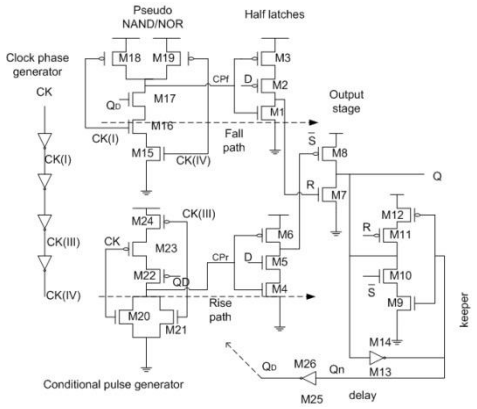

Fig. 4. Conditional Push-Pull Pulsed Latch circuit diagram (CP^3L) [20].

A push–pull output stage is used (M7–M8). This technique reduces the load of the driving circuitry by a factor 2–3, thereby making it faster and more energy-efficient. [20]. The active-high R (active-low set $\bar{S}$) pulsed signal, which resets (sets) the output when active are generated by the push–pull output stage driven by two split paths. These pulses are generated alternatively to enable a fall/rise output transition. These pulses are generated at the falling edge of clock by the conditional pulse generator, and are sent to the output stage by either M1–M3 or M4–M6 half latches, depending on whether input D is, respectively, low or high. This results in less parasitics [10]–[18]. The input D drives two different paths, respectively, through an nMOS (M5) and a pMOS (M2) transistor [20].

After the falling edge of clock, the pulse generator reviews if the previous output Q_D is high or low. If previous output is Q_D = 1, next output Q can make a falling transition or stay at the same value. A pulse is generated in the fall path through the active-low signal CP_f and nothing changes in the rise path (active-high signal CP_r is kept low, thus latch M4–M6 keeps $\bar{S}$ high and maintains M8 OFF).If the input remains at the previous value D = 1, the latch M1–M3 disabled; hence R is dynamically kept at the previous value R = 0. If the input changes to D = 0, the latch M1–M3 is enabled and the CP_f pulse determines a high pulse in R. Then M7 is turned ON and leads the output Q to low. Eventually, the replica of delayed output Q_D experiences the same transition. [20].

If the preceding output is Q_D = 0, after the falling edge of clock, then a pulse is generated in the rise path through the active-high signal CP_r (nothing changes in the fall path). If the input remains at the previous value D = 0, the latch M4–M6 is disabled and $\bar{S}$ is retained high. If the input changes to D= 1, the latch M4–M6 is enabled and the CPr pulse pulls down $\bar{S}$. Then M8 is turned ON and results Q to high. Eventually the replica of delayed output QD experiences the same transition. R ($\bar{S}$) is set to 0 (1) at the steady state, so that the output transistors M7–M8 is turned on. Output is maintained at the desired value by a keeper. Hence the parasitic associated with the memory element are moved to the output node, so the input

node of the output stage is mildly loaded. Hence faster and energy efficient. [20].

The output Q is driven by the keeper (M9–M12). The Keeper consists a cross-coupled inverter pair, its forward inverter is gated to avoid current contention with the output stageM7–M8. If R = 1 the pull-down network M7 of the output stage is turned ON and the pull-up network of the keeper is OFF through M11. If $\overline{S}$= 0, the pull-up networkM8 of the output stage is turned ON and the pull-down network of the keeper is OFF through M10. An advantage of placing the keeper after the output stage than before, CP^{3}L has lighter load on its critical path because the half latch M1–M3 (M4–M6) in the first stage has to drive the single transistor M11 (M10). Also, the two pulses R and $\overline{S}$ are alternatively generated, so that either M10 or M11 in the keeper are subject to transitions of the gate terminal in a given cycle. This in turn reduces the parasitic load of the first stage of CP^{3}L and reduces activity at the keeper capacitances, so that the first stage is made faster and more energy efficient. [20].

The pulse generator, consists of a clock phase generator, a pseudo-NAND for the fall path (M15–M19), and a pseudo-NOR gate for the rise path (M20–M24).Generally, the pseudo-NAND (pseudo-NOR) gate sets signal CP_f (CP_r) high (low), since signals $CK^{(I)}$ and $CK^{(IV)}$ (CK and $CK^{(III)}$) are complementary and thus keeps either transistor M18or M19 (M20 or M21) ON. After the falling edge of clock, signals $CK^{(I)}$ and $CK^{(IV)}$ (CK and $CK^{(III)}$) are both temporarily high (low) because of the transitions of the four inverters within the clock phase generator. A conditional pulse generator is implemented by the clock phase generator and the pseudo-NAND/NOR gates, which alternatively produce a pulse on either CP_f or CP_r, which is determined by the previous value of output Q_D[20].

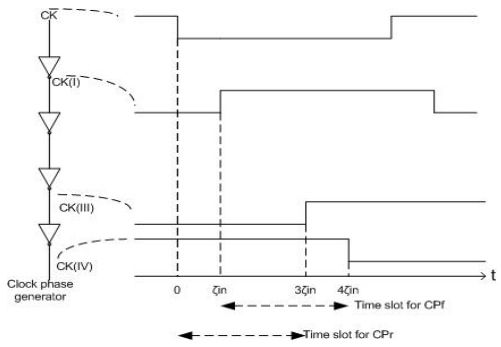

Fig. 5. Clock phase generator and waveforms defining CP_r and CP_f pulses [20].

A delayed replica Q_D of the output Q is generated by the delay stage in the feedback path. The delay stage is implemented by the two inverters M13–M14 and M25–M26. This delay stage makes sure that Q_D is kept stable at its previous value during the transparency window, so that the glitches in CP_r and CP_f are prevented and the dynamic energy get reduced. [20].

C. CSP^{3}L

In CP^{3}L, the pulse generator cannot be shared among multiple latches because the pseudo-NOR/NAND driven by Q_D, is different for each latch. In CSP^{3}L the conditional logic is used in the latch so that the whole pulse generator can be shared. The following Fig.6 shows the circuit diagram of CSP^{3}L [20].

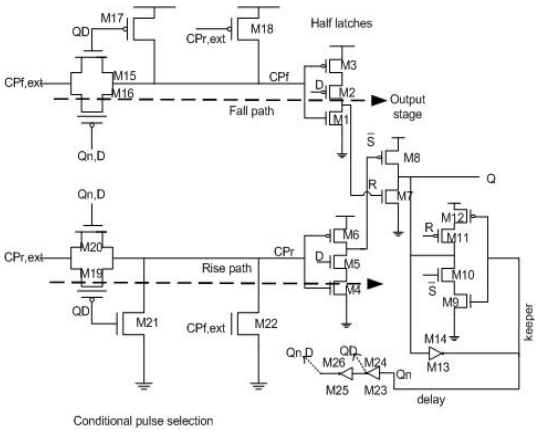

Fig. 6. Conditional Shareable Push-Pull Pulsed Latch Circuit Diagram. (CSP^{3}L)[20]

In CSP^{3}L, static NAND/NOR gates are used in the shareable pulse generator to generate the pulses $CP_{f,ext}$ and $CP_{r,ext.}$ These pulses are distributed to multiple latches and do the same role done by CP_f and CP_r in CP^{3}L. In each latch, such external pulses are enabled through the switches M16–M22 in Fig. 6, which implement the conditional pulse selection logic.It comprises two transmission gates and two small keepers to retain the similar operation as CP^{3}L. The delay stage M23–M26 is used in the feedback path (two more than CP^3 L). The resulting transistor count is the same as CP^3 L, hence CSP^{3}L area is expected to be the same as CP^{3}L (excluding the shareable part).

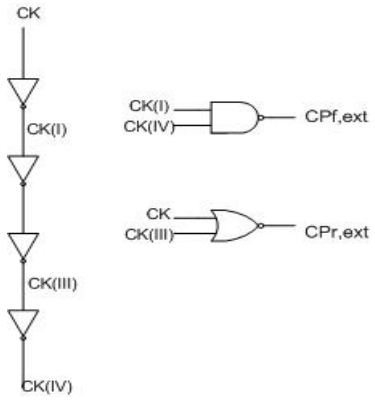

Fig 7. Shareable pulse generator[20].

Operation of CSP^{3}L is same as CP^{3}L. The difference between CSP^{3}L and CP^{3}L is in the conditional pulse selection logic. Conditional pulse selection logic allows the propagation of either $CP_{f,ext}$ or $CP_{r,ext}$ to the half latches, based on the value of replica of delayed output Q_D.If $Q_D = 1$ ($Q_D = 0$) the fall (rise) path is activated, and the transmission gate M15–M16 (M19–M20) transfers the $CP_{f,ext}$ ($CP_{f,ext}$) pulse to the input of the half latch M1–M3 (M4–M6)[20].

3. ANALYSIS AND MEASUREMENTS OF TGPL,CP3L,CSP3L

Implementation of these energy efficient latches in cadence 180nm yields the following results.

A. TGPL

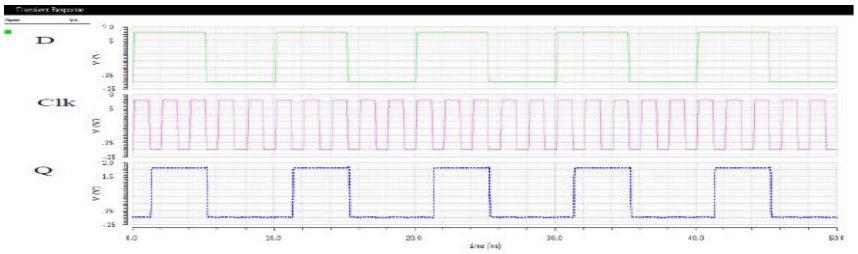

Fig. 8. Transient analysis of TGPL

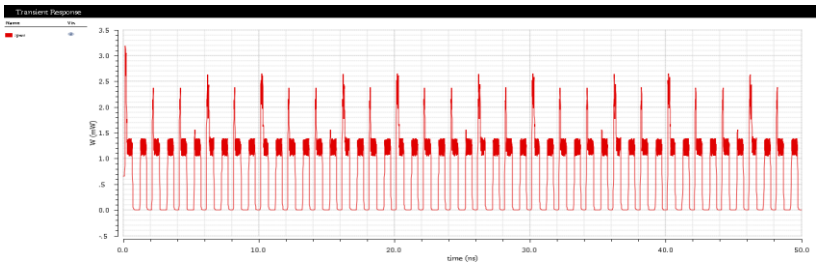

Fig. 9. Energy analysis of TGPL

B. CP^{3}L

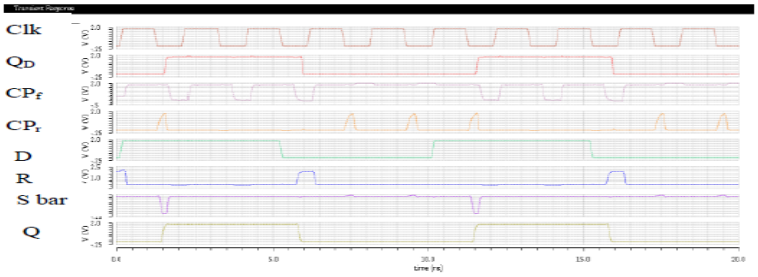

Fig. 10. Transient analysis of CP^{3}L

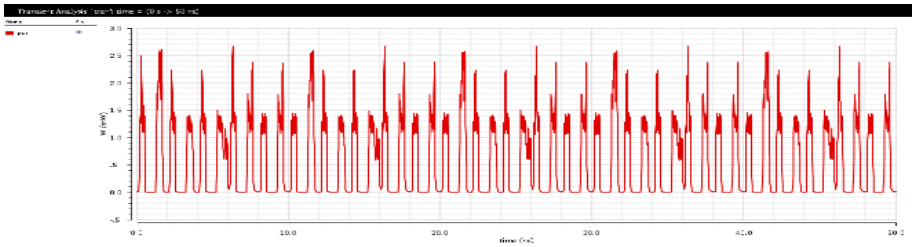

Fig. 11. Energy analysis of CP^3L

C. CSP^3L

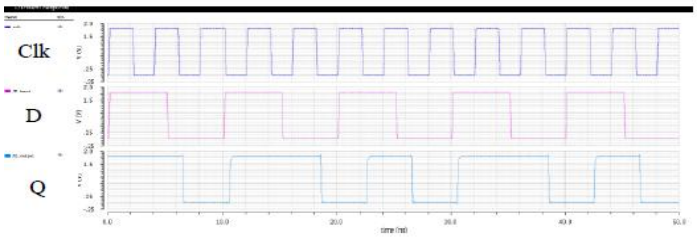

Fig. 12. Transient analysis of CSP^3L

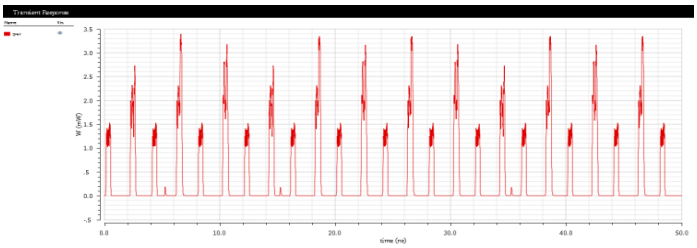

Fig. 13. Energy analysis of CSP^3L

D. Analysis Report

TABLE I ANALYSIS REPORT

PARAMETER		TGPL	CP^3L	CSP^3L
Energy (J)		708.9E-6	642.8 E-6	494.8 E-6
Delay (sec)	Q – D	6.178E-9	5.411 E-9	8.46E-9
	D – Q	-5.061 E-9	-3.765 E-9	-4.636 E-9
	Q – CLOCK	14.18 E-9	13.41 E-9	14.46 E-9
	CLOCK – Q	-17.06 E-9	-3.765 E-9	-4.364 E-9
ED Product(J-sec)		10.05E-12	8.62E-12	7.155 E-12
Max.operating frequency		49.1MHz	53.13MHz	43.6 MHz

4. UNIVERSAL SHIFT REGISTER USING ENERGY EFFICIENT LATCHES

A shift register is capable of shifting the binary information stored in one cell to its neighbouring cell, in a selected direction. The shift register consists of number of flip-flops arranged in cascaded configuration, and the output of one flip-flop is coupled to the input of the next flip-flop. All the flip-flops have identical clock pulses, which activate the data shifting. A shift register which shifts the data in both directions as well as load it parallel, then it is known as a universal shift register. The following Fig 14.demonstrates the symbol and circuit diagram of a four-bit universal shift register. The circuit consists of four energy efficient latches and four multiplexers. The four multiplexers have common selection inputs s1 and s0. The selection inputs control the mode of operation of the register according to the function entries in Table II.

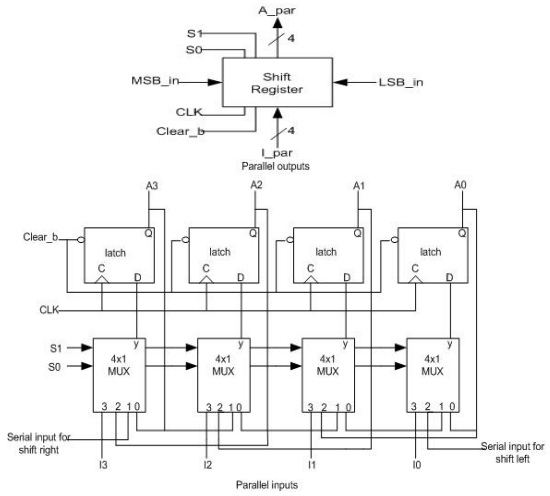

Fig. 14. Symbol and circuit diagram of a four-bit universal shift register.

When s1s0 = 00, the present value of the register is applied to the D inputs of the latches. This condition forms a path from the output of each latch into the input of the same latch, so that the output recirculates to the input in this mode of operation. The next clock edge transfers into each latch the binary value it held previously, hence no change of state occurs.

TABLE II MODE CONTROL FOR SHIFT REGISTER

Mode control		Register operation
S1	S0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

When s1s0 = 01, terminal 1 of the multiplexer inputs has a path to the D inputs of the latches. This brings about a shift-right operation, with the serial input shifted into latch A3. When s1s0 = 10, a shift-left operation results, with the other serial input going into the latch A0. When s1s0 = 11, the binary information on the parallel input lines is transferred into the register simultaneously during the next clock edge. Note that data arrives MSB_in for a shift-right operation and arrives LSB_in for a shift-left operation. An active-low signal Clear_b, clears all of the latches. Shift registers are often used to interface digital systems situated remotely from each other.

5. ANALYSIS OF UNIVERSAL SHIFT REGISTER USING ENERGY EFFICIENT LATCHES

A. Universal Shift Register Using TGPL

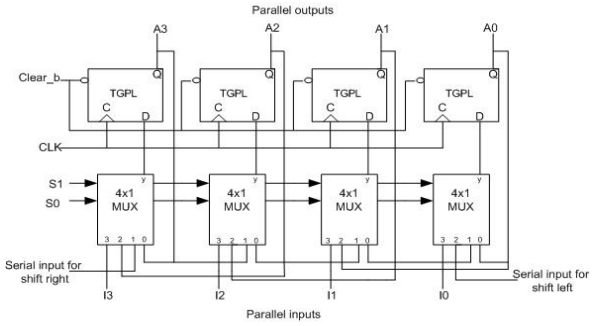

Fig. 15. Circuit diagram of a four-bit universal shift register using TGPL.

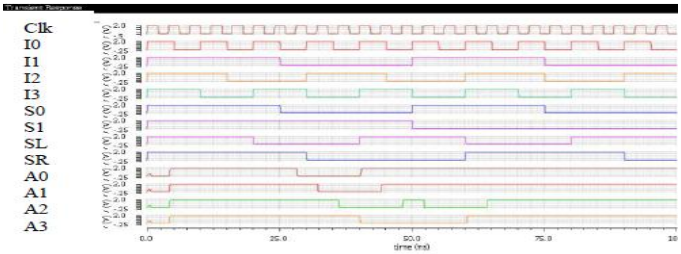

Fig. 16. Transient analysis of universal shift register using TGPL

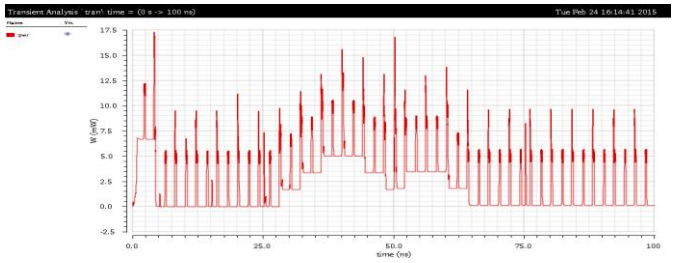

Fig. 17. Energy analysis of universal shift register using TGPL

B. Universal Shift Register Using CP^{3}L

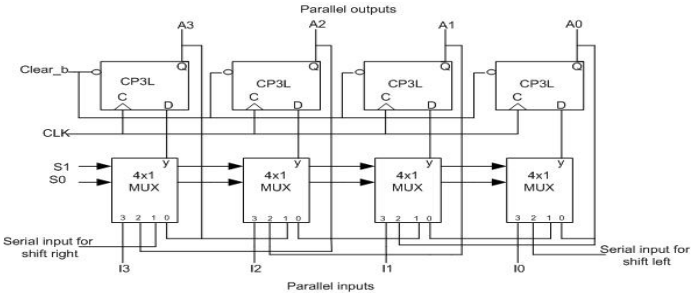

Fig. 18.Circuit diagram of a four-bit universal shift register using CP^{3}L

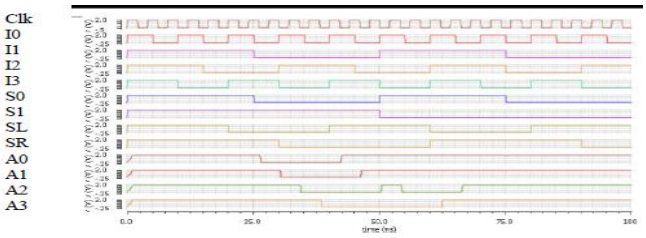

Fig. 19. Transient analysis of universal shift register using CP^{3}L

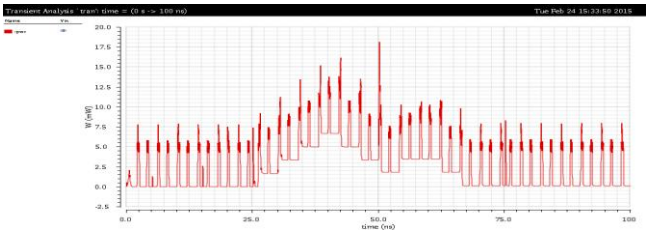

Fig. 20. Energy analysis of universal shift register using CP^{3}L

C. Universal Shift Register Using CSP^{3}L

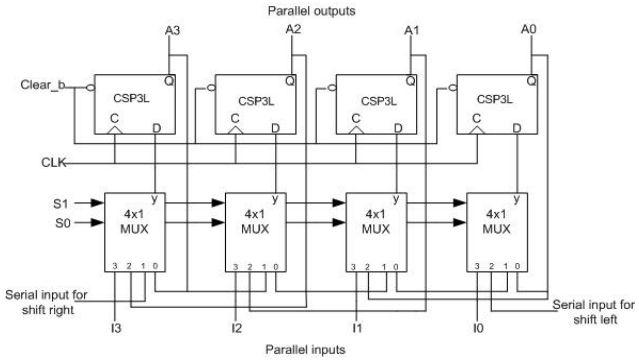

Fig. 21. Circuit diagram of a four-bit universal shift register using CSP^{3}L

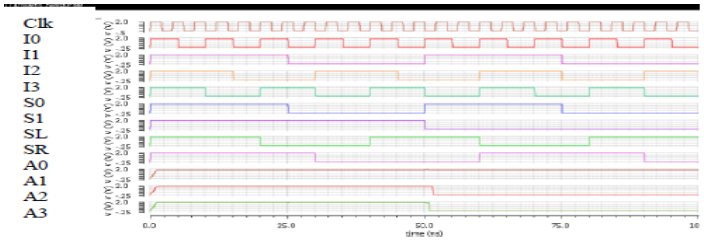

Fig. 22. Transient analysis of universal shift register using CSP^{3}L

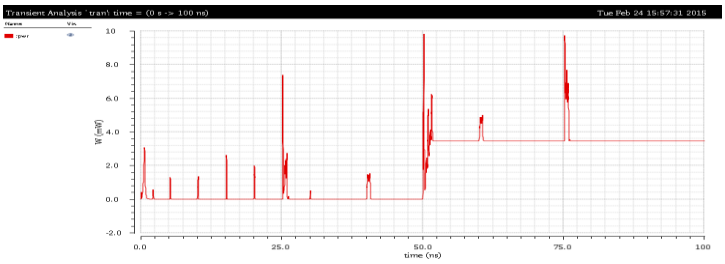

Fig. 23. Energy analysis of universal shift register using CSP^{3}L

D. Analysis Report

TABLE III ANALYSIS REPORT

PARAMETER	TGPL	CP^{3}L	CSP^{3}L
Energy(J)	2.033 E-3	1.09 E-3	E-6

6. UP/DOWN COUNTER USING ENERGY EFFICIENT LATCHES

A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter. The sequence of states may pursue the binary number sequence or any other sequence of states. A counter that pursues the binary number sequence is called a binary counter. An n -bit binary counter consists of n flip-flops and can count in binary from 0 through 2n-1. Counters are available in two categories: ripple (asynchronous) counters and synchronous counters. In a ripple (asynchronous) counter, a flip-flop output transition plays as a source for triggering other flip-flops. In other words, some or all the flip-flops are triggered, not by the common clock pulses, but by the transition that occurs in other flip-flop outputs. In a synchronous counter, all the flip-flops get the common clock.

The circuit of an up–down binary counter using T flip-flops is shown in Fig. 24. It has an up control input and a down control input. When the up input is high, the circuit counts up, since the T inputs get their signals from the values of the previous normal outputs of the flip-flops. When the down input is high and the up input is low, the circuit counts down, since the complemented outputs of the previous flip-flops are applied to the T inputs. This set of conditions ensures that only one operation is

performed at a time. Note that the up input has preference over the down input.

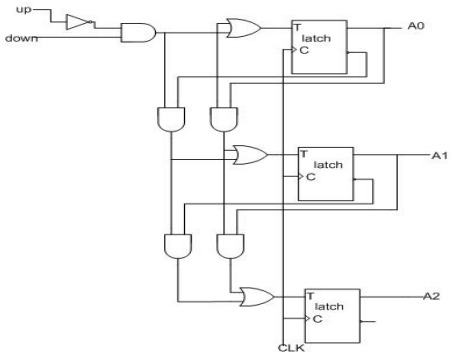

Fig. 24. Circuit diagram of a three-bit up/down counter.

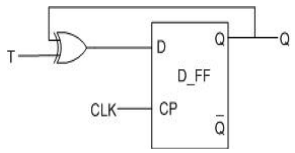

Fig. 25. Circuit diagram of latch to T_FF conversion.

7. ANALYSIS OF UP/DOWN COUNTER USING ENERGY EFFICIENT LATCHES

A. Up/Down Counter Using TGPL

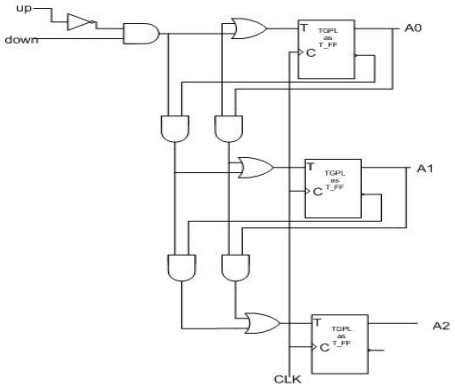

Fig. 26. Circuit diagram of a three-bit up/down counter using TGPL.

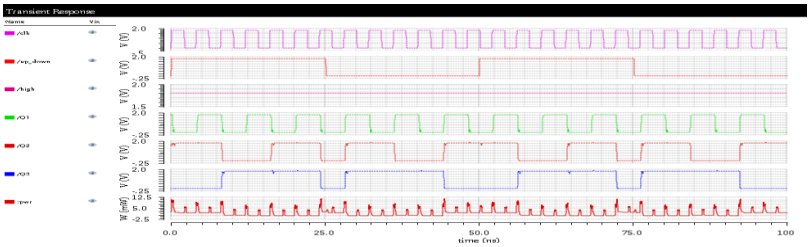

Fig. 27. Transient analysis and Energy analysis of up/down counter using TGPL

B. Up/Down Counter Using CP^{3}L

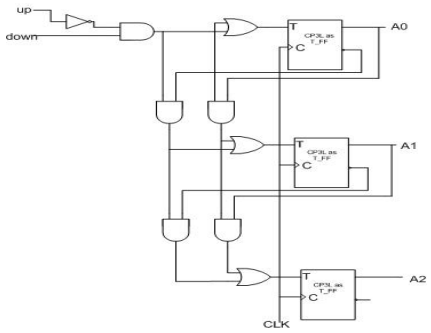

Fig. 28. Circuit diagram of a three-bit up/down counter using CP^{3}L

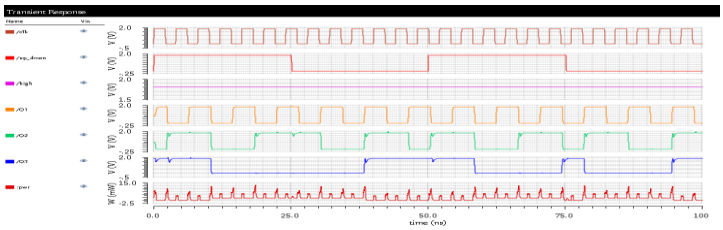

Fig. 29. Transient analysis and Energy analysis of up/down counter using CP^{3}L

C. Up/Down Counter Using CSP^{3}L

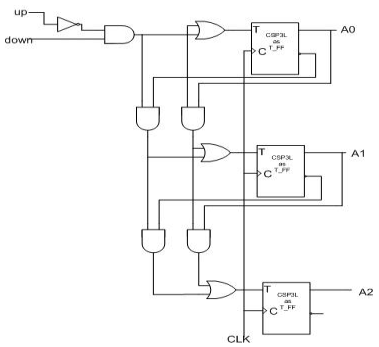

Fig. 30. Circuit diagram of a three-bit up/down counter using CSP^{3}L

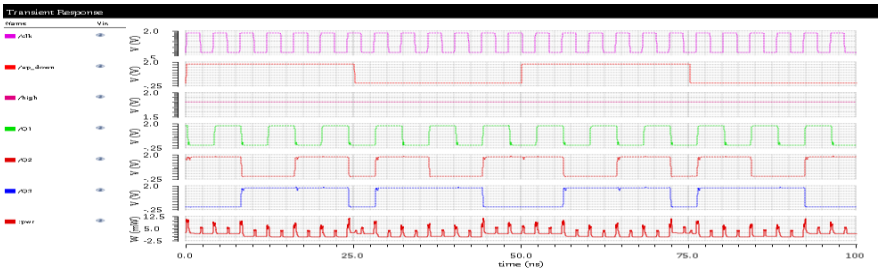

Fig. 31. Transient analysis and Energy analysis of up/down counter using CSP^{3}L

D. Analysis Report

TABLE IV ANALYSIS REPORT

PARAMETER	TGPL	CP^{3}L	CSP^{3}L
Energy(J)	3.351 E-3	2.027 E-3	82.45 E-6

8. CONCLUSION

In this paper, a new class of Universal Shift Register and Up/Down Counter have been introduced. Measurements showed that the universal shift register and Up/Down Counter using CP3L and CSP3L performs better than the Universal shift register and Up/Down counter using TGPL.This arrives at the cost of increase in overall area in typical systems but it is very less. Thus, the class of universal shift register and Up/Down Counter are well suited for VLSI systems that require energy efficiency.

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