International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 5 (2015) pp. 13027-13042

http://www.ripublication.com

A Simple Boost Shoot Through Control For Single Phase Cascaded Quasi Impedance Source Network DC-DC Converters

N.Shobanadevi

Assistant Professor, EEE department
University college of Engineering-Ariyalur,
Anna University-Chennai INDIA
(E-mail: Shobanadevi1975@gmail.com)

Dr.V.Krishnamurthi

Former professor, Anna University- Chennai

Dr. N. Stalin

Assistant Professor, Petrochemical Department,
University college of Engineering-Trichirappalli
Anna University-Chennai

Abstract

This paper presents a new DC-DC Converter with improved efficiency and reduced ripple free output, uses quasi ZSI (Impedance Source Inverter) for reducing energy losses in the output by the introduction of the two stage quasi impedance source network (qZSI). The proposed two stage quasi Z source network possesses one diode, two capacitors, and two inductors in addition to the conventional quasi ZSI. This paper proposes a new approach to the buck-boost DC-DC converter with high frequency, high boost factor and high voltage gain. Theoretical analyses of two operating modes ie shoot-through and non-shoot through mode of simple boost method is presented. The simulated results are presented and analyzed for various duty cycle and modulation index using simple boost pulse width modulation (PWM) technique by using MATLAB. Moreover, the proposed solution features over 50% increased boost factor and provide 53.33 % increased voltage gain than single stage quasi Z source buck boost dc-dc converter for the same shoot through duty cycle by SB PWM control technique.

Key-Words: - Impedance Source Inverter (ZSI), Pulse Width Modulation (PWM), full-bridge converter, VDR Voltage Doubler Rectifier

1. Introduction

In various industrial applications such as distributed power systems, hybrid electric vehicles, special power supplies and servomotor drives, the traditional VSI and CSI were widely used to replace the traditional inverter. To overcome the problems in the conventional inverters, the Z source inverter was emerged in which bridge type inverter have been successfully combined with dc – dc converter. In addition it provides high efficiency, reliability and low cost for its buck –boost power conversion ability [1]-[3].The advantage of shoot through state was utilized by gating focused, for the same component rating; shoot through duty cycle is greatly reduced for the same voltage boost ability. In other hand, for the same component rating, shoot through voltage conversion is greatly increased nearly fourfold boost of the DC input voltage due to the presence of VDR in the back end output side. As a modification of popular voltage fed Z source inverter (ZSI), voltage fed quasi Z source (qZSI) with continuous input current are discussed [4-6]. Dmitri vinnikov [7], provide two fold voltage boost of the DC input voltage with the overlapping of the active states control technique. In [10] were implemented with an input voltage V_{in}=40V the active duty cycle of active states ant the maximum shoot through duty cycle was set at D_A= 0.5 and D_{ST}= 0.5 per switching period in order to achieve the increased power density of the single stage converter also VDR implemented at its output side for its voltage doubling effect of the peak voltage of the secondary winding of isolation transformer.

To obtain a higher voltage gain with input voltage of V_{in}=230V to the output voltage of V_{out} =295(peak), with the same shoot through duty ratio D_{ST} =0.2 and the modulation index in the voltage fed impedance source inverter compares with the traditional Z source [11].The resonant period to match with the switching period of converter due to the large variance of the leakage inductance TR2 and resonant capacitor C3 in order to achieve the highest efficiency. Due to the reduced conduction losses of active states and output diodes with the lower current stresses, the converter provide higher output voltage and to attain higher efficiency [12].

Trinh et.al [13], dealt with addition of more capacitors and inductors with the conventional ZSI (Impedance Source Inverter) system. By doing this, voltage stress and voltage level can be improved. Even though there is addition of capacitor and inductor to the conventional system, shoot through ratio is maintained as same as that of conventional one. Further, voltage boost ratio can be improved, in order to improve the voltage boost level, concept of switched inductor is used. The shoot through states are eliminated when the DC input voltage is high and the qZS network based DC to DC converter starts to operate i.e. in the buck mode and the DC input voltage of conventional voltage source inverter when the DC input voltage is low, shoot through duty cycle ratio produces increase in voltage level i.e. in the boost mode. For realizing the voltage boost level, Pulse Width Modulation (PWM) control method is used and also the design of passive components is explained. The SL and SC Z Source inverters are proved much higher gain and to keep their component stress on both lower and upper switch of phase leg to boost the dc bus voltage. Hence qZS network based dc to dc converter working in the both operating condition i.e. buck-boost mode to keep their component rating lower [14]. For renewable and alternate energy source qzsI is an attractive converter for its unique advantage of lower component rating s and constant dc current from the source [15].

In [16] the improved inverter has a higher modulation index M with reduced voltage stress on the dc link and current stress flow to the diode and transformer winding also lower input current ripple for the same transformer turn ratio and input and output voltage for the fixed modulation index M with reduced size depends on problem and application under consideration on which select the controlling techniques because each technique has its own advantages and disadvantages and weight of the modulation index .

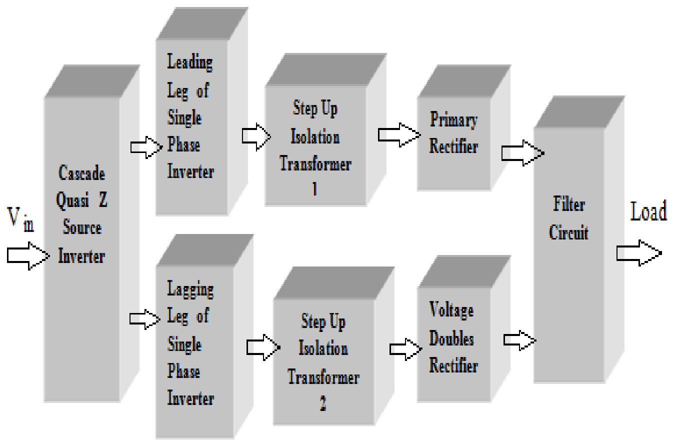


Fig: 1 Structure of DC-DC Converter with Cascaded qZSI

2. Basic Structure of Cascaded DC/ DC Converter

The basic block diagram of hybrid dc-dc converter with qZSI is shown in Fig.1. Here, DC supply is given to impedance source network in order to provide wide range of voltage than the traditional voltage or current source inverter. The output from impedance network is given to leading or lagging leg of single phase inverter depending on type of output from network. The fundamental voltage and current can be controlled through use of single phase inverter. In many applications, a constant or adjustable voltage is required.

So, in order to meet those requirements, a single phase inverter is used. The controllable AC output from inverter is stepped up by isolation transformers. Isolation transformers provide isolation of power device from power source and also it protects devices from electric shock or electric stress. The primary rectifier is used to convert AC to DC and given to filter circuit in order to eliminate ripples in output. The voltage doubler rectifier is used to produce twice as that of input voltage at output terminals. The filter circuit consists of combination LC circuit or output capacitors. It is used to select desired range of frequencies. The voltage doubler is used to improve the level of voltage to a required level and get filtered to reduce the ripples. Ripple free pulse is given to load circuit. So, it results improved quality of output. Thus, efficiency of system gets improved than the conventional method.

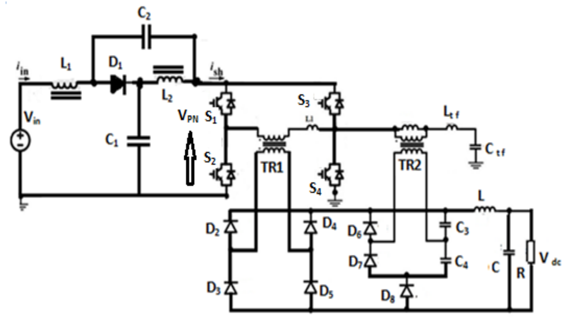


Fig: 2 Proposed System for Single Stage

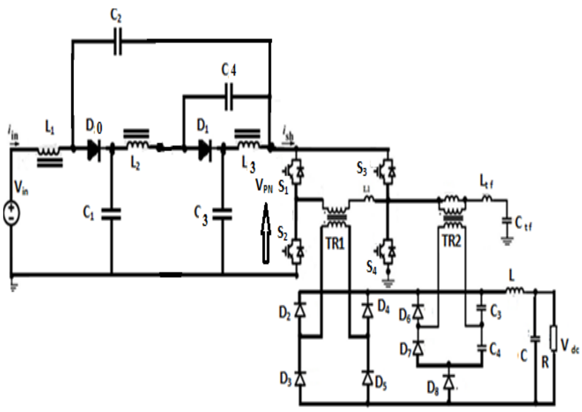


Fig: 3 Proposed System for Cascaded Stage

In above figure 2 & 3, input current flows Iin through the coil L_1 and shunt current I_{sh} flows through the switches. Based on the boosting factor, the level of input voltage can be increased or decreased by the use of impedance network. This network requires capacitance and inductance in small size and also it acts as a second order filter.

Assuming that quasi impedance network inductors L_{i1} and L_{i2} and capacitors C_{i1} and C_{i2} have same inductance (L) and capacitor (C) respectively, the quasi impedance source network becomes symmetrical. Using symmetry condition and equivalent circuit, we have

$$V_{Ci1} = V_{Ci2} = V_C \; ; \; V_{Li1} = V_{Li2} = V_L \qquad (1)$$

By observation of quasi impedance source dc-dc converter, the shoot through zero state for an interval of shoot through state interval T_{ST} during a switching cycle T_S , from Fig .2 has

$$V_L = V_C \,;\, V_d = 2V_C \,;\, V_i = 0 \tag{2}$$

Consider that the quasi Z source Inverter Bridge in any one of non shoot through states for an interval of T_{NST}. Hence As in Fig. 2

$$V_L + V_C = V_{in} \,;\, V_L = V_{in} - V_C \,;\, V_d = V_{in}$$

$$V_i = V_C - V_L = 2V_C - V_{in} \tag{3}$$

Where V in is input dc voltage.

The average inductor over one switching period (T_S) hould be zero, from equation (2) and (3), we get

$$V_L = \frac{T_{ST} V_C + T_{NST}\left(V_{in} - V_C\right)}{T_S} = 0 \tag{4}$$

Or

$$\frac{V_C}{V_{in}} = \frac{T_{NST}}{T_{NST} - T_{ST}} \tag{5}$$

Across the inverter bridge, average dc link voltage can be found as follows,

$$V_i = \frac{T_{NST}}{T_{NST} - T_{ST}} V_{in} = V_C \tag{6}$$

Similarly, from (3), the maximum dc link voltage across Inverter Bridge can be rewritten as,

$$V_i = V_C - V_L = 2V_C - V_{in} = \frac{T_S}{T_{NST} - T_{ST}} V_{in} = BV_{in} \tag{7}$$

Where

T_{ST} = Duration of shoot through state

T_{NST} = Duration of non shoot through state

T_S = operating period i.e. switching cycle

$$T_S = T_{ST} + T_{NST} \tag{8}$$

$$B=\frac{T_S}{T_{NST}-T_{ST}}=\frac{1}{1-\frac{T_{ST}}{T_S}(1+n)}=\frac{1}{1-D_{ST}(1+n)}\geq 1 \tag{9}$$

Where n is number of stages
If n=1 for traditional qZSI that is for single stage qZSI

$$B=\frac{1}{1-2D_{ST}}\geq 1 \tag{10}$$

D_{ST} is duty cycle of the shoot through state

$$D_{ST}=\frac{T_{ST}}{T_S} \tag{11}$$

The modulation index of qZS main circuit will be decreased to a very low level and it can be expressed as,

$$M\leq 1-D_{ST}$$

Where M is modulation index

$$M=\frac{Amplitude\ of\ Modulation\ waveform}{Amplitude\ of\ carrier\ Waveform}$$

From (7),

$$V_i=B.V_{in} \tag{12}$$

The equivalent dc link voltage of inverter is the maximum dc link voltage. Hence, the phase voltage of qZS inverter can be expressed as,

$$V_{dc}=V_i \tag{13}$$

$$V_{dc}=B.V_{in} \tag{14}$$

Resulting from shoot through state B is the boost factor. The equivalent dc link voltage of inverter is the maximum dc link voltage. Hence, phase voltage of qZS inverter can be expressed as,

$$V_{ac} = M\frac{V_i}{2} \tag{15}$$

Using equation (7) & (12), equivalent dc link of inverter can be further expressed as,

$$V_{ac} = M.B.\frac{V_{in}}{2} \tag{16}$$

Above equation further expressed as in terms of buck- boost factor

$$V_{ac} = B_{BB}.\frac{V_{in}}{2} \tag{17}$$

Where B_{BB} is buck boost factor.

$$B_{BB} = M.B = (0 \approx \propto) \tag{18}$$

The qZSI based dc-dc converter starts to function as traditional VS based dc-dc converter without shoot through condition, when input voltage is high enough, thus performing only buck function of the input voltage. From (1), (5) & (10), the capacitor voltage can expressed as,

$$V_{C1} = V_{C2} = V_C = \frac{1-D_{ST}}{1-2D_{ST}}.V_{in} \tag{19}$$

Note that the Boost factor B in (10) can be controlled by shoot through duty cycle D_{ST} which can be decided by interval of shoot through time D_{TST}. Also, buck boost factor B_{BB} is determined by the modulation index M and boost factor B. In simple boost method Pulse Width Modulation (PWM) techniques the modulation index M can be determined by the ratio of the amplitude of the modulation waveform to amplitude of the carrier waveform.

The voltage conversion ratio of qZS inverter can be expressed as,

$$G = V_{ac} = M.B.\frac{V_{in}}{2} \tag{20}$$

Hence From (1) & (14), the quasi impendence network can perform the step-up dc–dc conversion from V_{in} to Vdc, thus the numerical condition D_{ST} is limited to,

$$0 \le D_{ST} \le 0.5 \tag{21}$$

$$B = \frac{1}{1 - D_{ST}(1+n)} \geq 1$$; Where n=2 for 2 stage

$$B = \frac{1}{1 - 3D_{ST}} \geq 1$$

$$D_{ST} \leq 1/3 \tag{22}$$

3. SB PWM CONTROL

The block diagram of gating signal generator is shown in Fig.4. The various input pulses such as sinusoidal and ramp is compared with relational operator. The Pulse Width Modulation (PWM) signals are generated and part of output is inverted through logic gates to perform the control process of active and zero states. Thus, inverted output signal is given to thyristor switches S1 and S4 to turn ON. The relational operators used to analysis and compare the amplitude of various signals given as an input. The Pulse Width Modulation (PWM) with logic gates and comparator provides the control circuit for active and zero states.

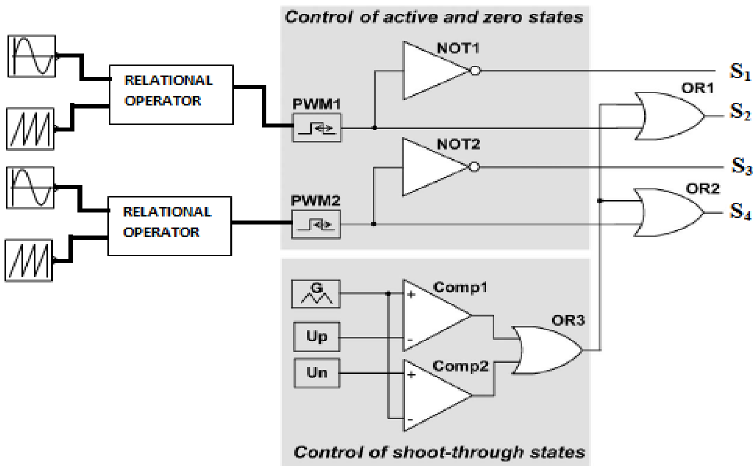


Fig .4 Generalized Block Diagram of Gating Signal Generator

The OR gates are used to perform addition of active and shoot-through states. Therefore, switches S2 and S4 get operated according to the gating signals. The shoot through states is controlled by comparator signals. The control from PWM signal is given as the input to logic gates which operates the switches. The upper and lower level signals output are compared with the help of comparator. The output from comparator is given to logic OR3 and given as one of the input to OR1 and OR2. The resultant is used to operate switches S2 and S4.The generation of shoot through pulses are given by Fig.5.

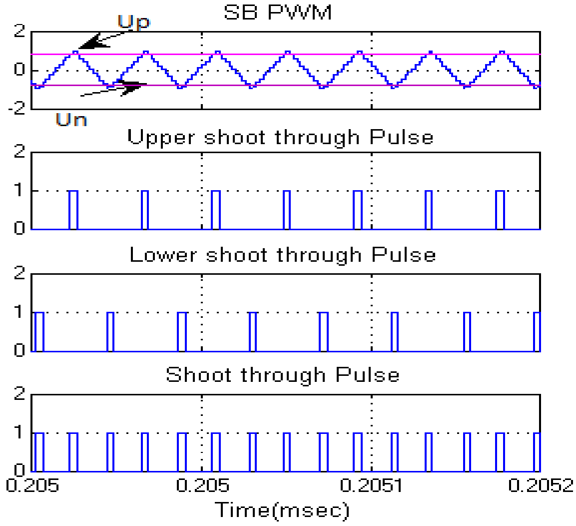


Fig.5 Generation of Upper and Lower Shoot Through Pulses

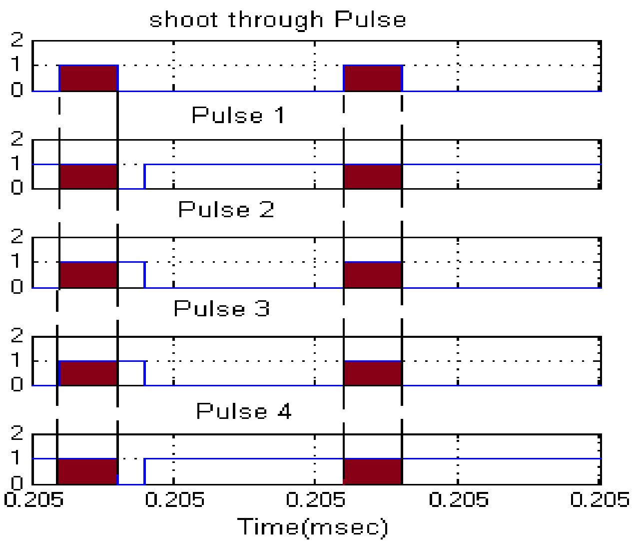


Fig: 6 Pulses of Various Switches

The upper and lower shoots through pulses generated are shown in figure. The peak of pulses is produced with reference DC line voltages. The lower and upper shoot through pulses are generated by comparing with the reference signal or saw tooth waveform. The lower shoots through pulses are produced as a inter-mediate pulses of upper shoot through pulses. These waves are modified and combined in order to reduce cost and reliability. Thus, the efficiency of power conversion can be greatly increased. In Fig. 6 various (S_1, S_2, S_3 &S_4) pulses are generated based on input given by the gate signal. At any instant two pulses starts at same time period and remaining two pulse remains in zero position for small interval of time.

4. SIMULATION RESULTS AND DISCUSSION

The parameters used in simulation are shown in Table 1. During simulation, the results are taken for various operating condition for boost factor and voltage gain. The simulation results for single stage qZS converter and cascaded two stage qZS converter are shown in the Table 2 and Table 3 respectively. By using various duty cycle and modulation index condition, the results are taken for simple boost control condition.

As in [8],V_{in}=40V,D_{ST}=0.25;M=0.75 showed that the qZS provide the voltage gain of B_{max}=2 for both the shoot through generation during freewheeling state and zero states .When using a generation of shoot through state by overlapping method for cascaded qZS as shown in [9], to produce a output voltage 80V, the demanded voltage boost is B_{max}=2 for the shoot through duty cycle D_{ST}=0.167, modulation index M=0.833 when using the SB control method the following simulation parameters are selected for the converters $L_1=L_2=L_3$=3mH, $C_1=C_2=C_3=C_4$= 20uF, R=47Ω. To demonstrate the waveforms the input voltage is set to 40V, switching frequency was f_S =47.6 KHz.

Table.1 Simulation Parameter

.

V_{in}	40V
L_1 , L_2 & L3	3 m H
C_1 & C_2	20 µF
C_3 & C_4	20 µF
C_0	20 µF
L_0	0.2 m H
R_0	47Ω
f_S	47.66KHz
D_{ST}	0.25
V_{dc}	100V
I_{dc}	3.4A

Table.2 Simulation Results for Boost Factor and Voltage Gain In Various Operating Condition for Single Stage

V_{in}	D_{ST}	M	B	G	V_{dc}	
					Simu	Calc.
40V	0.1	0.9	1.25	1.125	45	50
	0.2	0.8	1.667	1.33	65.2	66.62
	0.25	0.75	2	1.5	77	80
	0.3	0.7	2.5	1.75	100	100
	0.4	0.6	5	3.0	200	200
	0.45	0.55	10	5.5	400	400

Table.3 Simulation Results for Boost Factor and Voltage Gain In Various Operating Condition for Two Stage

V_{in}	D_{ST}	M	B	G	V_{dc}		I_o
					Simu	Calc.	
40	0.1	0.9	1.428	1.318	52.72	57.12	1.3
	0.2	0.8	2.5	2.3	92	100	1.9
	0.25	0.75	4	3.75	150	160	3.2
	0.3	0.7	10	9	360	400	3.5

An observation is noted from Table 2 & 3 the logic Controller set to the value of the shoot through duty cycle D_{ST} = 0.25, modulation index M = 0.75, in to the single phase inverter ,dc input voltage V_{in} = 40V is boosted to the simulated output voltage V_{out} = 150 with the voltage conversion ratio G = 3.75 and the boost factor B = 4.

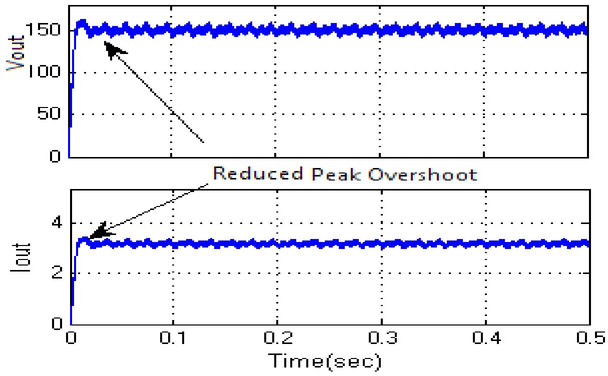
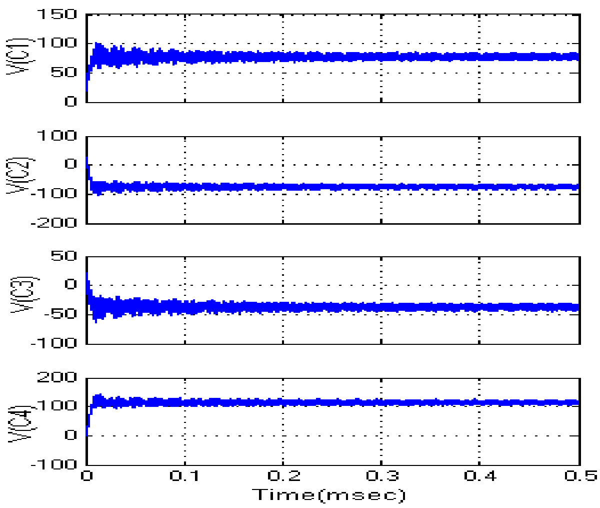
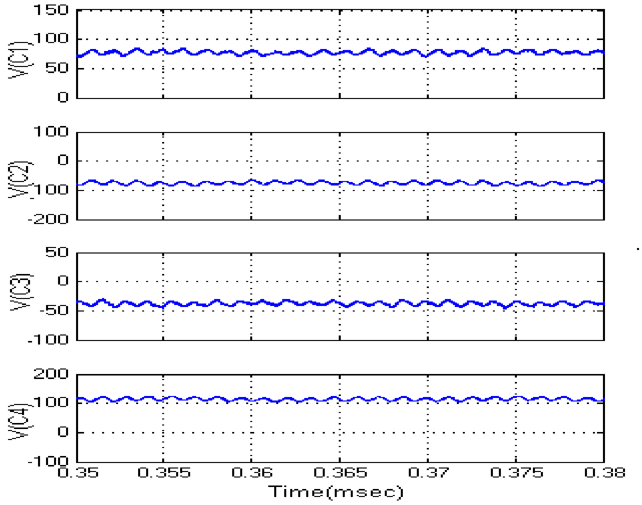


Fig.7. Simulated waveforms of DC Output Voltage and Output Current for input voltage V_{in}=40V; D_{ST} =0. 25; M =0.75.



(a)



(b)

Fig. 8. (a) Simulated waveforms of Operating Voltage of Capacitor C_1, C_2, C_3 & C_4 during the minimum input voltage V_{in}=40V; D_{ST} =0.25 (b) Zoom in view

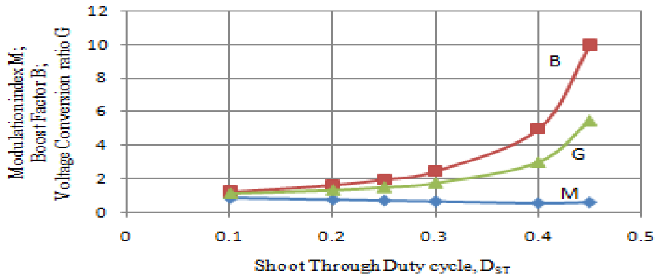


Fig: (9) Relationship of Modulation index M, Gain G, Boost Factor B for various duty cycle for input voltage V_{in}=40V for n=1.

We can get simulated output current and output voltage V_{out} = 150 with the reduced ripples at its output side for the input voltage V_{in} = 40V, these results can be shown in the Fig.7. In Fig 8a & 8b depicted the working voltage of various capacitance C_1 to C_4 associated with cascaded network and the zoom in view of simulated waveforms. Fig 9 & Fig.11 shows the correlation between modulation index M, voltage conversion ratio G, Boost factor B for the different values of shoot through duty cycle for the single stage (n =1) and for cascaded stage (n = 2). As can be seen from Fig 9 & Fig.11 and Table 2 & 3 for the same duty cycle D_{ST} = 0.25, the boost factor is accurately increased to 50% specifically fourfold (B=4) and voltage gain raised more than 50 % that is to say, gained to G=3.75 from G=1.75. The ac link voltage V_{pn} across the primary isolation transformer Tfr1 and secondary isolation transformer Tfr2 and simulated voltage and current stress of the inverter link switches S_1 and S_3 are shown in Fig.10. In Fig.12 the dc ended voltage for the single stage and cascaded quasi based dc/dc converter using SB PWM technique control are compared and showed that the cascade converter offer more boost voltage.

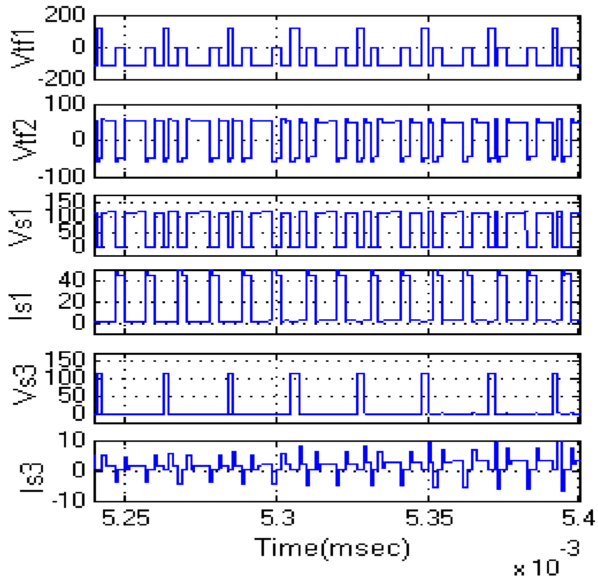


Fig: 10 Simulated waveforms of operating voltage and currents of the high frequency step up isolation transformer and switches 1 & 3 during the minimum input voltage V_{in}=40V; D_{ST}=0. 25.

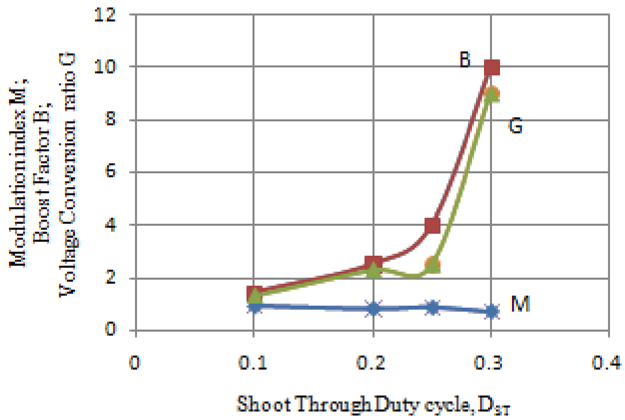
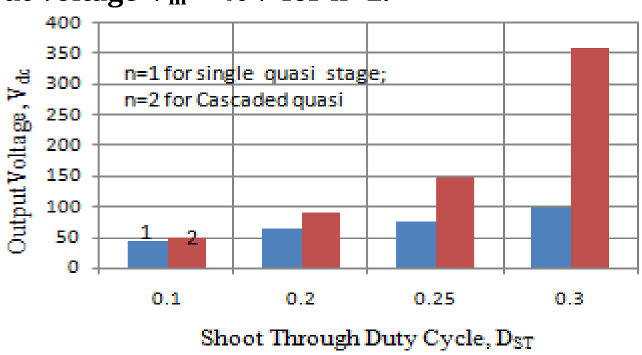


Fig: 11 Relationship of Modulation index M, Gain G, Boost Factor B for various duty cycle for input voltage V_{in} = 40V for n=2.



Figs.12 Relationship between dc output Voltage and Duty Cycle ratio for single and cascaded stage

5. Conclusion

The simple boost through PWM scheme are comprehensively analysed in DC/DC converter and their performances are obtained in simulation. The proposed cascaded quasi Z Source network converter with two transformer, primary rectifier and VDR has a higher modulation index, lower shoot through duty cycle with high output voltage gain , precisely fourfold boost inversion ability and reduced voltage stress flow to the transformer winding capacitance and diode when compared with single stage converter for same PWM techniques for the same shoot through cycle .The ripples and peak overshoot can be reduced in the output voltage and current by use capacitors to improve the efficiency of the output. The Z source inverter based DC/DC can be extended to any topology with suitable rectifier and modulation strategies.

References:

[1] F.Z.Peng, “Z source Inverter”, IEEE Trans. On Industrial Power Electronics., vol. 39, no.2, pp. 501–510, Mar/Apr 2003.

[2] F.Z peng and Miaosen Shen Zhaoming , “ Maximum Boost Control of the Z Source Inverter”, in the proc. of IEEE PSEC 2004.

[3] P.C. Loh; D.M.Vilathgamu; Y.S. Lai : G.T. Chua; Y.W.Li, “ Pulse Width Modulation of Z source Inverter” , IEEE Trans. on Power Electronics., vol. 21, no.6, pp. 1346–1355, Nov2005.

[4] Anderson, J.;Peng,F.Z; Dichen Liu, “Four quasi – Z source inverters”, in Proc. of IEEE power Electronics Specialists Conferences PESC’2008,pp.2743-2749,15-19 June 2008.

[5] Yuan Li; Anderson, J.;Peng,F.Z; Dichen Liu, “ Quasi Z source inverter for photovoltaic power generation”, in Proc. of IEEE Applied power Electronics Conferences and Exposition APEC’2009,pp.918-924,15-19 Feb 2009.

[6] Jong-Hyoung Park; Heung-Geun kim;Eui-cheol Nho; Tae-Won Chun; jaeo Choi, “Grid connected PV system Using a Quasi – Z source inverters”, in Proc. of IEEE Applied power Electronics Conferences and Exposition APEC’2009,pp.925-929,15-19 Feb 2009.

[7] Ditri Vinnikov;Indrek Roasto; Ryszard Strzelecki, Marek Adamowicz “Two Stage Network Based Step Up DC/DC Converter”, in Proc of IEEE ,PP.1143-1148,2010.

[8] Indrek Roasto;Dmitri Vinnikov; Tanel Jalakas; Janish Zakis;Silver Ott, , “Experimental Study of Shoot Through Control Methods for qZSI Based DC/DC Converters”, in Proc of IEE International symposium on Power Electronics SPEEDAM 2010 ,PP.29-34,2010

[9] Dmitri Vinnikov; Ryszard Strzelecki; Marek Adamowicz , “Performance Improvement Method for the Voltage-Fed qZSI with Continous Input current”, in Proc of IEEE ,PP.1459-1464,2010.

[10] Dmitri vinnikov;Indrek Roasto, “ Quasi –Z-Source – Based isolated DC/DC Converters for Distributed Power Generation” , IEEE Trans. on Power Electronics., vol. 58, No.1, pp. 192–201, Jan 2011.

[11] Wei Qian; Fang Zheng peng; Honnyong , "Trans-Z-Source Inverters" , IEEE Trans. Power Electronics., vol. 26, No.12, pp. 3453–3463, Dec 2011.
[12] Wensong Yu;Jih Sheng Lai;Wei –Han Lai; Hongmei wan, " Hyhrid Resonant and PWM Converters with High Efficiency and Full Soft switching Range" , IEEE Trans. on Power Electronics. vol. 27, No.12, pp. 4925–4933, Dec 2012.
[13] Quoc-Nam Trinh and Hong-Hee Lee, A New Z-Source Inverter Topology with High Voltage Boost Ability", Journal of Electrical Engineering & Technology Vol. 7, No. 5, pp. 714~723, 2012
[14] Ding Li;Poh Chiang; Miao Zhu; Feng Gao; Frede Blaabjerg, " Generalized Multicell Switched- Inductor and Switched Capacitor Z Source Inverters" , IEEE Trans. On Power Electronics, vol. 28, No.2, pp. 837–848, Feb-2013.
[15] H.bu-Rub;A.Iqbal;S.K.Moin Ahmes,F.Z.Peng ;Y.Li ;G.Baoming, " Quasi Z source inverter based photovoltaic Generation with maximum power tracking control using ANFIS", IEEE Trans. On Sustainable Energy2012.
[16] Minh-Khai Nguyen; Young-Cheol; Sung-Jun Park, "Improved Trans Z Source Inverter with Continous Input Current and Boost Inversion Capacity", IEEE Trans. On Power Electronics, vol. 28, No.10, pp. 4500–4510, Oct-2013.

N.Shobanadevi received her Bachelor of Electrical and Electronics Engineering from Alagappa Chettiar College of Engineering, Madurai Kamaraj University, Tamil Nadu, India in 1996 and her Master of Engineering in Power Electronics and Drives from the JJ College of Engineering, Anna University Chennai Tamilnadu, India in 2004 .She is with the Department of Electrical and Electronics Engineering in the University College of Engineering, Ariyalur, India. Currently she is working towards his Ph.D. at Anna University, Chennai, India. Her research interest includes power electronics circuits, renewable power conversion systems and solid state control of electrical drives.

Dr.V.Krishnamurthi Graduated from one of the prestigious institutes, College of Engineering, Guindy, Chennai, he served as Lecturer and Reader in Annamalai University, Chidambaram for eight years. Then he joined as Asst. Professor at the College of Engineering, Guindy, Chennai. Under quality improvement program, he was deputed to IIT, Madras for Ph.D. research. His research work on "Modeling and Analysis of Large Scale systems" has been acclaimed internationally. He has published more than 50 research papers in international and national journals including IEEE Transactions. In appreciation of his teaching and research works, the American Biographical Institute has awarded him with 2000 millennium Award of Honour. He was promoted as Professor in ECE Department in 1978 when the Anna University was formed and as Head of the Department. He has

guided many Ph.D. research scholars and at present is guiding 6 scholars. His present interest is Communications, computers, neural networks and Electric Drives and controls.

Dr.N.Stalin graduated with an engineering degree from Bharathidasan University. He proceeded to obtain his Master and Ph.D. in National Institute of Technology (NIT), Tiruchirappalli, now working as a Assistant professor in Anna University, Tiruchirappalli. He has an academic career spanning over 12 years in which he is successfully guiding 7 Ph.D. Research scholars, 25 M.Tech. Dissertations and 32 under-graduate projects. He has published more than 30 papers at national and international journals and conferences. He has conducted over 15 workshops/ training programmes/ short-term courses for practicing engineers and faculty of engineering institutions. He has received best paper award in the international conference conducted by Pondicherry Engineering College, Pondichery .He is the life member of ISTE, AICHE, and ISC. He has presented more than 15 guest lecturer in the training programmes. He has developed 8 energy efficient models for industrial and home applications.