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Evaluation and Analysis of Bidirectional and Unidirectional Routers For Network-On-Chip

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Abstract

Network on Chip (NoC) router plays an important role for System on Chip (SoC) embedded applications. Routing is quite challenging for SoC chip design due to large number of circuits on single Integrated Circuit (IC) which has millions of transistors onboard. The NoC router is, therefore, required to be designed carefully to enable efficient routing operations on the SoC board. It may have more delay for priority operations required by various input channels. The unidirectional router consumes more area on chip. If any path failure occurs, the unidirectional router cannot route the data through other output channel. To address this problem, a novel bidirectional NoC router with and without contention is proposed. It occupies less area on chip and has high speed compared to an existing unidirectional router. The proposed bidirectional router can route the data from any input channel to any output channel. It avoids conflicts and path failure problems. If any path fails, it will immediately take the alternative path through the switch allocator. Simulation is performed by using ModelSim6.3c and synthesis is carried out on Xilinx10.1 platform. The proposed bidirectional NoC router is implemented on FPGA Spartan3 development board and its performance are verified. The results prove that the proposed bidirectional router is suitable for high frequency operation and has reduced delay. It is of smaller size on-chip and much useful for network designs

Keywords: Bidirectional NoC router, Contention free router, Priority based Round Robin Arbiter (RRA), Switch allocator, Unidirectional NoC router.

Introduction

System on Chip (SoC) combines many smaller IC modules on a single chip which is normally designed for VLSI circuits and systems of higher complexities. It may

have multiple IP core processes on single chip. . The process of system on chip is much useful and has many advantages. Normally the cores make up an SoC module with interconnection architecture and interfaces with several peripheral devices simultaneously. The interconnection architecture is designed in one of the two ways based on dedicated wires or shared bus. The routing using dedicated bus is effective only for systems with a small number of cores. The number of wires in the system increases exponentially with the number of cores. It can be concluded that the dedicated wires have no reusability and flexibility. A shared bus is a set of wires commonly available for use by several cores. This scheme is reusable and easily scalable compared to dedicated bus. On the other hand, bus allows only one communication transaction at a time. Thus, all cores share the same communication channel. Bandwidth of the system and scalability is limited to a few dozen of IP cores. Using separate busses interconnected by bridges or hierarchical bus architectures may be better option. Different buses may operate on different protocols and may have different bandwidth requirements for expanded parallel communication. The scalability is very difficult for hierarchical bus architectures. A Network on Chip (NoC) scheme appears better solution for implementing SoC interconnection architectures. Normally an NoC is a collection of interconnected switches. The switches have the IP cores interconnected. NoC's have better bandwidth, scalability and performance compared to a shared bus [1] [2] [3] [4].

Routers are responsible for receiving incoming packets, storing packets, routing packets to an output port and onward transmitting packets to other switches. To achieve these tasks, four most important components play a major role in a crossbar switch operation. It consists of a router to provide interconnect path between input and output channel. The second important component is buffer which is a temporary storage device to store the intermediate data. The third important component is an arbiter to grant access to a given port if multiple input requests are made simultaneously. The fourth important component is flow control module to regulate the data transfer among many switches. The type of architecture and dataflow control may affect the design of NoC arbiter considerably. The arbitration is required to keep the fairness, make scheduling operation and maintain high speed all the times. The NoC switches should have high throughput and cost-effective resolution. It should route multiple packets from different input channels to output channel [5]. A fast arbiter is desirable for high speed NoC switches. The speed of the arbiter is considerably significant for a given NoC design [6] [7].

The NoC router is a very important component for on chip network. It performs a critical operation of coordinating the data flow. The network router operation involves two fundamental rules, the first rule related to associate control logic and the second rule involves the data path. The data path contains number of input and output channels to make easy packet transfers among switches. Usually 5×5 input and output routers are used in NoC router. Out of five ports, four are in cardinal direction (North, South, East and West) and one port is connected to its local Processing Element (PE). The router is the most important component for the NoC design and it constitutes a back-bone of NoC router. In a packet switched network router, the working principle of the router is to transmit an incoming packet to the destination port if it is directly connected to it. Next, it may transmit the packet to another router connected to it. It is desirable that the NoC design should be done in a

way that it should be as simple as possible. This is desirable because implementation cost increases with increasing the design complexity of a router. The design of router mainly consists of five parts, buffer, arbiter, crossbar, routing logic and channel control logic. In this paper, the authors have designed bidirectional router with and without contention situation by introducing virtual channel allocator, switch allocator and round robin arbitration schemes [8].

Conventional Unidirectional Router

Unidirectional router performs the routing operation in a single direction. Main drawbacks of this routing logic include occurrence of path failures, dead lock and live lock problem. The 5×5 Round Robin Arbiter consists of number of OR gates, AND gates and D flip-flops. As shown in Fig.1, five channels sent the request at the same time. Only one request is accepted at a given time. Similarly other requests are processed based on the priority of the data. Mask-able and Unmask-able priority arbiters are designed and implemented by using Round Robin Arbitration Technique [9]. An unmaskable arbiter is granted, if the previous grant output is zero. This gives an input for a two input AND gate. If the request is one, the OR gate output is one and the output is inverted. Next, it gives an input to AND gate. Likewise the priority is generated for different input data. Once the unmasked priority is enabled, the next masked priority is processed continuously in routing algorithms. It defines the path followed by a packet from source to target switch.

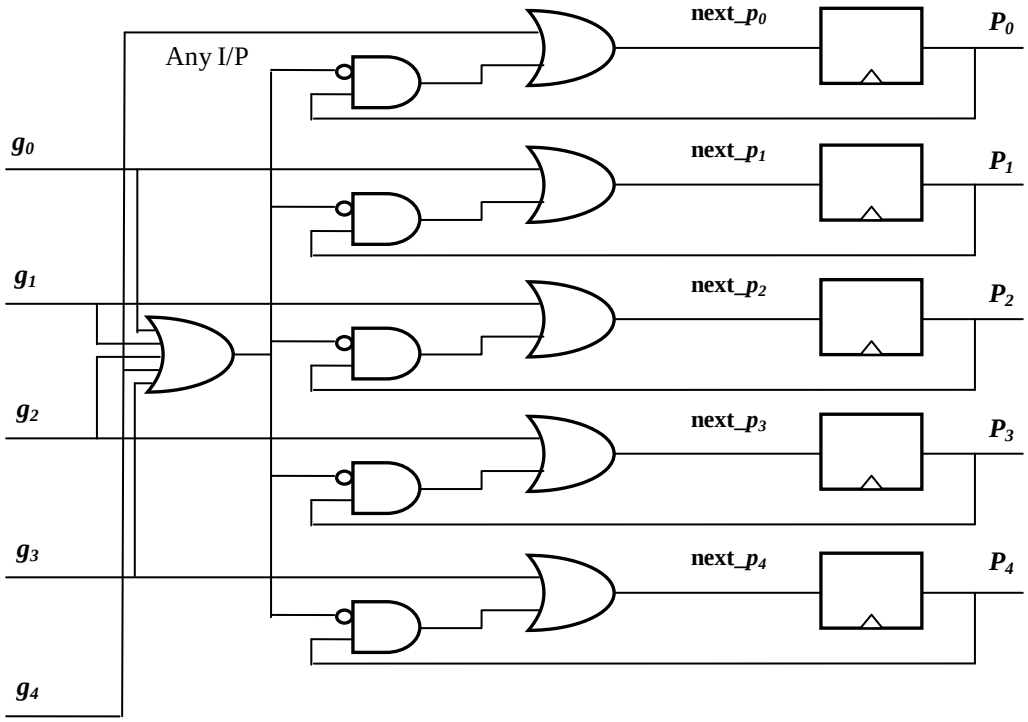

Figure 1: Circuit diagram of priority based 5X5 Round Robin Arbiter

The deadlock, live lock, and starvation situation should be avoided at all the times. Deadlock may be defined as a condition of nodes requiring access to sources

but cyclically keeps rotating without any forward development irrespective of any series of occurrences. Live lock is another condition in which the packets circulate in a network without moving towards intended destination. Starvation happens when a packet in a buffer requests an output channel but the output channel is always allocated to another packet and it never becomes available.

The routing algorithms can be classified into three different categories, the first refers to point where the routing decisions are taken, the second category refers to how a path is defined and the third is a path length. According to what routing choices are chosen, it is possible to categorize the routing as a source and distributed routing. The whole path is decided in source routing at the source switch, whereas in distributed routing each switch obtains a packet and describes the direction to send it. In source routing, the header of the packet carries all the routing information. It increases the packet size. The path can be chosen as a function of the network traffic conditions in distributed routing instantly. Distributed routing can also have path failures, resulting in fault tolerant algorithms.

Depending on selection of direction, routing can be divided as deterministic or adaptive. The direction is completely specified from the relative position of source and target addresses in deterministic routing. In adaptive routing, the direction is a function of the network's instantaneous traffic. Adaptive routing increases the number of possible paths usable by a packet to arrive to its destination. However, deadlock and live lock situations can happen in fully adaptive algorithms, which limit its usage. Regarding the path length criterion, routing can be minimal or non-minimal. Minimal routing algorithms guarantee shortest path between source and target addresses. In non minimal routing, the packet can follow any available path between source and target. Non minimal routing offers great flexibility in terms of possible paths, but can lead to live lock situations and increase the latency to deliver the packet.

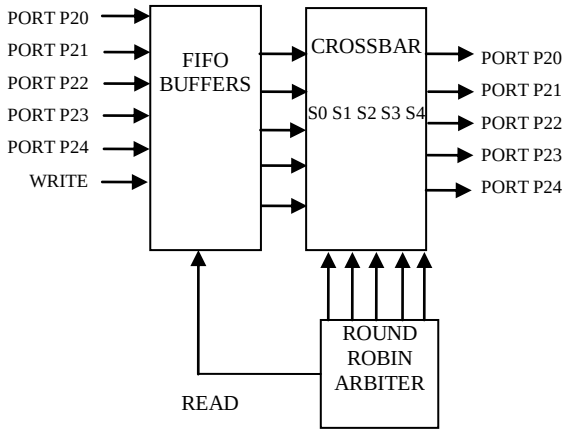

Figure 2: Block diagram of conventional unidirectional router

Conventional unidirectional router structure is shown in Fig. 2. It consists of Round Robin Arbiter module, First in First out (FIFO) buffers and crossbar switches. Arbiter is used to grant the data based on the priority. Higher priority data are routed

first. A FIFO buffer is used to store the data few times. It functions as a temporary storage device. These FIFO buffers are used in both input and output channel side. Crossbar switches is used to transfer the data, which comes from the arbiter. Channel control logic is incorporated in this router to send the control signal to crossbar switches. For example, input channel A can route the data through corresponding output channel A only, and cannot route the data via output channel B. Hence it is called unidirectional router [10].

Proposed Bidirectional Noc Router With and Without Contention

In this paper, the design of bidirectional Network on Chip router is presented. It avoids the contention situation. The Proposed Bidirectional NoC router architecture is shown in Fig. 3, which consists of In-Out port, Static RAM, Round Robin Arbiter, Routing Logic and Channel Control module. Arbiter is a type of device that chooses one output from a number of inputs based on the logic used. The number of input and output in crossbar switches are the same as in the arbiter. Normally, there are three parameters from the crossbar inputs which are to be identified. These are data, request and destination. Data is the information or the actual message to be routed. The information is to be routed to the output port for further processing. The address of the output port is included in destination information. The same address is used to find the path to send the information. The next parameter is request. If the request is activated then the data is routed from the corresponding input port.

If two or more packets send the request at the same time from the crossbar input, the round robin arbiter can enable only one request at a time. Hence only one packet can access the crossbar switch at a time. This may cause loss of a few data packets. To overcome this problem in a buffers of FIFO or memory (SRAM), an arbiter is incorporated. To obtain the lost packets, the output port of crossbar can be stored in FIFO or SRAM. The packet from the FIFO or SRAM can be transferred in next clock cycle. It is a contention free crossbar [11] [12].

To pair the input ports and output ports, an allocation or a matching process is performed in a router. One input port is paired with only one output port to avoid conflicts. Initially, the router architecture is designed to use for routing operation in the wired network, then it is implemented for the method of matching maximization for present and next allocations. Finally, it provides the exhaustive operations of a matching with the future requests. In First in First out (FIFO), the data read /write occur in an order. If an address pointer is incremented by one, FIFO full and empty flags point to the status of FIFO. The FIFO clears the data if the data is read from it. Random Access Memory (RAM) is a type of volatile memory, for which a read/write operation can be done randomly. This, however, is not possible in FIFO. It always starts from first address and the address pointer keeps on incrementing by one step at a time. If FIFO reads data from memory at a given address, immediately the data are cleared off memory whereas in case of RAM, the data are available even after the read operation has been accomplished [13] [14].

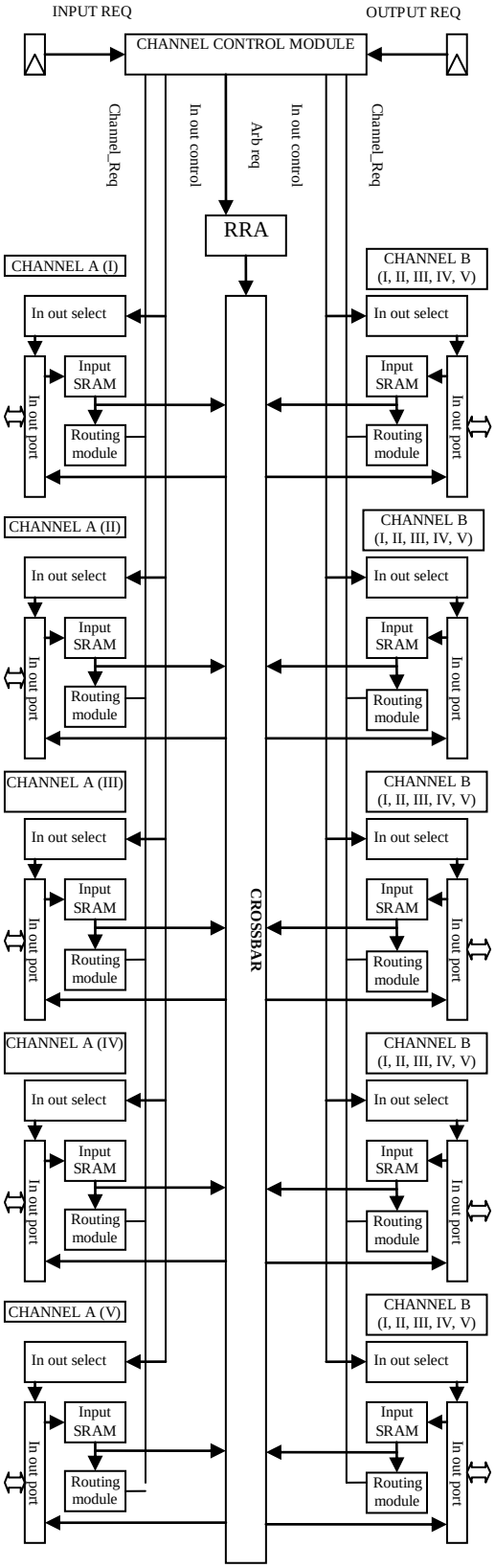

Figure 3: Architecture of proposed bidirectional NoC Router

Dynamic RAM (DRAM) consists of transistors and capacitors. The drawback of DRAM is that it needs periodical refreshment of charge to compensate leakage power through discharging of capacitors. Moreover, the operating rules are different in DRAM. Because of these factors, the performance of DRAM is poorer than Static RAM (SRAM). However, in DRAM chip size requirement is smaller than SRAM due to the fact that DRAM erases the data immediately after the data has been read off. The main advantage of SRAM is higher speed of it than the DRAM. Static RAM consists of thousands and thousands of transistors which occupy more area, but it has less leakage power due to performance enhanced transistors. It also improves the readability. In this paper, the proposed router is designed using SRAM to improve the speed of the router and reduce the leakage power. Round Robin Arbitration is incorporated to reduce the area and dynamic power consumption. The virtual channel allocator and the source allocator are used to control the channel. Virtual channel allocator is used to virtually change the corresponding channel direction and switch allocator is used to remove the path failures [15] [16].

The proposed Bidirectional NoC Router is used to transfer the data by three different methods. First, all input and output channels act as either slaves or masters. For example, if the first output channel acts as a slave, then the first input channel acts as a master. All other channels perform the routing operation in a similar way. Second, all the data from all input channels are routed through same output channel. This eliminates the path failures. Third, all input packets are transferred through all the output ports. These avoid the live lock and dead lock problems. Also the proposed bidirectional NoC router uses less on chip area and performs at higher frequency than the conventional unidirectional router [17] 18]. The area and delay are reduced due to incorporation of an efficient routing logic in the proposed bidirectional router [16] [19] [20] [21] [22].

Results and Discussion

The design of bidirectional NoC router with and without contention is a main goal of this research work. The proposed router is designed using Verilog HDL programming platform. Performance analyses are done for unidirectional and bidirectional NoC routers in a comparative manner. Experimental simulations are done on ModelSim6.3c. Synthesis is verified by using Xilinx10.1. Contention free bidirectional NoC router is designed using SRAM to store the data until the next clock cycle arrives. Simulation results show that the SRAM supports high speed and has low leakage power in overall system. Crossbar switches with Round Robin Arbitration scheme is used to eliminate the path failures that may occur. Simulation result of conventional unidirectional NoC router is shown in Fig. 4.

The Fig. 4 illustrates a 5×5 unidirectional routing technique. For the first clock cycle reset is *zero* and corresponding channel inputs are *100, 200, 44, 144* and *244*. Based on the request, the inputs are routed to corresponding destinations as indicated. If the request is *one* and reset is *one*, first local channel input *100* is routed to first output channel and the same data cannot be routed through any other channel. Similarly, second input *200* is transferred through second output channel only, if and only if the request is *eight*. Next, fourth channel data, *144*, are routed

through fourth output channel, if and only if the request is two. Likewise all other data are routed through corresponding output channels in the same way. If path failure occurs, the data cannot be routed through unidirectional router. It may cause data loss.

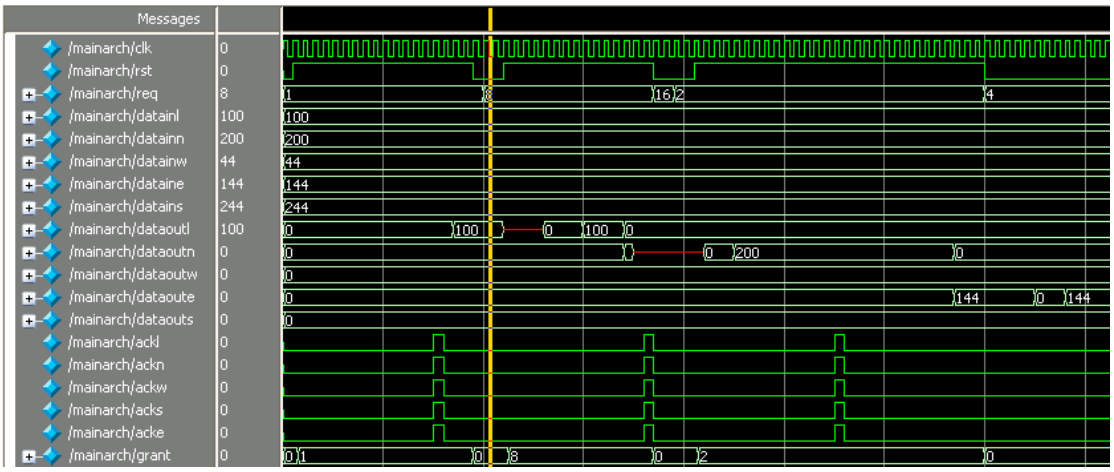

Figure 4: Simulation result of unidirectional NoC router

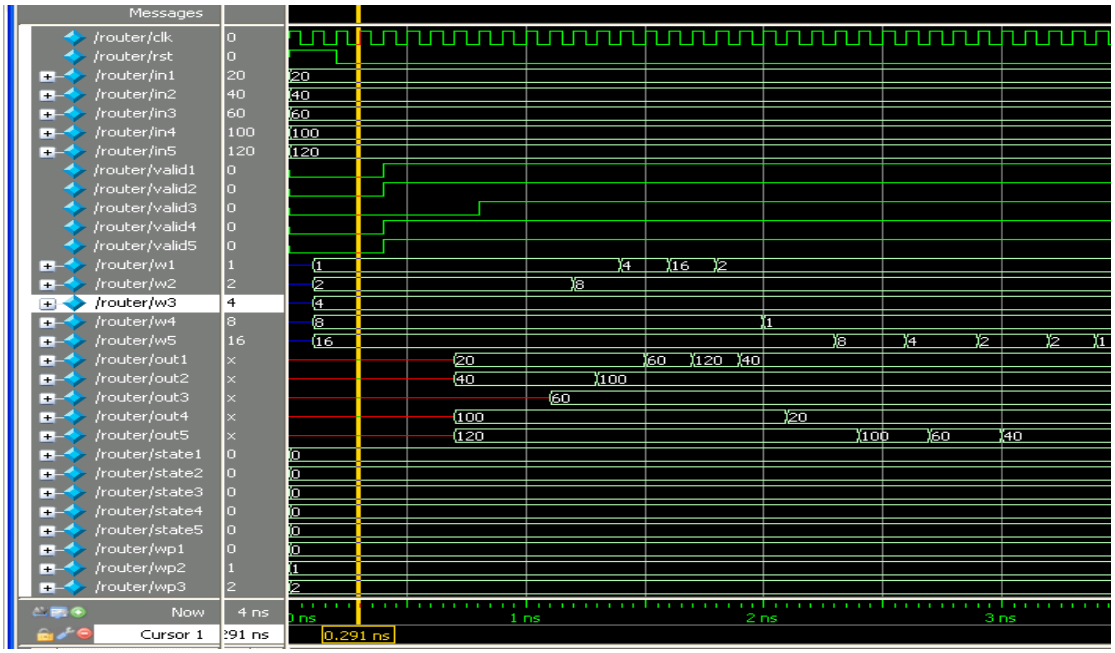

Figure 5: Simulation result of proposed bidirectional NoC router

The proposed bidirectional NoC router is designed and verified by simulating it. The results of simulation are shown in Fig. 5. If reset is active high, all the outputs are *zeros*. The outputs are generated only if reset is low. The information or data for channel1 is *20*, input channel2 is *40*, input channel3 is *60*, input channel4 is *100* and input channel5 is *120* (Fig. 5). As seen in the Fig. 5, if valid data signal goes high, then the valid information of input channel is transmitted.

From *w1* to *w5* are the 5 bit requests for all the input channels. A hot bit encoding technique is used to enable request. For example, *w1=0000*, the first input data is *20*, which is routed through first output channel; *w1=00010*, the second input data is *40*, which is routed through first output channel; *w1=00100*, the third input data is *60*, which is routed via first output channel; similarly all the inputs (*1* to *5*) are routed through first output channel only, if *w1* request is enabled. This is called contention free routing. With contention means that if first channel input is *20*, which is transferred through any output channel, i.e. output channel1 get the first data value *20*, if the *w1=1*; output channel2 get the first data value *20*, if the *w2=1*; output channel3 get the first data value *20*, if the *w3=1*; output channel4 gets the first data value *20*, if the *w4=1*; and output channel5 get the first data value *20*, if the *w5=1*. This is called contention situation. Therefore first data *20* can be transferred through any output channel based on the corresponding grant signal.

The number of occupied slices in case of unidirectional NoC router is *1202*. Further, the number of slices is reduced to *260* in the bidirectional NoC router. The delay utilization in case of unidirectional NoC router is *5.6* ns, which is reduced to *2.213* ns in case of bidirectional NoC router. The frequency utilization in unidirectional NoC router is *178.575* MHz, which is increased to *451.896* MHz in bidirectional NoC router. The comparison results are illustrated in Table 1. Performance comparison of bidirectional NoC router with unidirectional NoC router in terms of slices, delay and frequency are shown in Fig. 6. On comparing the above router circuits in terms of chip size and speed utilization, it can be seen that the bidirectional NoC router offers 78% less area compared to other circuits. Also the frequency of proposed bidirectional NoC router is increased by a margin of *60%* compared to the unidirectional NoC router.

Table 1: Result performance of unidirectional and bidirectional NoC routers

NoC Router	Slices	Frequency (MHz)	Delay (ns)
Unidirectional Router	1202	178.575	5.600
Bidirectional Router	260	451.896	2.213

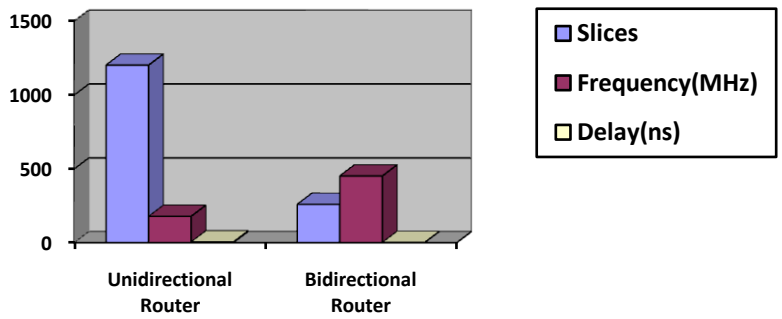

Figure 6: Performance analysis of bidirectional router over unidirectional router

Conclusion

A high speed and small in size bidirectional NoC router is proposed with and without contention in this research paper. The new bidirectional NoC router is compared with the conventional unidirectional router for the performance and results. By simulation and analysis it is concluded that the proposed bidirectional router occupies small area compared to unidirectional router. The simulation result shows that the proposed bidirectional NoC router can operate at higher speed with reduced delay compared to the conventional unidirectional NoC router. The bidirectional router provides optimized area reduction by a 78% and delay reduction by a 60% margins as compared to conventional unidirectional NoC router. The bidirectional router is used to avoid dead lock and live lock conditions through channel control techniques. For removing the contentions; all the input channels can send the request to all output channels at a same time. SRAM is used to store data during contention and it can release the data in the next clock cycle based on grant signal sent by round robin arbiter. The proposed NoC router may be used in System on Chip applications for efficient on chip routing process. The future work may include further improvement and scalability of NoC router.

References

[1] Amit Kumar Lamba, Bharati B. Sayankar and Pankaj Agrawal, "Performance Analysis of Speculative Virtual Channel Router for Network -On-Chip". European Scientific Journal, Vol. 3, February 2014.

[2] Anh T. Tran and Bevan M. Baas, "Achieving High-Performance On-Chip Networks With Shared-Buffer Routers". IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 6, June 2014.

[3] Arthur Pereira Frantz et al., "Crosstalk- and SEU-Aware Networks on Chips". IEEE Design & Test of Computers, IEEE, 2007.

[4] Arun Arjunan and Karthika Manilal, "Noise Tolerant and Faster On Chip Communication Using Binoc Model". International Journal of Modern Engineering Research (IJMER), Vol. 3, Issue. 5, Sep - Oct. 2013.

[5] Ashish Khodwe and Prof. C. N. Bhoyar, "Efficient FPGA Based Bidirectional Network on Chip Router through Virtual Channel Regulator". International Journal of Advances in Engineering Sciences Vol.3 (3), July, 2013.

[6] Bhavana Pote, V. N. Nitnaware and Dr. S. S. Limaye, "Optimized Design of 2D Mesh NOC Router using Custom SRAM & Common Buffer Utilization". International Journal of VLSI design & Communication Systems (VLSICS) Vol. 2, No.4, December 2011.

[7] Cédric Killian, Camel Tanougast, Fabrice Monteiro, and Abbas Dandache, "Smart Reliable Network-on-Chip". IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE, 2013.

[8] En-Jui Chang, Hsien-Kai Hsin, Shu-Yen Lin, and An-Yeu (Andy) Wu, "Path-Congestion-Aware Adaptive Routing with a Contention Prediction Scheme for Network-on-Chip Systems". IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 33, No. 1, January 2014.

[9] Manjushree.k.chavan and Yogeshwary. B.H, "Reusability of test bench of UVM for Bidirectional router and AXI bus". International Journal of Computational Engineering Research (IJCER), Vole 04, Issue 4, April, 2014.

[10] Minakshi M. Wanjari, Dr. R. V. Kshirsagar and Dr. Pankaj Agrawal, "Implementation of Buffer for Network on Chip Router". International Journal of Technological Exploration and Learning (IJTEL), ISSN: 2319-2135, Vol.3, No.1, February 2014.

[11] Rajalingam, A. and Bechtel Brabi, "An Effective Bidirectional Network on Chip with Pipelining and Self Reconfigurable Channel". Research Journal of Applied Sciences, Engineering and Technology 7(22): 4714 - 4719, 2014.

[12] Sahar Foroutan, Yvain Thonnart, and Frederic Petrot, "An Iterative Computational Technique for Performance Evaluation of Networks-on-Chip". IEEE Transactions on Computers, Vol. 62, No. 8, August 2013.

[13] Saravanakumar U, Anil Krishna Galla, Arun R, Abhishek Prabhu P, "Implementation of Wormhole Router with Low Power Buffer Management". International Journal of Computer Science and Technology (IJCST), Vol. 4, Issue 4, Oct - Dec 2013.

[14] Saravanakumar, U. and Rangarajan, R., "Design and Performance Evaluation of on Chip Network Routers". Journal of Theoretical and Applied Information Technology, Vol. 52, No.2, June 2013.

[15] Si Qing Zheng and Mei Yang, "Algorithm-Hardware Co design of Fast Parallel Round-Robin Arbiters". IEEE Transactions on Parallel and Distributed Systems, Vol. 18, No. 1, January 2007.

[16] Subhananthan, N. and C. G. Joy Merline, "Efficient and Advance Routing Logic for Network on Chip". International Journal of Engineering Research and Applications (IJERA), March, 2014.

[17] Subhasakthe, S. A., Manoj, K. K. and Mithunraj, S., "A Reliable Flexi-Router Architecture for NOC Applications". International Journal of Emerging Technology and Advanced Engineering, Volume 4, Issue 1, January 2014.

[18] Suyog K.Dahule, M.A.Gaikwad, "Design & Simulation of Round Robin Arbiter for NoC Architecture". International Journal of Engineering and Advanced Technology (IJEAT), ISSN: 2249 – 8958, Volume-1, Issue-6, August 2012.

[19] Thomas Canhao Xu, Pasi Liljeberg and Hannu Tenhunen, "Exploring DRAM Last Level Cache for 3DNetwork-on-Chip Architecture". International Conference on Embedded System and Microprocessors (ICESM 2010), IEEE, 2010.

[20] Turhan Karadeniz et al., "Hardware Design and Implementation of a Network-on-Chip Based Load Balancing Switch Fabric". IEEE, 2012.

[21] Young Jin Yoon, Nicola Concer, Michele Petracca, and Luca P. Carloni, "Virtual Channels and Multiple Physical Networks: Two Alternatives to Improve NoC Performance". IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 32, No. 12, December 2013.

[22] Zhiliang Qian, Ying Fei Teh and Chi-Ying Tsui, "A Flit-level Speedup Scheme for Network-on-Chips Using Self-Reconfigurable Bi-directional Channels". EDAA, 2012.