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Survey on Efficient and Accurate Method For Multiple Fault Diagnosis Technique

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Abstract

Diagnosing the fault is very important to analyses the physical failure and Yield learning. Billions of transistors integrated in a single chip, so multiple faults will appear. The fault masking and reinforcing effects will appear in multiple fault cases. Single-fault-based diagnosis methods such as the single location at a time (SLAT) to be invalid because there are not enough SLAT patterns that can be explained by a single stuck at fault. In a real silicon defect behave as different fault models. The SLAT approach invalid in different failing patterns. So here initiate the concept of fault element to support multiple fault models and use of fault element graph to consider fault masking and reinforcing effects among multiple faults. Based on the fault element graph is of all failing patterns, the most fault locations and their fault elements are iteratively identified. This fault element graph mainly used in multiple fault locations are identified. Such that increase the speed of diagnosis the faults, and reduce the testing time.

Keywords: multiple fault model; multiple faults; Fault diagnosis; fault element; fault element graph.

Introduction

Testing and diagnosis are the two primary role to ensure the reliability of the system. Testing is done to check whether the system behaves correctly. If incorrect behaviour detected, second goal is Testing and diagnosis are the two primary role to ensure the reliability of the system. Testing is done to check whether the system behaves correctly. If incorrect behaviour detected, second goal is locate or diagnose the fault.

Diagnosing the fault is very important to analyse the physical failure and Yield learning process. Quick yield learning is very important in the semiconductor industry, where the short marketing profit window of integrated circuits mandates quick time-to-market and time-to- volume [1]

A fault model is an engineering model of something that could go wrong in the construction or operation of a piece of equipment. The designer or user can then predict the effect of this particular faultBasic fault models in digital circuits includes The stuck-at fault model - a signal, or gate output will stuck at high(1) or low(0) value, The bridging fault model- two signals are connected together. Depending on the logic circuitry employed, this may result in a wired-OR or wired-AND logic function. Transistor faults- In This model is used to report faults for CMOS logic gates, here transistor will stuck-short or stuck-open. Stuck-short will make a short between VSS and VDD and Stuck-open causes a transistor never conducts current (or stuck-off) The open fault model- Here a wire is assumed open or disconnected from the output line. (v)The delay fault model- the signal gets value more slowly (or quickly) than normal.A fault model, falls under one of the following assumptions: (i) single fault assumption-only one fault occur in a circuit. multiple fault assumption, (ii) multiple faults may occur in a circuit.When multiple faults exist, a single- fault model is inadequate to accurately locate the actual faults [2].

Single stuck-at (SA) fault model more than 41% of the faults cannot be accurately diagnosed. Multiple-fault diagnosis is challenging because: (i) a real silicon defect can behave as different fault models (DM) under different patterns, such as a fault behaving as an open fault under some patterns but as a bridging fault under some other patterns and (ii) multiple faults may cause fault masking and reinforcing effects when a fault effect is interfered by others. According to the patterns used by fault diagnosis, diagnosing multiple combinational logic faults can be classified into two categories: diagnostic- pattern-based diagnosis methods and manufacturing- test-pattern-based diagnosis methods [3].

Diagnostic-pattern-based diagnosis methods usually achieve high diagnosis quality, it is expensive to load diagnostic patterns to an automatic test equipment for a second run of test. For the manufacturing-test-pattern-based diagnosis methods, no diagnostic patterns are generated and used. Failure chips failing responses under manufacturing test patterns are compared with potential faults' failing responses to find the candidate faults [4].

This diagnosis method targets multiple combinational logic faults under DM for scan-based circuits. Thus, in the following context, inputs refer to primary inputs and pseudo primary inputs (scan cells), and outputs refer to main outputs and pseudo primary outputs (scan cells). The diagnosis result contains ranked candidate locations and their fault elements. A fault element describes a fault location and its faulty value under a pattern. It support the diagnosis of a real silicon defect that behaves as DM under different failing patterns. Using fault elements with the layout information, the candidate locations and the behavior of real silicon defects are identified. To handle the issue of fault masking and reinforcing effects among multiple faults, fault-element graphs are constructed to describe the combined effects of multiple fault elements. Unlike previous approaches that consider one fault at a time to identify multiple

faults, our approach identifies the multiple faults by using FEGs to keep track of multiple-fault effects. Based on FEGs of all failing patterns, the candidate locations and their fault elements are iteratively identified with FEGs pruned iteratively and All the FEGs are reduced to null, until all the fault locations are identified[5]. In section 2 describes the methods of diagnosing multiple faults under different fault models, Section 3 FEG construction and scoring, section 4 describes conventional system of diagnosing multiple faults. Section 5 describes literature summary. Section 6 describes conclusion.

Methods of Diagnosing Multiple Faults Under Different Fault Models

The diagnosis of this method consists of failing pattern for FEG is constructed. An FEG describes the combined effects of multiple fault elements. Each vertex in an FEG represents a fault element, and relation between the corresponding fault elements is represented by each directed edge. The construction of FEGs in Section 3 in detail. During the FEG construction, each fault element is scored to keep track of its contribution to faulty values at all outputs. To ensure correct scores of all fault elements, fault masking and reinforcing effects are considered accordingly. The solutions are identified based on the fault-element scores and FEGs of all failing patterns. The candidate locations in a solution are iteratively selected. At First, the fault locations with the highest score are selected based on the fault-element scores. All the FEGs are pruned by removing the fault effects of the selected candidate locations fault elements, if there is only one candidate location with the highest score. The scores of all remaining fault elements in the FEGs are updated accordingly. If there is more than one candidate location with the highest score, and they have different fault masking or reinforcing effects to other faults, or produce different failing outputs. To avoid the missing correct solutions, we analyze them separately in parallel. Until all the FEGs become null, this process is repeated.

Feg Construction and Scoring

An FEG is constructed by tracing backward in a breadth-first order from failing outputs to circuit inputs for each failing pattern. When tracing, fault elements are identified and their scores are calculated based on their contribution to faulty values at all outputs by considering the fault masking and reinforcing effects among multiple faults. If there is a circuit with three fault locations q, b,and c. Three faults produce three failing patterns. Each location has specific good machine value which is written aside the location label. Each failing pattern of FEG is given below the circuit.In the FEGs, each vertex represents a fault element, and each line directed from the edge represents the relation between corresponding fault elements The fault element score is written below the fault-element label in the vertex.Then iterative process is started. Some candidate locations and their fault elements are selected, and the candidate locations selected in the preceding procedure will guide the selection of candidate locations in the succeeding procedure.Final diagnosis results is obtained by ranking the all candidate locations.

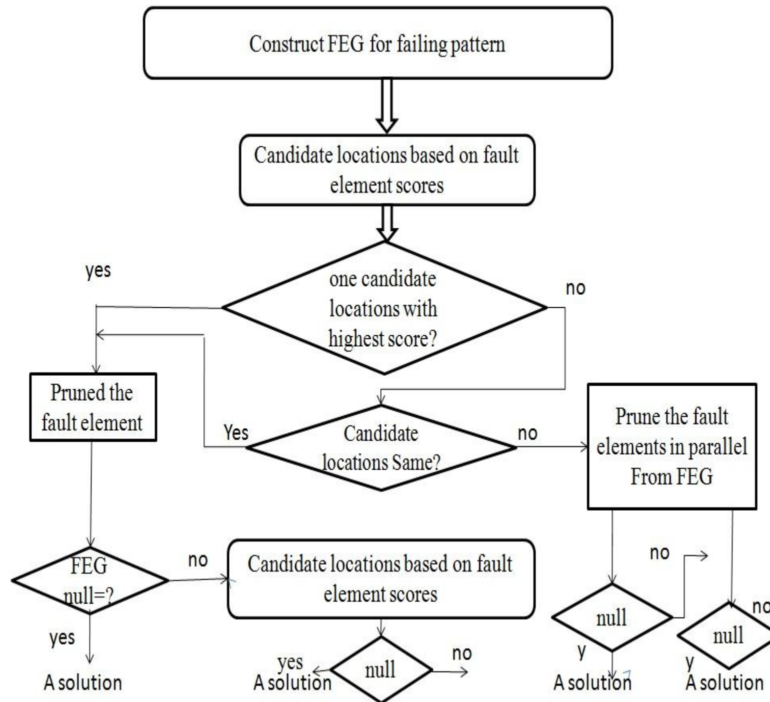

Figure: Flow of Diagnosis Method

Conventional System of Diagnosing Multiple Faults

Aitken, R.C (1997)
Because defect behavior is so variable, a fault model always leaves some faults unmodeled. One solution is to use improved matching algorithms to diagnose complex behaviors even with inaccurate modeling. However, when multiple faults exist, a single fault model is inadequate to accurately locate the actual faults.

L. M. Huisman (2004)
This paper discribes A new form of logic diagnosis is described that is suitable for diagnosing fails in combinational logic. It can diagnose defects in the integrated circuit. It manage by first identifying patterns during which only one element is affected by the defect, and then diagnosing the faults observed during the application of such patterns, one pattern takes at a time. Single stuck-at faults are stuck-at fault locations thus identified is then further analyzed to obtain the most accurate estimate of the identities of those elements that can be affected by the defect. This proposal to logic diagnosis is as effective as that of classical stuck-at fault-based diagnosis, when the final applies, but is far more general. In specific it can diagnose fails caused by bridges and opens as well as fails caused by regular stuck-at faults. Experiments in show that more than 41% of the faults cannot be accurately diagnosed when using only the single stuck-at (SA) fault model.

Y-C Lin et al(2007)
In this paper they showed two fault-diagnosis methods for improving multiple-fault diagnosis resolution. In first method, based on the concept of single-fault activation and single-output inspection it employs a new circuit transformation technique in conjunction with the use of a special type of diagnostic test patterns, named single-observation single-location-at-a-time (SO-SLAT) pattern. For a list of candidate suspects, a set of SO-SLAT patterns is generated, each of which attempts to operate only one fault in the list and propagate its effects only to a specific observation point. For noticing the responses of the circuit under diagnosis, SO-SLAT patterns helps more precisely to determine each fault suspect is a true or false candidate. This procedure can tolerate most of the timing hazards for a more accurate diagnosis of failures caused by timing faults. Other method generates and applies limited-cycle sequential test, to identify multiple defective signals which can jointly explain the circuit's faulty behavior. These two methods can be applied separately and/or jointly after any existing state-of-the-art diagnosis process to further improve the diagnosis resolution. Experimental results expresses the effectiveness of the proposed methods for diagnosing multiple faults, contain timing faults.

A. Smith et al(2004)
Recent advances in Boolean satisfiability have made it an attractive engine for solving many digital VLSI design problems such as conformation, model checking, optimized pattern generation. Fault diagnosis and logic debugging have not been direct by existing satisfiability-based solutions. To bridge this space by proposing a satisfiability-based solution to these problems, the initiated formulation is intuitive and easy to implement. It shows that satisfiability catches significant problem characteristics and it offers different trade-offs. It also gives new opportunities for satisfiability-based diagnosis tools and diagnosis-specific satisfiability algorithms. Theory and demonstration validate the claims and demonstrate its potential diagnosis method to target multiple combinational logic faults under DM for scan-based circuits. In the following context, inputs refer to main inputs and pseudo primary inputs (scan cells), and outputs refer to main outputs and pseudo primary outputs (scan cells). The diagnosis result hold ranked candidate locations and their fault elements.

B. Boppana et al(1999)
In this paper, multiple error diagnosis algorithms are used to overcome two significant problems associated with current error diagnosis techniques targeting large circuits, their use of limited error models and a lack of solutions that scale well for multiple errors occurred. The solution is based on a non-enumerative analysis technique, based on logic simulation for simultaneously analyzing all possible errors at sets of nodes in the circuit. Error models are introduced in order to address the locality aspect of error location and to identify sets of nodes that are local with respect to each other. Theoretical results are provided to guarantee the diagnosis of modeled errors and robust diagnosis approaches are shown to address the cases when errors do not correspond to the modeled types. Experimental results on

benchmark circuits demonstrate accurate and extremely rapid location of errors of large multiplicity. The X-fault model is used to represent the unknown behavior of potential faults, that can produce more matched failing outputs and cause less passing outputs to fail are ranked higher in the reported candidate fault list. Fault masking and reinforcing effects among multiple faults are not specified [6].

Saqib Khursheed et al (2009)
In this paper, they discusses the usage Multiple voltage diagnosis method which is commonly used and effective dynamic power reduction design technique in low-power ICs. The purpose of this paper is to propose a method for diagnosing bridge defects. The impact of varying supply voltage on the accuracy of diagnosis demonstrated how the additional voltage settings can be leveraged to improve the diagnosis resolution through a novel multivoltage diagnosis algorithm. It also identifies the most useful voltage settings to reduce diagnosis cost by eliminating tests at certain voltage setting thereby achieving high diagnosis accuracy at reduced cost. It target bridging faults. For every candidate fault location, they extract the nets nearby the candidate location. Then, with the information about whether the candidate fault is activated or not under each pattern, the valid range of bridging resistance between the candidate location and its nearby nets at layout could be calculated. If no valid range of bridging resistance exists, the candidate location will be removed [7].

X. Yu et al(2010)
This paper describes a multiple-defect diagnosis methodology that is flexible in handling various defect behaviors and arbitrary failing pattern characteristics. The search space of the diagnosis method does not grow exponentially with the number of defects. This method can efficiently diagnose circuits that are affected by a large (>20) or small number of defects of various types. This method is capable of accurately estimating the number of defective sites in the failing circuit can be used regardless of whether failing patterns are SLAT or not. They analyze the faults propagation capabilities, faults that are easier to be propagated to the failing outputs and are harder to be propagated to the passing outputs are ranked higher in the reported candidate fault list [8].

H. Takahashi et al(1993)
In this paper they showed the method for determining the set of all possible stuck-at faults from the faulty response observed at the primary output based on deducing internal values along the sensitized path. Multiple stuck-at fault diagnosis in combinational circuits are based on restricted single sensitized paths generated by a seven-valued calculus. The fault-free lines are removed along the sensitized path by using the fault-free response observed at the primary output, from the set of the candidates and checking whether the fault-free response is prevented by the candidate fault from propagating to the primary output regardless of the presence of any other candidates. Experiment results on the benchmark circuits show that the fault locations are identified within 2-25% of all stuck-at 0 and 1 faults on all lines in the circuit with up to fourfold multiple faults without probing internal lines. Here failure chips failing

responses under manufacturing test patterns are compared with potential faults failing responses to find the candidate faults [9].

M.-J. Tasi et al(2009)
The fault diagnosis has become an increasing portion of today IC-design cycle and significantly determines product time-to-market. The failure behaviors from the defective chips may not be fully represented by the single fault model. A fault-diagnosis framework targeting multiple stuck-at faults and all real faults are topologically covered. A proposed ranking method is applied to sieve out the real faults from the candidates within the suspect region. The experimental results shows that the proposed diagnosis framework can effectively locate the multiple stuck-at faults within a location, which may generate erroneous signals cancelling one another and are difficult to be diagnosed based on a single-fault-model method[10].

W. C. Tam et al(2008)
This paper discusses the software-based diagnosis of failing chips and typically identifies several lines where the failure is believed to reside. The physical failure analysis is difficult because these lines can span across multiple layers. There are emerging diagnosis techniques that identify both the faulty lines as well as the neighboring conditions for which an affected line becomes faulty. The approach presented here is to improve failure localization by automatically analyzing the information associated with the outcome of diagnosis. Experimental results shows that a significant improvement in failure localization is achieved when this method is applied to real IC failures and independent of specific fault models. They use the concept of fault-tuple to extract the fault activation conditions of candidate faults. The candidate fault will be removed, if any conflicts are found among the fault activation conditions of a candidate fault, It also attempts to narrow down the candidates by analyzing the candidate fault elements with passing bits and layout information[11].

C.-W. Tzeng et al(2009)
This paper presents a layout-based methodology to predict the exact physical location of a bridging defect inside a standard cell and it involves a number of techniques. Most likely intracell bridging defects are identified through layout analysis and then converted into equivalent logic models. A new defect-oriented formulation is used to generate test pattern for each candidate defect so as to further enhance the diagnostic resolution. This methodology can remove 90% false defect candidates beyond gate-level diagnosis for four real designs and ISCAS'85 benchmark circuits. It targets intracell faults and performs transistor-level simulations to obtain the activation conditions and the behaviors of intracell faults. The candidate faults without reasonable activation conditions are removed [12].

D. Lavo et al(2002)
This paper discusses the advantages and disadvantages of using "one test at a time" fault diagnosis. Its ability is to implicate the components of complicated defect behaviors and the disadvantage is the large size and opacity of the diagnostic answer.

The problems of per-test diagnosis is eliminated by improving the candidate matching, introduce scoring and ranking methods, and by developing a method to translate the results into common defect scenarios. By considering passing test results we improve a common case where per-test algorithms can perform significantly worse than traditional diagnosis algorithms. Candidate analysis provides a way to bridge the per-test approach with traditional model-based fault diagnosis. The candidate faults are chosen from the single fault that can explain the SLAT patterns. As few candidate faults as possible are chosen to explain all the SLAT patterns. But SLAT patterns do not always exist and if they exists, its patterns may be too few to achieve high diagnosis quality [13].

Literature Summary

A detailed survey conducted shows the importance of fault diagnosis in increasing yield. The conventional single-fault-based diagnosis methods such as the single location at a time (SLAT) to be invalid because it is inadequate to accurately locate the actual faults when multiple fault exists. It also requires plenty of fault simulations to find candidate fault combinations to explain all the failing patterns and to identify complex fault defects. The multiple error diagnosis algorithms can be used for large circuits, their use of limited error models and a lack of solutions that scale well for multiple errors. But, Fault masking and reinforcing effects among multiple faults are not specified. The Fault Element Graph based multiple fault model considers fault masking and reinforcing effects among multiple faults. It eliminates the requirement of. This method can identify the locations of multiple faults even under DM with high diagnostic accuracy and resolution In the proposed method, multiple fault locations are identified and reduce the area, and testing time required.

Conclusion

This survey reveals about the importance of fault diagnosis and the method of diagnosing multiple faults at a time. The fault masking and reinforcing effects among multiple faults are addressed. Thus the fault element graph mainly used in multiple fault locations are identified. Such that, it increase the speed of fault diagnosis and reduce the testing time.

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