International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 4 (2015) pp. 10653-10664

http://www.ripublication.com

Low Power Implementation of 3-Weight Pattern Generation Based on Accumulator

C.Subashini[1], Dr. G. Saravanan Kumar[2] and Dr.S.Ravi[3]
[1]research Scholar ,Department of ECE, Dr.M.G.R Educational and research institute university, Chennai, India;
[2]Professor, Department of ECE, Vel Tech High Tech Dr. Rangarajan Dr. Sakunthala Engineering College, Chennai.
[3]Professor and Head, Department of ECE, Dr.M.G.R Educational and Research Institute University, Chennai, India

Abstract

A Pseudorandom pattern generator (PRPG) is used for generating test patterns (TPG). A weighted Pseudorandom built-in-self-test (BIST) schemes have been utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Weighted sets comprising three weights, namely 0, 1, and 0.5 have been successfully utilized so far for test pattern generation, since they result in both low testing time and low consumed power. While this objective still remains important, reducing heat dissipation during test application is also becoming an important objective, significantly higher during BIST than that during its normal operation. Excessive switching activity during test application can cause several problems. The proposed TPG reduces the number of transitions that occur at scan inputs during scan shifting by scanning in the test patterns where neighboring bits are highly correlated. The proposed BIST comprised of two TPGs. Low transition random TPG (LT-RTPG) and 3-weight weighted random BIST (3-weight WRBIST). Test patterns generated by the LT-RTPG detect the easy-to-detect faults and remain the undetected faults can be detected by the WRBIST. The 3-weight WRBIST is used to reduce the test sequence lengths by improving detection probabilities of random pattern resistant faults (RPRF). So, in this part of project maximum numbers of faults are covered with automatic test pattern generation.

Keywords: ATPG - Automatic Test Pattern Generation, BIST- Built In Self-Test, RPRF- Random Pattern Resistant Fault, LT RTPG – Low transition Random Test Pattern Generation, LFSR – Linear Feedback Shift Register, WR BIST -Weighted Random

Introduction

Test power is the major issue for current generation VLSI testing. It has become the biggest concern for today's SoC. Traditional DFT methodologies increase useless power dissipation during testing and are not suitable for testing low power VLSI circuits leading to lower reliability and manufacturing yield. Power and energy consumption of digital systems may increase significantly during testing. This extra power consumption due to test application may give rise to severe hazards to the circuit forever, it may be responsible for cost, performance verification as well as technology related problems and can dramatically shorten the battery life when on-line testing is considered. A built-in self-test (BIST) or built-in test (BIT) is a mechanism that permits a machine to test itself. Engineers design BISTs to requirements of high reliability, Lower repair cycle times in integrated circuits, BIST is used to make faster, less-expensive manufacturing tests. The IC has a function that verifies all or a portion of the internal functionality of the IC. In some cases, this is valuable to customers, as well. The main purpose of BIST is to reduce the complexity, and thereby decrease the cost and reduce reliance upon external (pattern-programmed) test equipment.

BIST reduces cost in two ways:

- reduces test-cycle duration
- It reduces the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven/examined under tester control.

Test Pattern Generation of BIST

Test pattern generation is the process of defining an effective test set which will drive the circuit under test so that the faults in the circuit. The algorithms used in test pattern generation are usually directed to non-functional testing, which concentrate on propagating any available faults on the circuit nodes to primary outputs. This type of testing is termed fault oriented testing. Test pattern generation is strongly related to fault modelling. Test pattern generation approaches for BIST schemes can be divided into four categories:

1. Exhaustive testing
2. Pseudorandom testing
    a. Weighted test generator
    b. Adaptive test generator
3. Pseudo exhaustive testing
4. Deterministic testing

Existing System

Accumulator cell Design

An Accumulator Cell is designed with Full adder and D flip flop with set and reset inputs. According to these schemes a typical weight assignment procedure would involve separating the test set into two subsets as follows S1 = {T1,T4} and S2 = {T2,T3}, The weight assignments for these subset is W(S1)={-,-,1,-,1} and W(S2)={-

,-,0,1,0}, where a "-" denotes a weight assignment of 0.5, a "1" indicates that the input is constantly driven by the logic "1" value, and "0" indicates that the input is driven by the logic "0" value. The implementation of the weighted-pattern generation scheme is based on the full adder truth table.

Operation of Accumulator cell

A fig 1 shows an accumulator cell with full adder and D-flip flop. In this the upper D-flip flop uses set as reset and reset as set inputs. The output of upper D-flip flop is given as input of full adder. The output of full adder is connected with another D-flip flop with actual set and reset inputs. Full adder uses 3 inputs, 2 inputs from output of both D-flip flops, and another input is C_{in}. The sum output of full adder is given as input of D-flip flop.

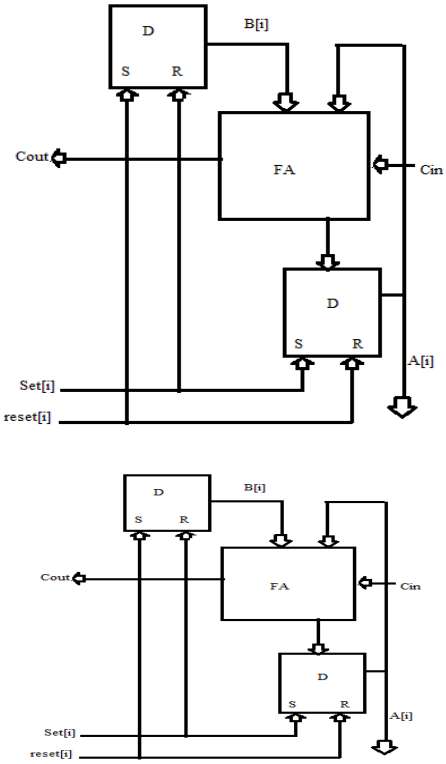

Figure 1: Accumulator Cell

Configuration of Accumulator cell

There are three configurations for Accumulator cell is proposed. It is shown in Fig 2. The configuration (a) in Fig2 that drives the CUT inputs when A[i] ="1" is required. Set[i] = "1" and reset[i] ="0" and hence A[i]="1" and B[i]="0".Then the output is equal to "1", and C_{in} is transferred to C_{out}.

The configuration (b) that drives the CUT inputs when A[i]=”0” is required. Set[i] = “0” and reset[i]=”1” and hence A[i]=”0” and B[i]=”1”. Then the output is equal to “0”, and C_{in} is transferred to C_{out}.

The configuration (c) that drives the CUT inputs when A[i]=”-“ is required. Set[i]=”0” and reset[i]=”0”.This condition is also referred as 0.5 weight output or don’t care state. The D input of the flip flop of the register B is driven by either 1 or 0, depending on the value that will be added to the accumulator inputs in order to generate random patterns to the inputs of the CUT.

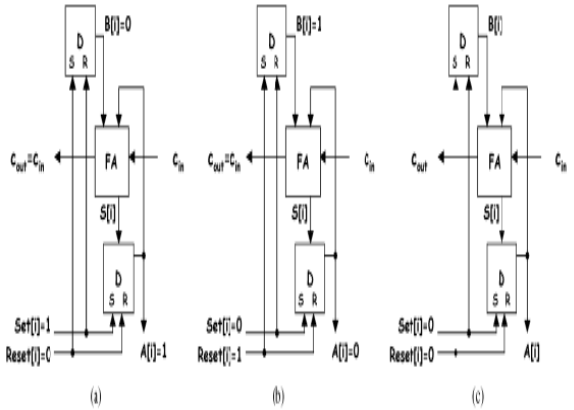

Figure 2: Configurations of accumulator cell

Testing a Circuit By Using Test Vectors

A fig 3 shows a C17 benchmark circuit. In this 5 inputs are used.

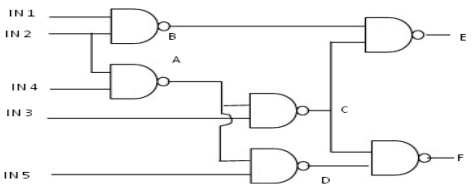

Figure 3: C17 Benchmark circuit

The weights are applied through set and reset values, the test vectors are generated automatically by pseudorandom method. The fault coverage is calculated. Fig 4 show a C17 benchmark circuit with inputs from accumulator cell output.

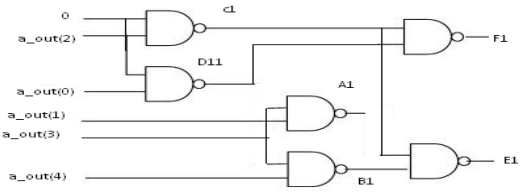

Figure 4: C17 Benchmark circuit with inputs from accumulator cell output

A benchmark circuit is taken and it is tested by using test vectors which is generated by using pseudorandom pattern generation method. A C17 benchmark circuit is taken and tested by using test vectors. The fault coverage is more by applying these test vectors. These outputs are used as inputs for another benchmark circuit. Stuck-at-fault is applied and test vectors are generated automatically.

The output of accumulator cell are a_out(0),a_out(1),a_out(2),a_out(3),a_out(4). These outputs are used as inputs for another benchmark circuit. Stuck-at-fault is applied and test vectors are generated automatically. The faults are covered by test vectors. The fault coverage is more by applying these test vectors.

If the fault output is "1" means, it indicates that **"fault is detected"**. If the fault output is "0" means, it indicates that**, "fault is not detected"**. Mostly 90% of faults are detected so, the fault coverage is more.

Proposed Design

Proposed Bist

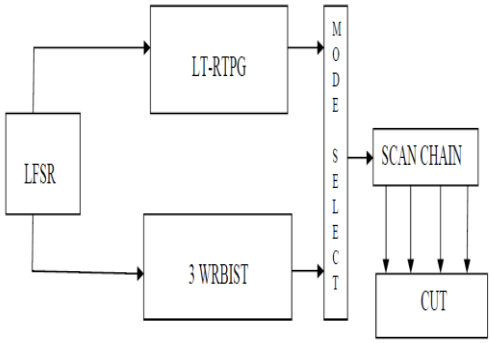

Figure 5: Architecture diagram of BIST

Fig 5 shows the proposed BIST provides two different BIST sessions; the LT-RTPG and 3-weight WRBIST session. Patterns generated from LFSR are given to LT-RTPG and 3 weight WR-BIST. LT-RTPG will detect the easy-to-detect faults and remain undetected faults are detected by 3Weight WR-BIST. The LT-RTPG is comprised of an LFSR, y T flip-flop and AND gate pairs, each of which is connected to a scan chain through a multiplexer. The three inputs of each AND gate are connected to different stages of the LFSR to reduce correlation among test patterns that are scanned into each scan chain. The 3-weight WBIST TPG is comprised of an LFSR, session counter and accumulator.

The multiplexer, which drives the input of scan chain, selects a test pattern source between the LT-RTPG and the 3-weight WRBIST. In this, test patterns generated by the LT-RTPG are selected and scanned into the scan chain to detect easy-to-detect faults. In next technique, test patterns that are generated by the 3-weight WRBIST are selected to detect the faults that remain undetected after the first session.

LT-RTPG BIST

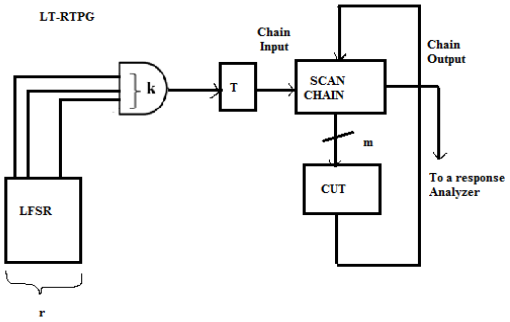

Figure 6: Architecture of LT-RTPG

The Low transition random test pattern generation (LT-RTPG) reduces switching activity during BIST by reducing transitions at scan inputs during scan shift operations The LT-RTPG is comprised of an r-stage LFSR, a K-input AND gate, and a toggle flip-flop (T flip-flop). Hence, it can be implemented with very little hardware.

Since a T flip-flop holds previous values until the input of the T flip-flop is assigned a 1, the same value v, where v€{0.1}, is repeatedly scanned in to the scan chain until the value at the output of the AND gate becomes 1. Hence, adjacent scan flip-flops are assigned identical values in most test patterns and scan inputs have fewer transitions during scan shift operations. Since most switching activity during scan BIST occurs during scan shift operations (a capture cycle occurs at every (m+1) cycles), the LT-RTPG can reduce heat dissipation during overall scan testing.

WR-BIST

In the 3-weight WRBIST scheme, fault coverage for a random pattern resistant circuit is enhanced by improving detection probabilities of RPRFs; the detection probability of an RPRF is improved by fixing some inputs of the CUT to the values specified in a deterministic test cube for the RPRF. The architecture of WR-BIST is shown in Fig 7.

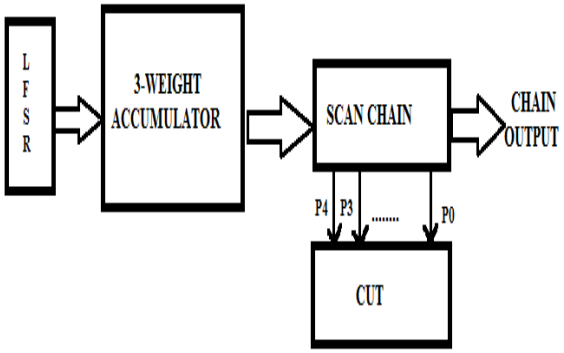

Figure 7: Architecture of WR-BIST

Simulation Results

Simulation Result for Accumulator cell Configurations

The waveform of Accumulator cell's configurations is shown in the fig 8. The configuration (a) that drives the CUT inputs when A[i]="1" is required. Set[i] = "1" and reset[i] ="0" and hence A[i]="1" and B[i]="0". Then the output is equal to "1", and C_{in} is transferred to C_{out}.

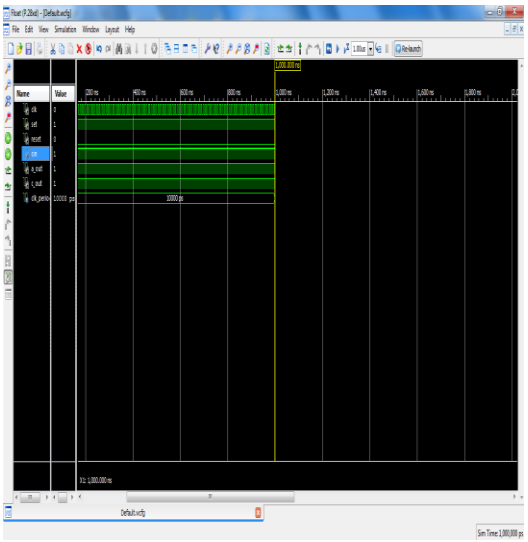

Figure 8: Waveform for the configuration of set[i]="1" and reset[i]="0"

The waveform for Accumulator cell with set[i]="0" and reset[i]="1" is shown in the Fig. 9.

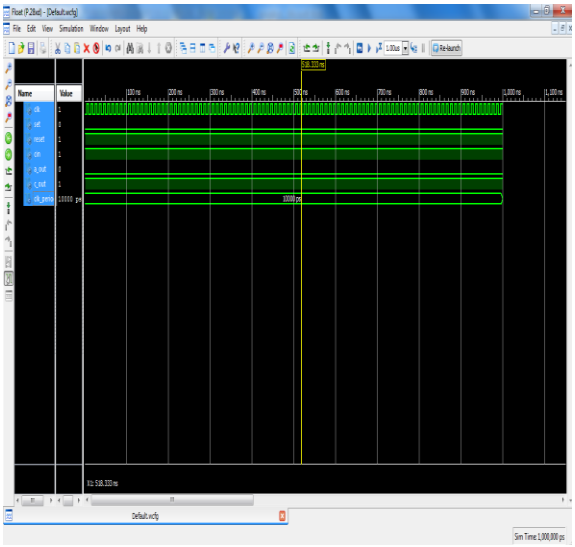

Figure 9: waveform of the configuration of set[i]="0" and reset[i]="1"

The waveform for Accumulator cell with se[i]t="0"and reset="0" is given in fig 10.

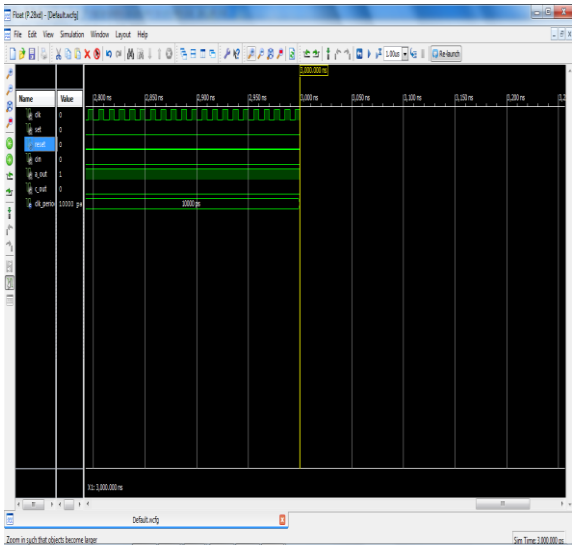

Figure 10: Waveform of the configuration of set[i]="0" and reset[i]="0"

Simulation Result for Test Vector Generation for Fault Coverage

Fig 11 shows the applied test vectors for set and reset are "10000" and "00001" respectively. If fault is present means fault output parameter is set as"1". If no fault in circuit means, fault will be set as "0". For this applied test vectors the test patterns are generated automatically.

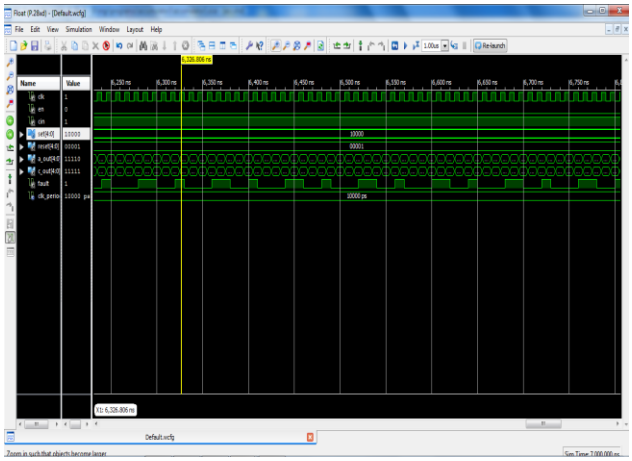

Figure 11: Output Waveform For Benchmark Circuit Using Accumulator Cell

Simulation Result For LT-RTPG

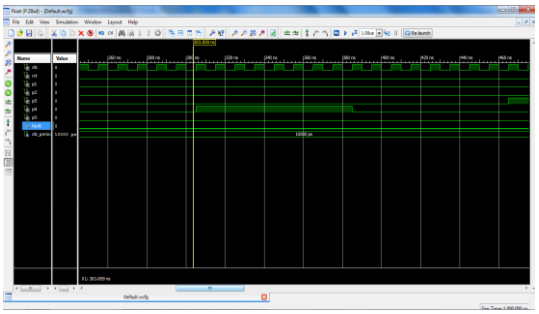

Figure 12: Output Waveform of LT-RTPG for Fault not detected

Fig 12 shows the output waveform for LT-RTPG. It is the waveform for fault not detected because the fault is shown as "0".

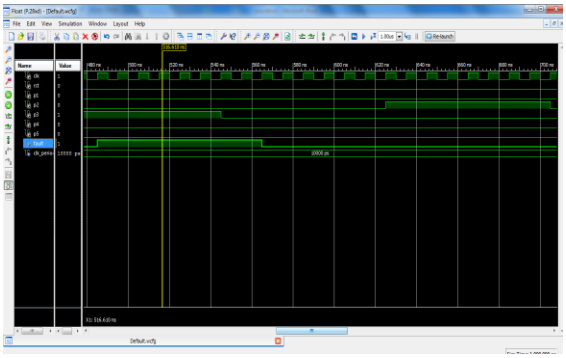

Figure 13: Output Waveform of LT-RTPG for Fault detected

Fig 13 shows the output waveform for LT-RTPG. It is the waveform for fault detected because the fault is shown as "1".

Simulation Result For WR-BIST

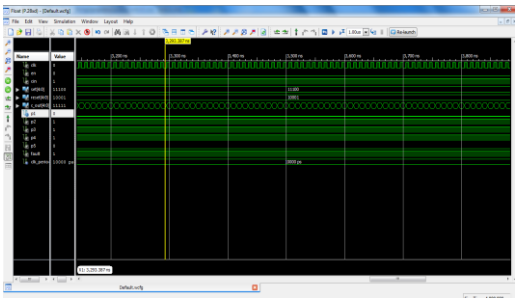

Figure 14: Waveform of WR-BIST with high fault coverage

In Fig 14 clk , C_{in}, set and reset are the inputs. $C_{\_out}$, fault, p_1,p_2,p_3,p_4,p_5 are the outputs. Set and reset values for generated patterns are “11100” and “10001”… fault coverage for this vector is 100%.

Simulation Result For Proposed BIST

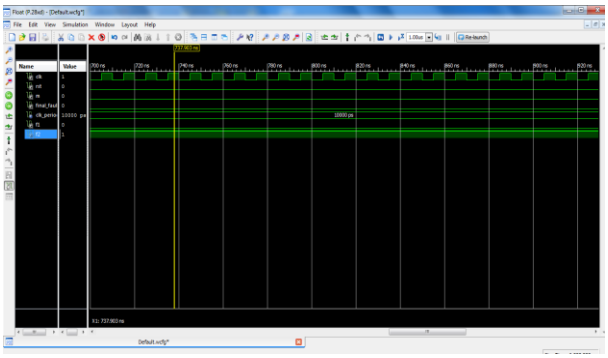

Figure 15: Waveform of Proposed BIST for fault not detected

Fig 15 shows the waveform of Proposed BIST for fault not detected. In this clk, rst , and m are the inputs of the Proposed BIST. f1,f2 are the outputs of the Proposed BIST.

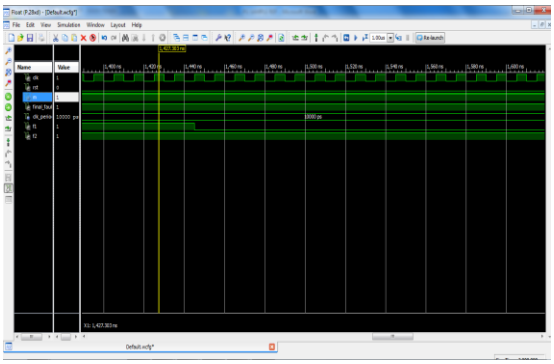

Figure 16: Waveform of Proposed BIST for fault detected

Fig 16 shows the waveform of Proposed BIST for fault detected. In this clk, rst , and m are the inputs of the Proposed BIST. f1,f2 are the outputs of the Proposed BIST.

Power Table

The table below shows the comparison of the power for various methods. The power consumed by the accumulator is 0.103w , by LT-RTPG is 0.064w, by WR-BIST is

0.062 w and the results shows that the power consumed by the proposed method is low and is only 0.053 w. The same is shown is Fig.17 as comparison graph.

Table 1: Power Summary

Series	Accumulator	LT-RTPG	WR-BIST	Proposed BIST
Power [w]	0.103	0.064	0.062	0.053

A. Power Comparison Chart

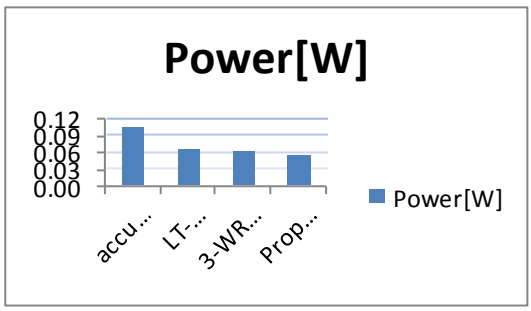

Figure 17: Power Comparison Chart

Conclusion

In this project the proposed TPG uses 49% less power than the existing (accumulator) scheme. A low hardware overhead TPG for scan based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with an arguable length of test sequence is presented through this project. An Accumulator-based 3-weight technique can reduce the hardware implementation cost and fault coverage is more. The power is get reduced and increased fault coverage. The fault coverage is more and it is proved by testing a c17 benchmark circuit. The time for testing a circuit is less and very simple method, because of its automatic test pattern generation. The test patterns are generated automatically for applied test vectors The proposed TPG LT-RTPG and 3-weight WRBIST reduces switching activities in the circuits, so that the number of transitions will be decrease and less power will be consume. Further we can try to reduce the power consumed by increasing weights.

References

[1]. H.J.Wunderlich,"multiple distributions for biased random test patterns"in proc.IEEE int.test.conf.,1988

[2]. Pomeranz. I, and S. M. Reddy.., "3 weight pseudo-random test generation based on a deterministic test set for combinational and sequential

circuits"., IEEE Trans. Computer-Aided Design Integrated Circuits System., vol.12, no. 7, pp. 1050–1058, 1993.

[3]. Nur A. Touba, Member, IEEE, and Edward J. McCluskey ., „Bit- Fixing in Pseudorandom Sequences for Scan BIST presented at IEEE transactions on computer-aided design of integrated circuits and systems,vol. 20, no. 4, (2001).

[4]. Wang. S.., "Low hardware overhead scan based 3-weight weighted random BIS", IEEE Int. Test Conf.. pp. 868–877…,2001

[5]. Shalini Ghosh, Eric Mac Donald, Sugato Basu, and Nur A. Touba.„Low-Power Weighted Pseudo-Random BIST Using Special Scan Cell system‟ .

[6]. Voyiatzis . I,, D. Gizopoulos, and A. Paschalis..,"Accumulatorbased weighted pattern generation".., presented at the IEEE Int. Line Test Symposium…, 2005

[7]. Manich. S, L. Garcia-Deiros, and J. Figurers., "Minimizing test time in arithmetic test-pattern generators with constrained memory resources", IEEE Trans. Computer-Aided Design. Integrated Circuits System. 2007

[8]. Mehrdad Nourani, Mohammad Tehranipoor, and Nisar Ahmed ,"Low-Transition Test Pattern Generation for BIST-Based Applications".., IEEE Transaction on computers, vol no: 57, no. 3.2008

[9]. Seongmoon Wang, Sandeep K. Gupta, „LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation‟ Presented at the ITC international test conference, IEEE Xplore (2009).

[10]. Savir. J., "Distributed generation of weighted random patterns",IEEE Trans. Computer-Aided Design of Integrated Circuits System.vol.48, no. 12, pp. 1364–1368.., 1999.

[11]. Secongman Wang.., "faults diagnosis for using TPG low power dissipation and high fault coverage" .IEEE Trans. Vol.15 no.7, 2010.

[12]. Antonis Paschalis,Ioannis Voyiatzis,&Dimitris Gizo Poulos "accumulator based 3 weight pattern generation", IEEE transactions on VLSI systems.vol.20.no.2.feb.2012