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Analysis of FPGA Based Non-Deterministic PWM In Induction Motor Drives

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Abstract

The prime advantages of non-deterministic pulse width modulation (PWM) strategies are that the harmonic spectrum of the output voltage is spread over the range without any specific dominant harmonic. This absence of distinct dominant harmonics results mainly in reduction of acoustic noise and torque ripples in drives. In this paper, a field-programmable gate array (FPGA) based implementation and corroboration of Pseudo Random Binary Sequence (PRBS) bit based random carrier PWM (RPWM) for the three-phase voltage source inverter (VSI) fed induction motor drive, are presented. First a detailed simulation study on performance characteristics such as harmonic spectrum, total harmonic distortion (THD), harmonic spread factor (HSF) and power density spectrum, are presented for both conventional sinusoidal PWM (SPWM) and RPWM. Secondly, a new circuit realization of the above PWM strategies are developed using state of-the-art FPGA technology. The designed controller provides a simple and effective solution for high-performance AC drives.

Keywords: Field programmable gate array (FPGA), harmonic spread factor (HSF), power density spectrum, random pulse width modulation (RPWM), voltage source inverter (VSI).

Introduction

Pulse-width modulated (PWM) voltage source inverters(VSIs) represent the dominant technology in industry today [1]-[5].A large number of PWM switching pattern generators have been developed over the last four decades to meet the respective requirements for distortion free output waveforms of sinusoidal nature. Overall system performance and quality output waveforms can be improved based on the selection criteria imposed on the scheme. An important advantage of random or

nondeterministic modulation techniques is non-repetitive spectral characteristics of the output waveforms without energy concentration at distinct harmonics [6]-[8]. Also this period was outstanding due to the revolution of technological possibilities in the field of digital electronic control by micro controller, digital signal processor (DSP), complex programmable logic devices (CPLD), field programmable gate array (FPGA) and application specific integrated circuit (ASIC)technologies. Among all these possibilities, FPGA is a good candidate having the advantage of the flexibility of a programming solution and the efficiency of a specific architecture with a high integration density, and high speed. The field programmable gate array (FPGA) technology provides programmable system-on-chip (PSoC) environments for designing modern digital ASIC controllers for specific applications.

In 1987, A.M. Trzynadlowski et al have developed a Random PWM (RPWM) technique to reduce acoustic noise and mechanical vibration [8]. The random switching is based on a uniform probability density function. The superiority of the RPWM techniques over the deterministic PWM methods is studied. Thomas G. habetler and Deepakraj M. Divan have introduced an acoustic noise reduction option using a randomly modulated carrier [9].The randomly modulated carrier is compared with reference waveform to produce the RPWM pulses. In this technique random signal is used as the modulating function, the effects of its magnitude and varying speed (or bandwidth) on the inverter output harmonic distributed characteristics are analyzed.

The design and development of dynamic partially reconfigurable PWM (DPRPWM) controller for three-phase voltage-source inverters (VSI) in a single Xilinx Spartan 3 XCS400PQ208 field programmable gate array (FPGA) has been developed [10]. A scheme of FPGA-based three-level space vector modulation (SVM) inverter has been proposed [11]. The SVM algorithm for three-level inverter is described, including the approach to calculate the dwell times of each switching state using volt-second characteristic, the algorithm of determining the space vector location and the principle for selecting switching sequences to generate symmetrical PWM output waves. The standard design flow of FPGA implementation and the functional block diagram of FPGA realization are given. Five-phase sinusoidal PWM signal generator at fast sampling frequency using one-chip programmable gate array (FPGA) has been realized. It is shown that the generation of sinusoidal PWM using FPGA can perform the switching frequency of the inverter at 40 kHz switching frequency that may raise potential for excellent drive performances [12]. A FPGA based speed control IC for three-phase induction motor drives have been presented [13]. The sinusoidal PWM is realized on a single FPGA chip from Xilinx Inc. to provide controlling switching pulses for inverter block.

Even though the industrial society has understood the PWM persuaded torque ripples and acoustic noises, the lack of methodical evaluation of existing PWM techniques sojourn the further verdicts. Secondly, the analog platform is inappropriate to non-deterministic PWM methods because of their nature. A flexible, reprogrammable digital platform could solve this issue. A methodical study on performance characteristics such as harmonic spectrum, total harmonic distortion (THD), harmonic spread factor (HSF) and power density spectrum, are presented for

both conventional sinusoidal PWM (SPWM) and RPWM. A FPGA based implementation and corroboration of Pseudo Random Binary Sequence (PRBS) bit based random carrier PWM (RPWM) for the three-phase voltage source inverter (VSI) fed induction motor drive, are presented.

Random Carrier PWM

Figure 1. shows the randomized triangular carrier generation. As shown in Figure 1. the triangular carrier with fixed frequency 'fc+'and the triangular carriers with fixed frequency but opposite phase 'fc-' are given as input to the 2×1 multiplexer. Both the frequencies (fc+ and fc-) are same. The randomized triangular carrier 'R' can be obtained randomly selecting the fc + and fc- by the PRBS output bits 0 or 1 of the random bit generator.

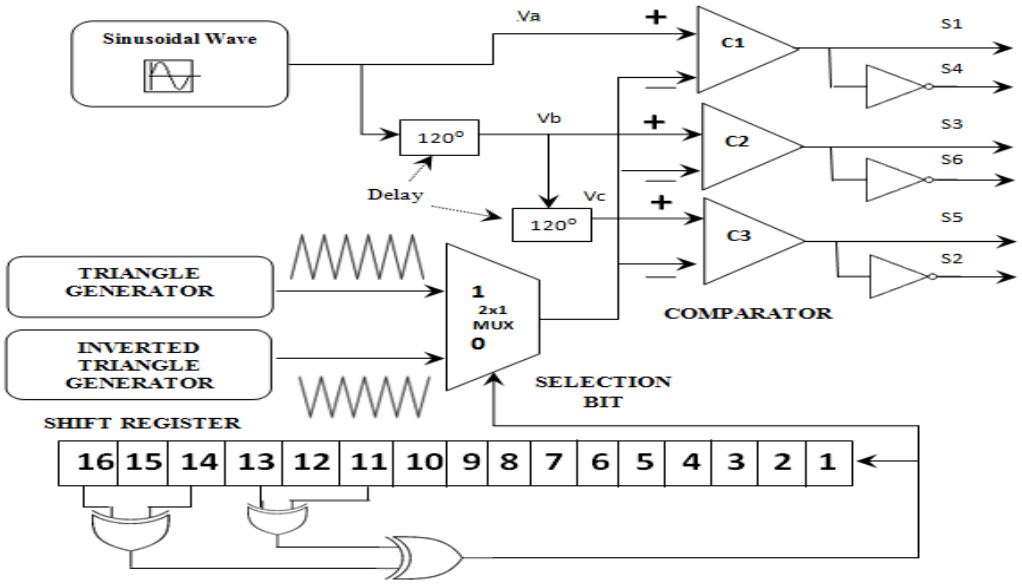

Figure 1: Random Carrier PWM

In order to obtain the random bit number for selecting the winning triangle, a triumph sequential digital circuit with large number of distinct states (bigger repetition cycle) is required. This is because the randomness does not rely only on two distinct carriers but also on the sequential pattern used for selection. LFSR is the best solution to offer the above requirement (good randomness) [14-17].

The principle of LFSR is based on the logical operation of several bits of a digital number and is commonly known as pseudo PWM code generator in communication systems [17]. In this paper, 16 bits LFSR with a feedback of four tapings is used and the feedback causes the register to loop through repetitive sequences of pseudo-random value. The choice of taps determines how many values there are in a given sequence before the sequence repeats. The optimum tapping bit numbers are used for logical XOR operation (Bits 4, 5 and 6, 8). Repetition is depends upon the length of

LFSR and the clock frequency used. The winning triangle carrier cycle is compared with sinusoidal reference to get the gating pulses.

Simulation

The simulation study is performed in MATLAB/Simulink software. A three-phase VSI inverter with three-phase Squirrel Cage Induction Motor (0.75 kW and 2.5 A load) is considered. The input dc voltage (Vdc) is 415V and the output frequency is taken as 50 Hz. The switching frequency of SPWM is 3kHz while the RPWM employs ±3kHz.

The line voltage and current waveforms resulted from SPWM are illustrated in Figure 2. and Figure 3. respectively for modulation index, Ma=0.8. Table 1 describes various performance indices of SPWM. Table 2 presents the results of RCPWM. Figure 4. illustrates the output spectrum output voltage for the RCPWM and the power density spectrum is depicted in Figure 5. The bar chart drawn in Figure 6. exhibits the modulation depth dependency of HSF.

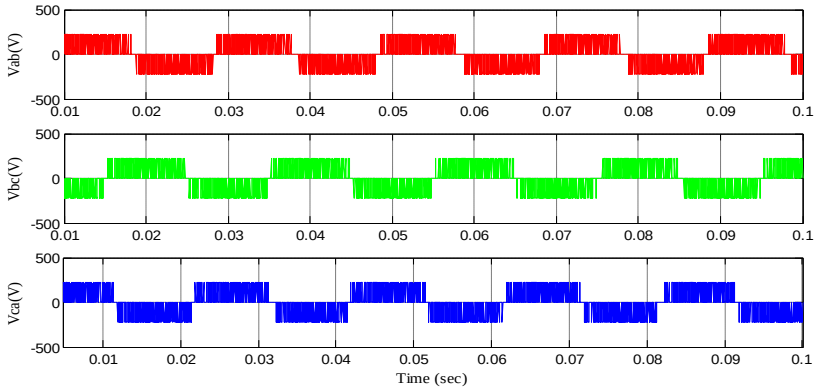

Figure 2: Simulated line-line voltage waveform for Ma=0.8

Table 1: Performance of SPWM

Simulation Results			
Modulation Index (Ma)	Output Voltage (V_0)	THD (%)	HSF
0.2	75.31	240.71	4.9308
0.4	136.80	168.07	4.6710
0.6	211.10	122.01	4.6054
0.8	293.80	89.15	4.0572
1.0	367.3	66.13	3.7386
1.2	395.2	58.21	3.5091

Table 2: Performance of RCPWM

Simulation Results			
Modulation Index (Ma)	Output Voltage (V_0)	THD (%)	HSF
0.2	49.059	257.97	8.312
0.4	75.86	164.31	6.142
0.6	114.00	121.10	5.880
0.8	153.30	90.60	5.566
0.9	170.30	80.73	5.162
1.0	190.90	68.42	4.952

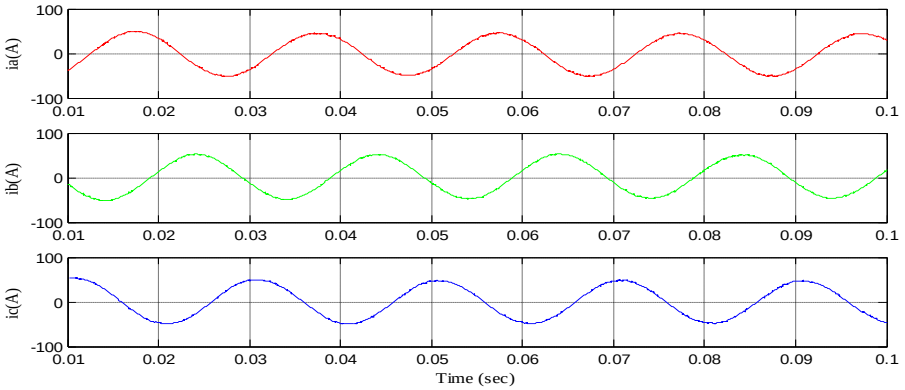

Figure 3: Simulated line current waveform for Ma=0.8

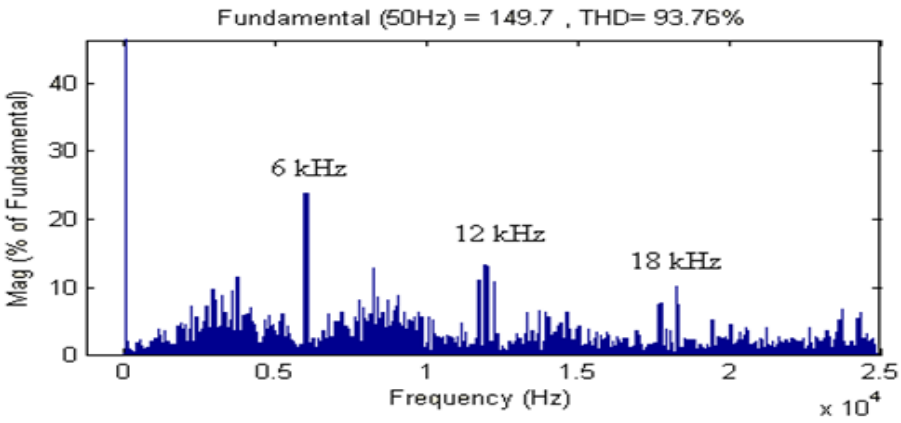

Figure 4: Spectrum of output voltage

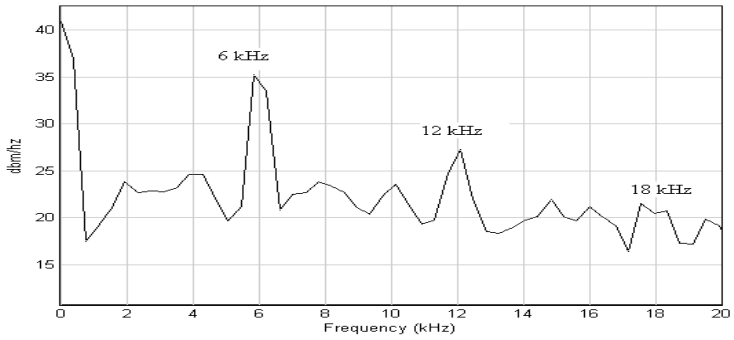

Figure 5: Power spectral density for Ma= 0.8

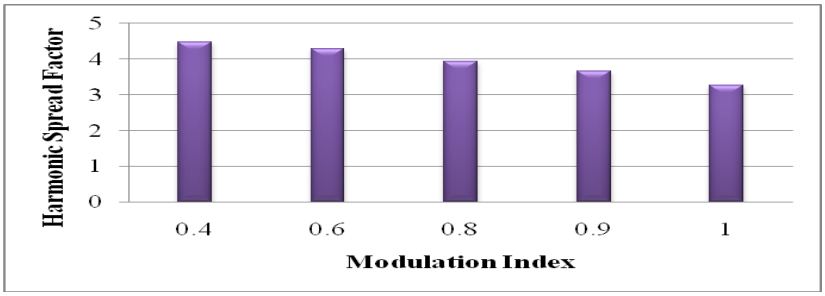

Figure 6: RPWM Harmonic Spread Factor and Modulation Index

Hardware Implementation

The proposed Random Carrier PWM architecture has been designed using the VHDL language. The functional simulation of the architecture has been carried out using the tool Modelsim 6.3. The Register Transfer Level (RTL) level verification and implementation are done using the synthesize tool Xilinx ISE 13.2. Then the designed architecture has been configured to the SPARTAN-6 FPGA (XC6SLX45) device.

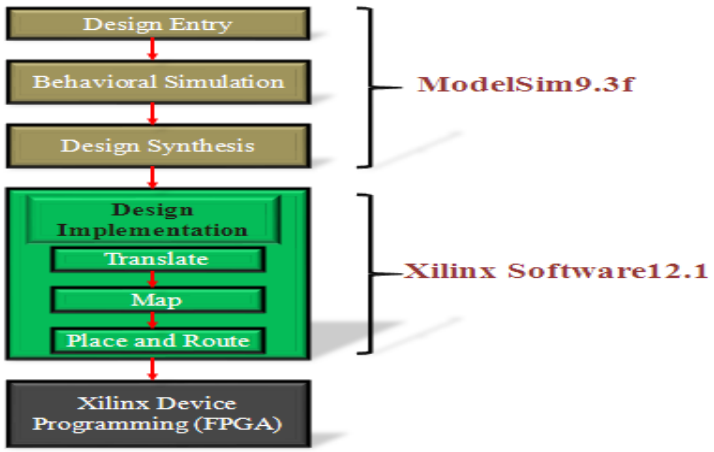

Figure 7: FPGA Design flow for SPWM and RPWM schemes

The functionality of each block in the architecture is simulated thoroughly using the Modelsim software. The detailed flow is represented in the Fig.7 as a flow chart. The algorithm involved in the RCPWM implementation is diagrammed in Fig.8. The triangular data is initialized first and inverse triangular data is derived from it. From the fed sine reference data of 'A' phase, data from 'B' and 'C' phases are derived. Now the called LSFR sequence select between the carriers and its comparison with the reference results in required pulses for the VSI. The simulated VHDL Design of the RCPWM architecture is synthesized using Xilinx ISE software. The RTL verification and logic implementation of the design are carried out here. The corresponding synthesis results are shown in Figure.9 and Figure10.

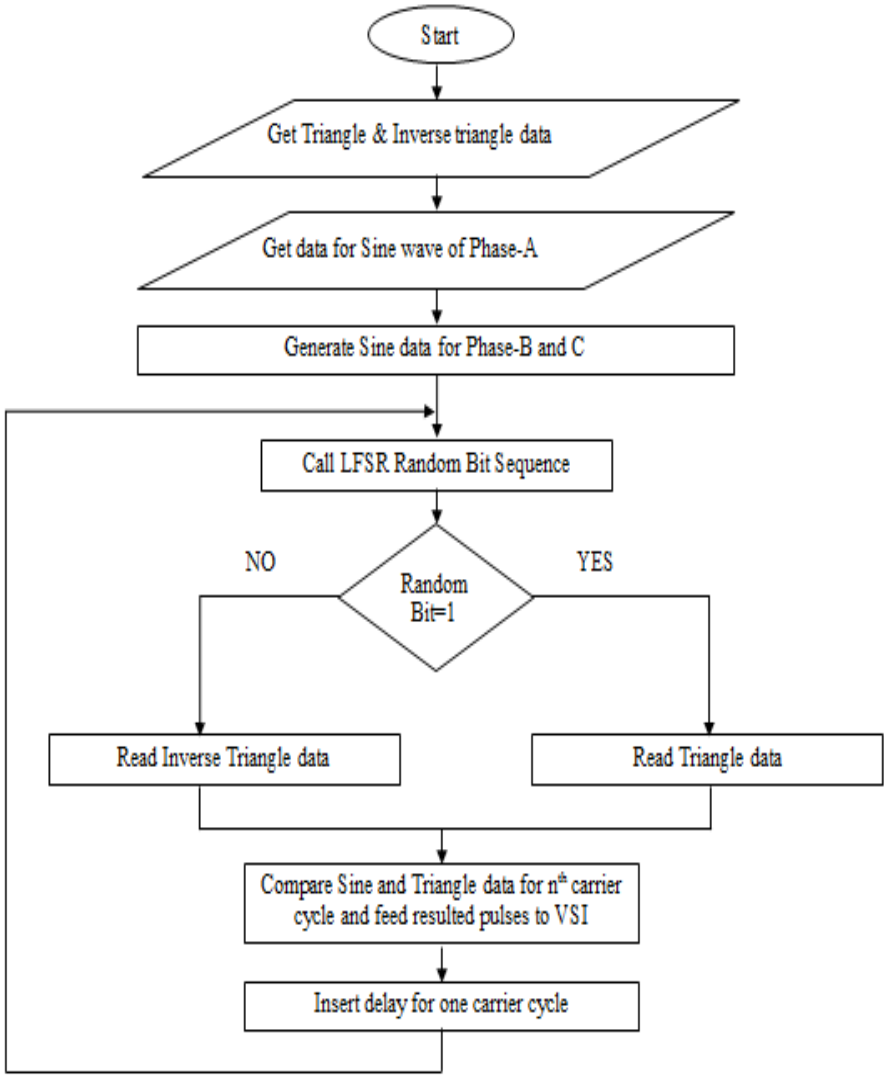

Figure 8: Implementation of RCPWM

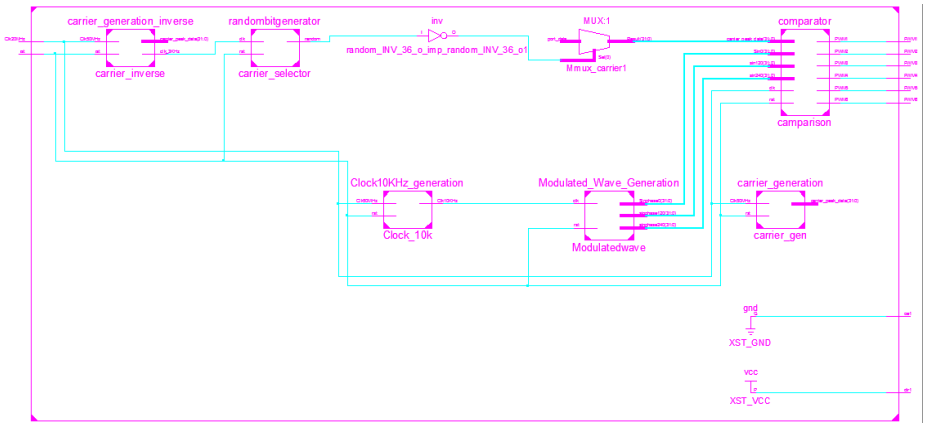

Figure 9: RTL Diagram for RPWM 8-bit PRBS

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	325	30064	1%
Number of Slice LUTs	793	15032	5%
Number of fully used LUT-FF pairs	228	890	25%
Number of bonded IOBs	10	186	5%
Number of BUFG / BUFG CTRLs	5	16	31%
Number of DSP48A1s	3	38	7%

Figure 10: Device utilization summary

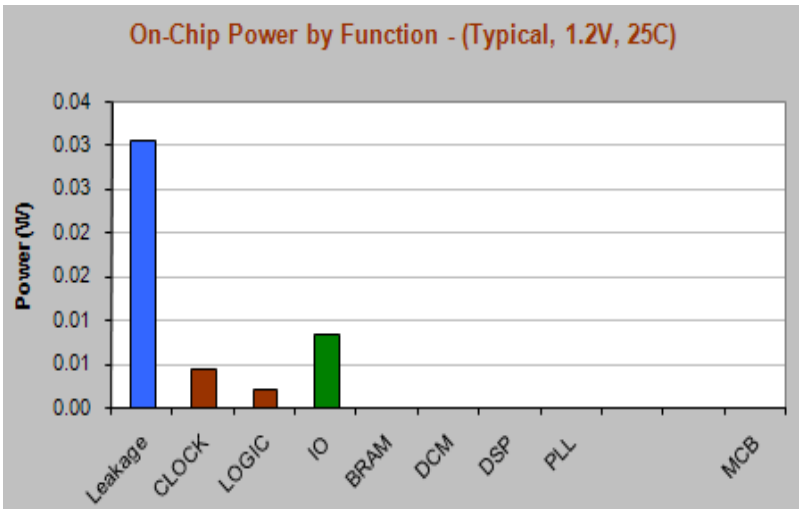

Figure 11: Power Estimation Report

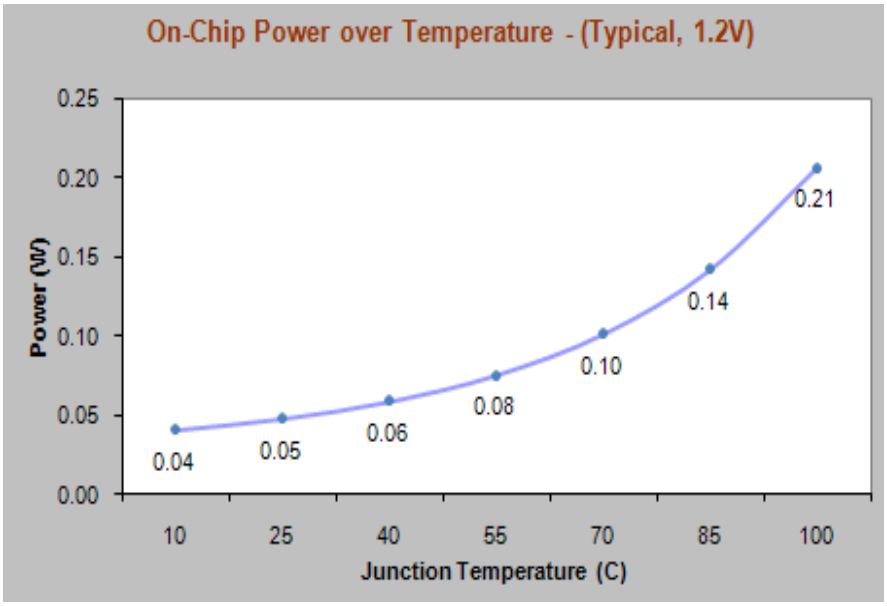

Figure 12: Temperature dependency of power

The power estimation for the designed architecture has been done using the Xilinx power estimator tool (Xpower Estimator (XPE)-14.1).The power estimation report for the RCPWM design is generated and shown in Figure 11. and the temperature dependency of the On-Chip power also analyzed as illustrated in Figure 12.

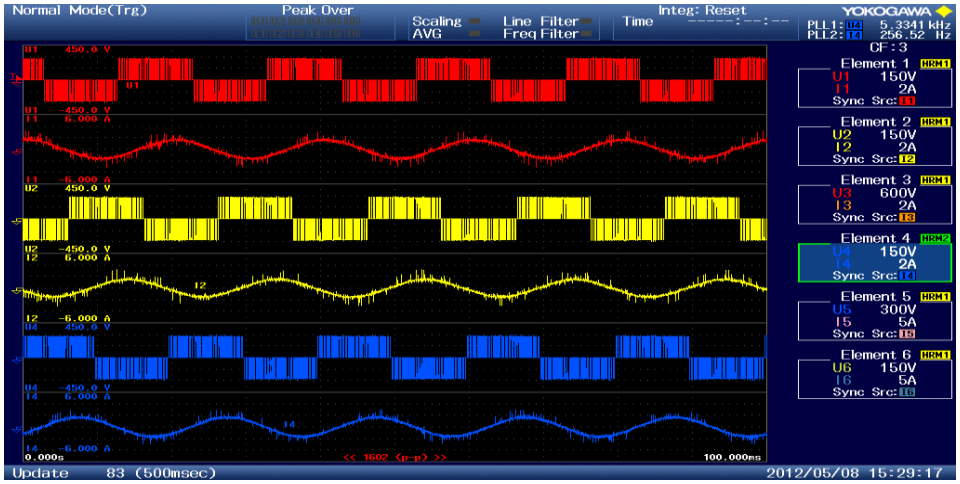

Figure 13: Output line voltage & current waveform at Ma=0.8

The synthesized design of RCPWM architecture is downloaded to the FPGA Spartan 6 device (XC6SLX45) with the help of device programming software "DIGILENT ADEPT". The configured FPGA device with proposed architecture has been tested with a prototype of three phase VSI with an input dc voltage (Vdc) of 400V and a load of 0.75 kW three-phase Squirrel Cage Induction Motor. The output

line to line voltage and current is shown in Figure 13. The triumph of the devolved code is proved by the results presented in Figure 14. and Figure 15. which are simulation and hardware harmonic spectra.

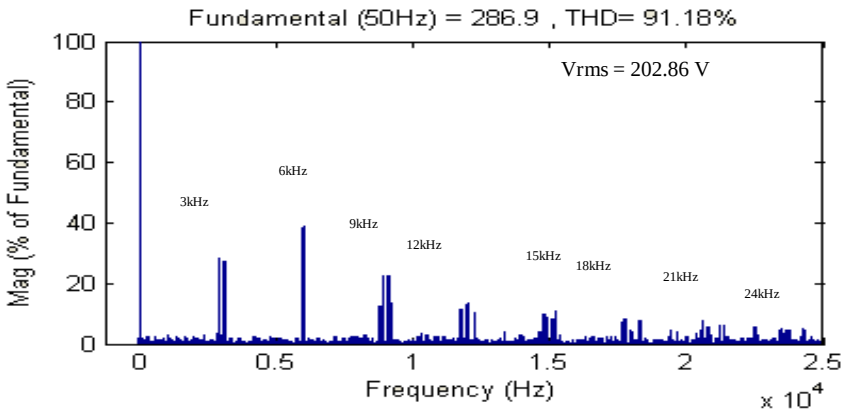

Figure 14: MATLAB Simulation Results

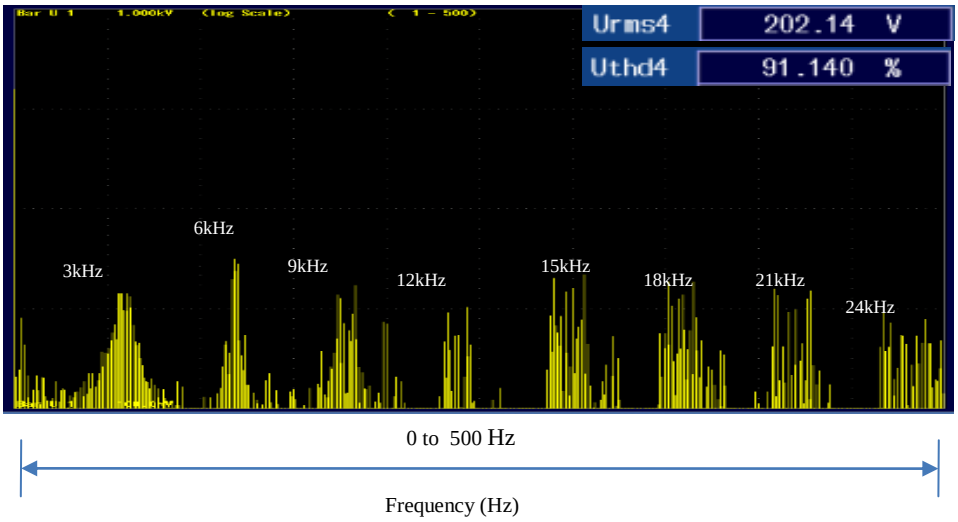

Figure 15: Hardware Results

Table 3: Comparison Of Simulation And Hardware Results-RCPWM

	Simulation Results		**Hardware Results**	
Modulation Index (M_a)	**Output Voltage(V)**	**THD (%)**	**Output Voltage(V)**	**THD (%)**
0.2	49.18	255.73	47.56	246.94
0.4	103.52	161.59	103.94	101.93
0.6	151.39	122.24	151.68	120.93

0.8	203.97	91.32	202.68	91.53
0.9	227.26	80.61	228.13	79.389
1.0	253.63	69.13	255.22	67.07

Conclusion

Induction motors are mainly employed in industrial processes and become dominant adjustable speed drive (ASD). The performance of the induction drive depends largely on PWM techniques employed. Random PWM is widely used to spread the harmonic power, and hence reduce the torque ripples and acoustic noises of the ASDs. The proposed architecture of RCPWM is the effective solution for the acoustic noise in the Adjustable Speed Drives. The results such as device utilization summary, power estimation and temperature dependency are very useful for the handling of digital device used for the control purpose. The harmonic power spreading ability of the RPWM is validated by the simulation study while the accurate imitation of the RPWM in FPGA platform is confirmed by the hardware results. The RCPWM offers higher output voltage, lesser THD and minimal HSF than the SPWM for the entire working range.

Appendix

Power (P)……0.75kW
Line- Line Voltage (VL)…….……..415 V
Frequency (f)…….…..….50 Hz
Stator Resistance (Rs) ……..…435Ohm
Stator Inductance (Ls) ……5839H
Rotor Resistance (Rr)……...1.395Ohm
Rotor Inductance (Lr)……...0.005839H
Inertia (J)…….……..……...0.0131Kgm2
Friction factor……...0.0029Nms
Pole Pairs…….…2

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