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Analysis of Area, Delay and Power Efficient High Speed Fast Adder

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Abstract

In electronics, adder is a digital circuit that performs addition of numbers. The carry select adder (CSLA) is one of the fastest adders. In this paper, we have removed all the unneeded logic operations present in the regular CSLA and proposed a new logic formulation for CSLA. This method, the carry select (CS) operation is scheduled before the calculation of final-sum; it is non-identical from the conventional method. Bit patterns of two expecting carry words and fixed Cin bits are used for logic optimization of CS and generation units. An efficient adder design is obtained using optimized logic units. The design of the proposed CSLA structure involves low area, delay and power consumption than the recently proposed BEC-based SQRT CSLA. The proposed SQRT-CSLA includes nearly 35% less area delay product (ADP) than the binary to excess converter based square root SQRT-CSLA, which is best among the existing SQRT-CSLA designs average for different bit-widths.

Keywords: Adder, Carry Select Adder (CSLA), Square Root Carry Select Adder (SQRT-CSLA)

1. Introduction

Analysis of low power, Area Efficient and High performance VLSI System are increasingly used in portable devices like mobiles, laptops, multi standard wireless receivers etc. In digital circuit, an adder is the main part of the arithmetic unit. A digital signal processing (DSP) involves several adders. Essentially, an efficient adder design is improve the performance of the complex digital processing system. The CSLA can compute faster because the current adder stage is does not need to wait for the previous stages carry out signal. Further it is used in many computational systems to alleviate the problem of carry propagation delay (CPD) by independently generating multiple carries and then select a carry to generate the sum. A ripple carry adder (RCA) uses a compact design, but the propagation delay is important concern in

this adder.

Carry select and Carry look-ahead methods are used to reduce the CPD of adders. The BEC-based CSLA include less logic resources than the Regular CSLA, but it has marginally higher delay in [4]. To overcome this drawback, a new logic formulation has been proposed for CSLA. It was observed that logic optimization mainly depends on availability of unneeded operations in the formulation, where adder delay largely depends on data dependence. In the existing designs, logic is optimized without giving any analysis to the data dependence. The main contribution in this method is logic formulation based on data dependence and optimized carry generator (CG) and carry select design. Based on the proposed logic formulation, an efficient logic design has been inherited for CSLA. Due to optimized logic units, the proposed CSLA includes significantly low area delay product than the existing CSLAs.

2. BEC based SQRT CSLA

A structure and the function of a 4-b BEC are shown in Fig. 2**.** Figure.1 shows how the basic function of the CSLA is obtained by using the 4-bit BEC join with the multiplexer. One input of the 8:4 multiplexer gets as it input (B3, B2, B1, and B0) and another input of the multiplexer is the BEC output. This produces the two possible partial results in parallel and the multiplexer is used to select either the BEC output or the direct inputs according to the control signal Cin [4].

The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed [4]. The Boolean expressions of the 4-bit BEC is listed as bellows,

$X0 = \sim B0$

$X1 = B0 \wedge B1$

$X2 = B2 \wedge (B0 \& B1)$

$X3 = B3 \wedge (B0 \& B1 \& B2)$

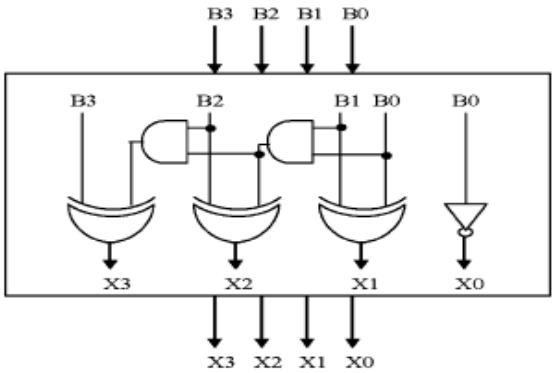


Fig.1 4-b BEC

Table 1:Function table of the 4-b BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

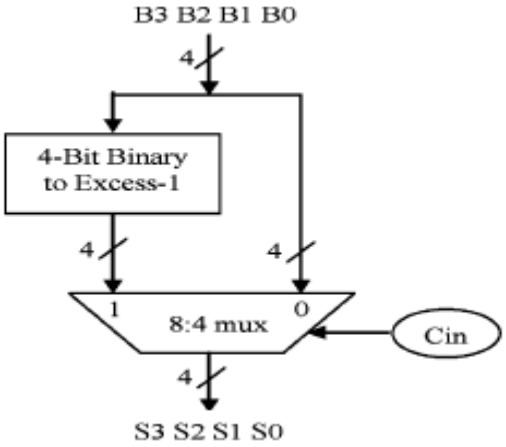


Fig.2 4-b BEC with 8:4 mux

The structure of 16-b SQRT CSLA using BEC for ripple carry adder (RCA) with Cin=1optimize the power and area is shown in Fig.3. It has five groups of different size RCA [2]. Each group consists of dual RCA and MUX. The RCA is the simplest and most compact full adders, but their performance is limited by a carry that must propagate from the least significant bit to the most-significant bit. RCA has the lowest speed compare to all the adders because of large propagation delay but it occupies the low area.

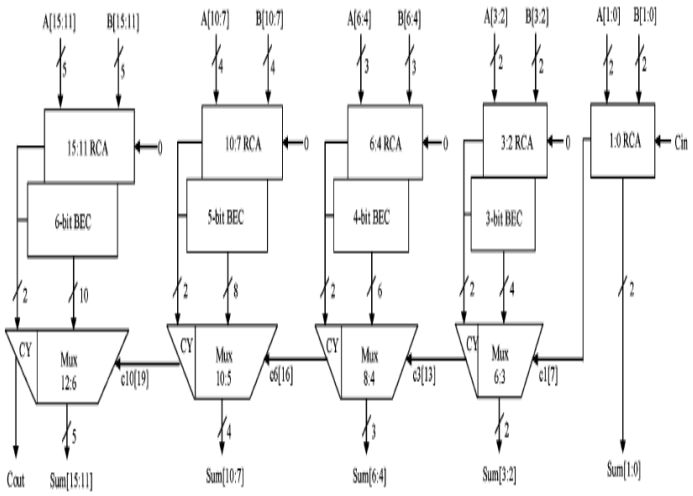


Fig.3 BEC based SQRT CSLA

BEC based SQRT CSLA is similar to that of conventional SQRT CSLA, the only difference is we replace RCA with Cin=1 with BEC. This structure consumes less delay; area and power than regular SQRT CSLA because of less number of transistors are used.

3. Proposed SQRT CSLA

The proposed method is based on the logic formulation and its structure illustrates in Fig.4. The structure consists of half sum generation (HSG) unit, FSG (full sum generation) unit, CG (carry generation) unit, and CS unit. The CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry '0' and '1'. These unit logic expressions are given in (1) to (7).

This method is removed all the redundant logic operations present in the conventional CSLA. The new logic formulations are optimized the adder structure. The main contribution of the logic formulation based on data dependence and optimized carry generator (CG) and CS design.

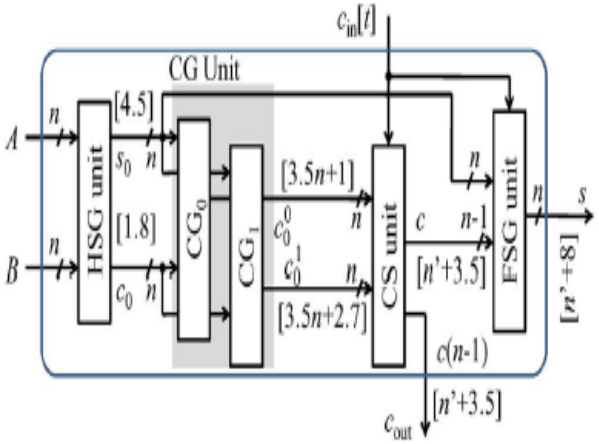


Fig.4 Proposed carry select adder design

The proposed logic formulation for the CSLA is given as,

$S_o(i) = A(i) \oplus B(i)$, $C_O(i) = A(i).B(i)$ (1)

$C_1^0(i) = C_1^0(i\text{-}1).S_o(i) + C_O(i)$ for $C_1^0(0) = 0$ (2)

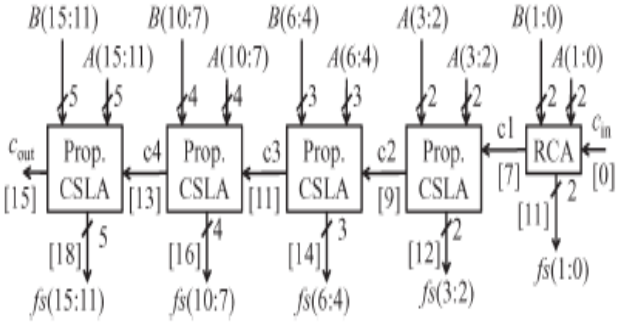
$C_1^1(i) = C_1^1(i\text{-}1).S_o(i) + C_O(i)$ for $C_1^1(0) = 1$ (3)

$C(i) = C_1^0(i)$ if (Cin = 0) (4)

$C(i) = C_1^1(i)$ if (Cin=1) (5)

Cout = C(n-1) (6)

$S(0) = S_o(0) \oplus Cin \quad S(i) = S_o(i) \oplus C(i\text{-}1)$ (7)



The HSG receives two n-bit operands (*A* and *B*) and generate half-sum word

S0and half-carry wordC0of width n bits each. Both CG0 and CG1 receive S0and C0from the HSG unit and made two n-bit full-carry words $C_1^0$and C_1^1 corresponding to input carry '0' and '1', respectively. The carry select unit selects one final carry word from the two carry words available at its input line using the control signal Cin. It selectsC_1^0 when Cin=0; otherwise, it selects C_1^1. The CS unit can be implemented using an n-bit 2-to-l MUX.However, we find from the truth table of the CS unit that carry words C_1^0 and C_1^1 follow a specific bit pattern. If $C_1^0(i)$= '1', then C_1^1(i) = 1, irrespective of S0(i)andC0(i), for 0≤i≤n–1.This advantage is used for logic optimization of the CS unit. The most significant bit (MSB)is sent to output as Cout, andleast significant bit (LSB) are XORed with (n-1) MSBs of half-sum(*s*0) in the FSG to obtain MSBs of final-sum.Fig.5 illustrates the proposed method block Diagram.

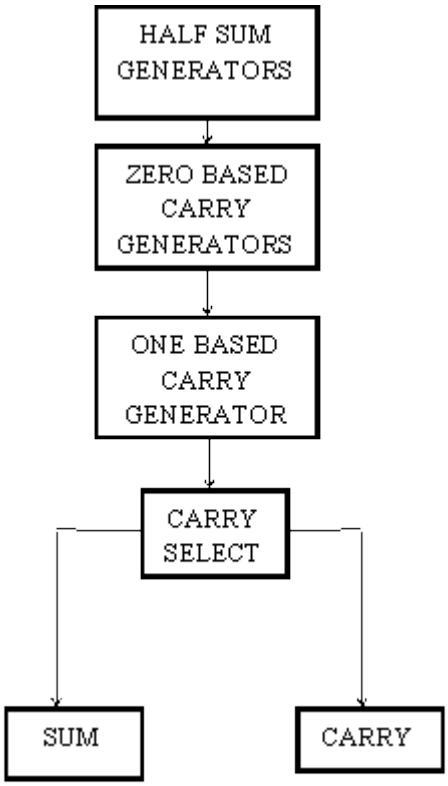


Fig.5 Block Diagram of Proposed Method

4. Experimental Results

The implemented design in this work has been simulated using Verilog Modelsim. The adders are designed and simulated using Modelsim. All the existing and proposed methods are also simulated in Modelsim and corresponding results are compared**.**

The structure of the proposed CSLA design involves significantly less area, delay and power consumption than the recently proposed BEC-based SQRTCSLA.The proposed SQRT-CSLA involves nearly 35% less area–delay–

product (ADP) than the Binary to Excess Converter (BEC) based SQRT-CSLA, which is best among the existing SQRT-CSLA method. The comparisons tables are shown below,

Table 2: Comparison Result

Adder	Area (um^2)	Delay (ns)	Power (uW)	ADP
Conventional CSLA (16 bit)	2890.52	5.61	30.5673	6.30
BEC Based SQRT CSLA (16 bit)	1929	3.048	25.7958	7.62
Proposed SQRT CSLA (16 bit)	1706.80	2.8	19.6652	5.12

Simulation results are shown below the figure 6 and figure 7.

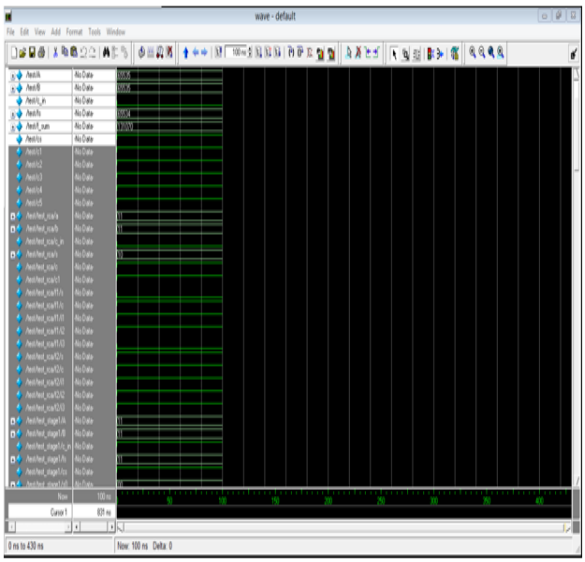


Fig.6 Simulation result of the proposed SQRT CSLA

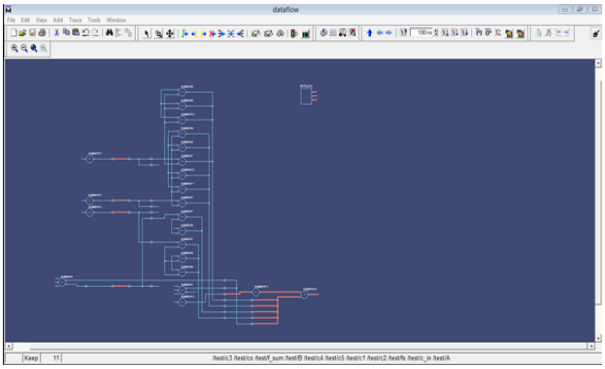


Fig.7 Data flow of proposed SQRT CSLA

5. Conclusion

Area, power and delay are the constituent factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the area, delay and power of CSLA architecture. The existing carry select adder has the disadvantage of more power consumption and occupying more chip area. The proposed SQRT CSLA using new logic formulation has low power consumption, less delay and reduced area than all the other adder structures. The proposed CSLA architecture is therefore, low area, low power, less delay and efficient for VLSI hardware implementation.

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