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A Modified SHPWM Method for Multilevel Inverters for Uniform Utilization of Power Electronic Switches

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Abstract:

The carrier based sub-harmonic pulse width modulation (SHPWM) methods commonly used for multilevel inverters (MLIs) suffer due to the unequal utilization of power semi conductor switches. The numbers of switching transients are different at different levels. This paper develops a novel SHPWM scheme with equal switching counts for all the switches. Apart from the switch counts, the other merits such as output voltage magnitude, the total harmonics distortion (THD) are same as basic SHPWM. The novel method is developed first then tested for seven level cascaded MLI using MATLAB-Simulink tools. The results such as output voltage, harmonic spectrum and THD are presented.

I. INTRODUCTION

An "inverter" is a static circuit which provides ac power from dc source with controllable voltage and frequency. The basic circuit for inversion is the H-bridge, which gives three level output ($+V_{dc}$, 0, $-V_{dc}$) i.e. a square wave and thus it can be named as a square wave inverter. Since the output is a square wave the distortion is very high due to the fact that the harmonic spectrum contained lower order harmonics with higher magnitude. To clear out these harmonics, bulky filters are needed to be designed, whose response is never going to be ideal and thus the purpose remained unfulfilled. Thus the usage of a square wave inverter was restricted for some sophisticated applications.

To enhance the performance of a square wave inverter, the Pulse Width Modulation (PWM) strategy was proposed and it proved its significance in the same. The aim of PWM control is varying the output pulse width such that it is proportional to required output (in this case, sine). Thus, the PWM control survives better for the inverter is Sinusoidal-PWM (SPWM). Here, a sine wave is the reference and triangular wave is taken as carrier, and comparison of both the signals gives pulses of

varying width proportional to the reference sine. Since the pulses are proportional to the sine wave, the output also takes the same fashion and thus the distortion is less. Also, the harmonics with high magnitude were shifted to a higher order decided by the number of commutations per cycle, which in turn is directly related to the frequency of the carrier signal. This eased the filtering since no bulky inductance and capacitances are needed and also the size of the module was considerably reduced. This control method laid a strong base for the three level inverters and thus they are being made useful in some sophisticated applications and dominating in the last three decades.

Though the evolution of PWM strategy helped the riposte of the three level inverter, it could not help out in some of the problems encountered. The usage of a three level PWM inverter for high power applications was restricted due to the fact that when the devices are chopped from higher voltage to zero level for many times per cycle, the loss across the devices increases and hence circuit efficiency reduces. Also, it is well known fact that the basic PWM strategies limit the fundamental component value to 86.6% that can be obtained from square wave. Thus the industrial applications of three level inverters were restricted and this made the research strong, which evolved with the proposal of "Multilevel inverters".

A multi-level PWM technique has been developed to reduce the lower order harmonic distortion (Corzine et al., 2004). The implementation of the existing control strategies for a diode-clamped MLI has been found to affect the switch utilisation and increase the losses (McGrath and Holmes, 2002). The effective switching has been reduced through the introduction of phase shift in the carriers. The variable frequency carrier band (VFCB) has been found to equalise the number of switching at all levels and contribute to reducing the losses besides allowing uniform dissipation of power in the switching devices (Tolbert and Habetler, 1999). Hybrid modulation techniques have been utilised in an inverter with the same number of sources as a cascade inverter to produce an output with increased number of levels (Manjrekar et al., 2000).

An analytical solution of the PWM techniques used in MLI inverters has shown that the harmonic components produced by alternative phase opposition disposition (APOD) technique in diode clamped inverter is the same as that of phase shifted carrier (PSC) technique in cascaded inverter (Zainal et al., 2003). Two novel carrier-based PWM methods namely carrier overlapping PWM and carrier overlapping SFO PWM have been found to yield better harmonic characteristics than the conventional PWM methods and found to offer encouraging results even for lower modulations indices (Tolbert and Habetler, 1999).

After understanding the scope of research in the area of multilevel inverters, the aim of this project work is solving all the problems listed. The objective of this project is,

(i) Understanding and simulation of all the control strategies available in the literature.

(ii) Comparison of the existing strategies to get a better idea of their feasibility with the circuit configurations.

(iii) Proposing a strategy that gives equal switching in all levels, with good harmonic characteristics.
(iv) Proposing strategies for easy implementation in digital platform.
(v) Hardware implementation of the novel circuit with the proposed control strategies.

II CASCADED MLI

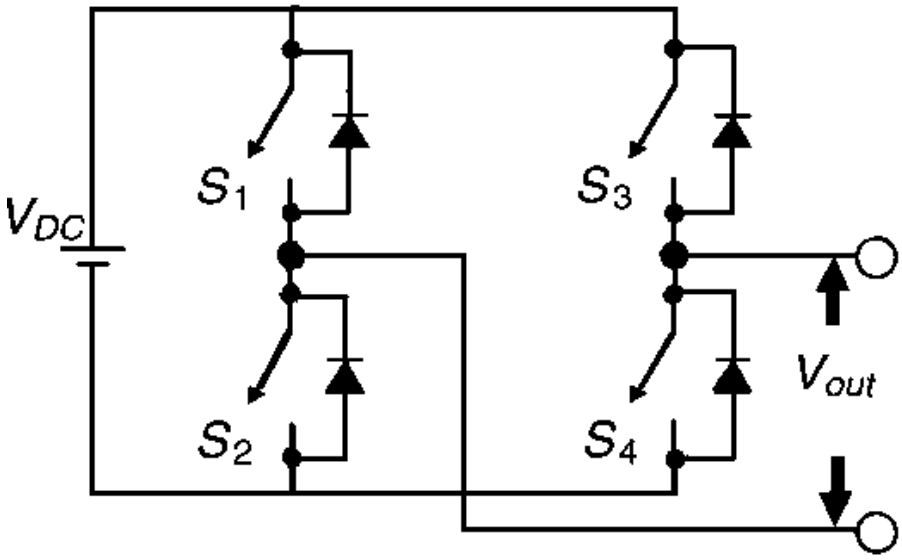


Fig:1 Single phase H-bridge inverter

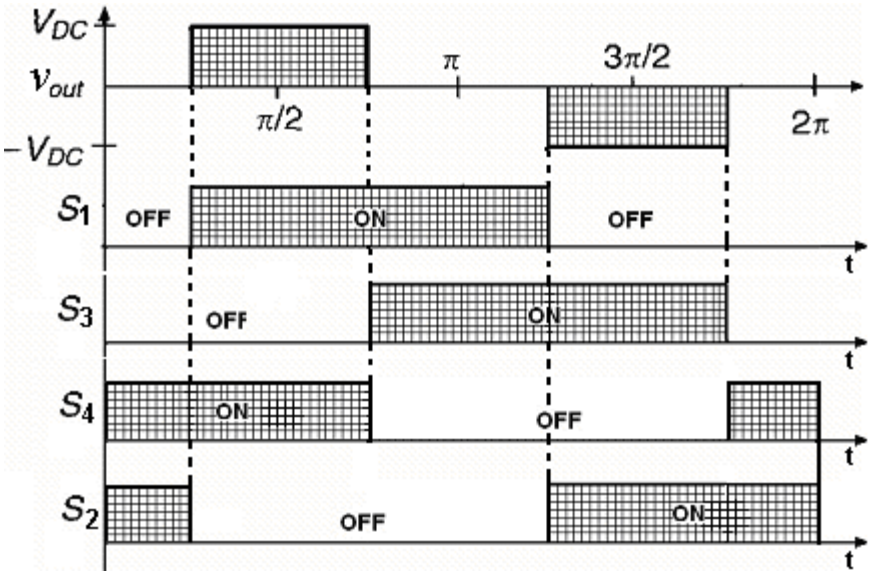


Fig:2 Control signals and output waveform

The inverter is composed of multiple units of power cells. Each power cell is mainly composed of an H-bridge inverter powered by a three-phase diode rectifier connected to an isolated secondary winding of a phase shifting transformer. The power cells in an inverter phase are normally connected in cascade on their ac output side to achieve high voltage operation and low harmonic distortion. In practice the number of power cells in a drive is mainly determined by the operating voltage and manufacturing cost. The number of voltage levels in a CHB inverter can be found from m=2H+1, where H is the number of H-bridge cells per phase.

III MODULATION SCHEMES FOR CASCADED MLI

The modulation schemes for the multilevel CHB inverters can be generally classified into carrier based modulation, space vector modulation and stair case modulation with selective harmonic elimination.

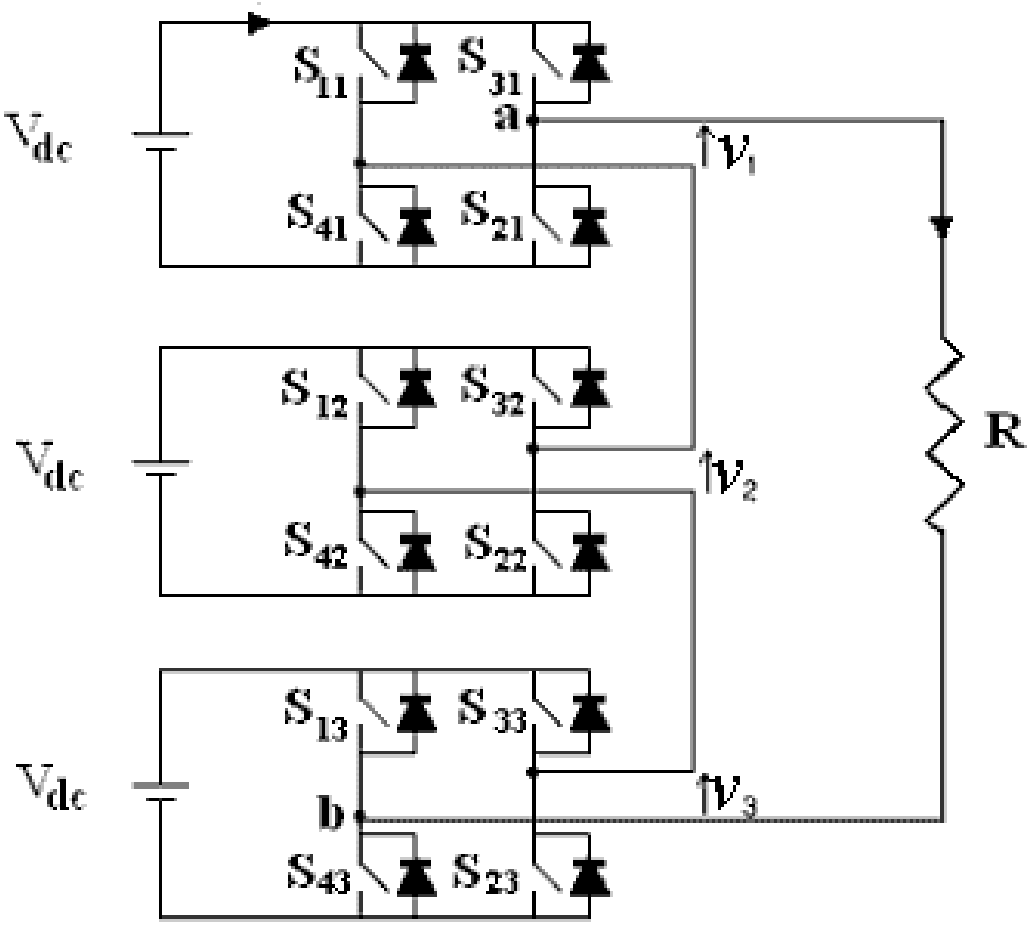


Fig.1: 7-level cascaded H-bridge inverter

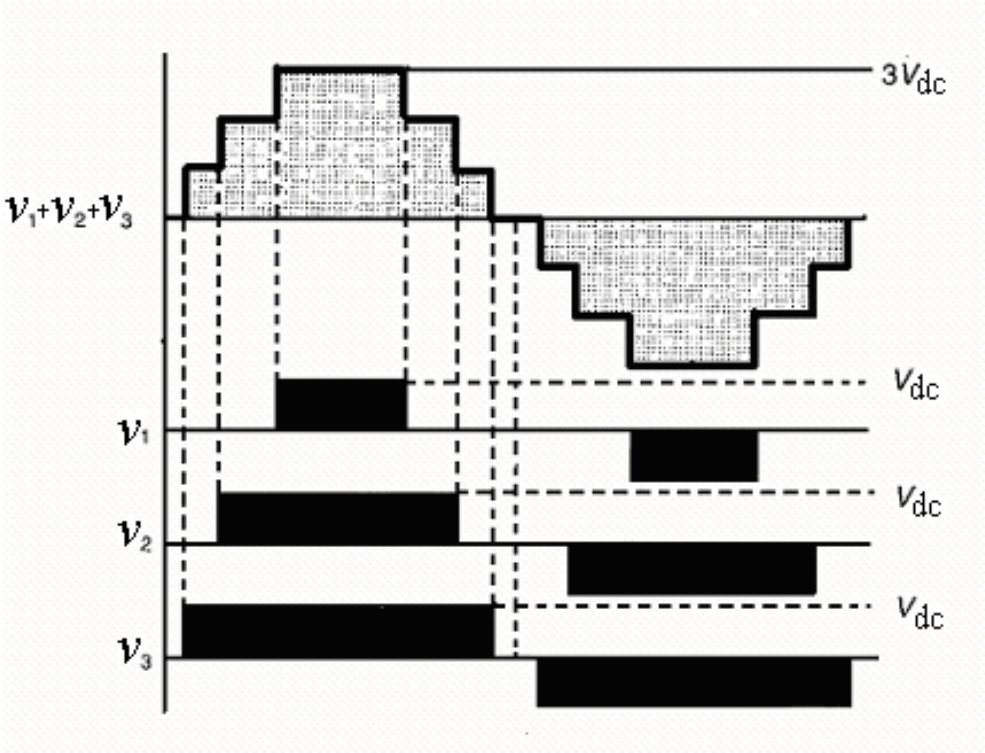


Fig.2: Output waveform

The stair case modulation scheme with selective harmonic elimination (SHE) is simple to implement. All the switching angles can be calculated off-line and the stored in look up table for digital implementation. Compared with the carrier based PWM schemes, the staircase modulation features low switching losses due to the fact that all the $IGBT_s$ operate at the fundamental frequency it is one of the preferred methods for the multilevel CHB inverter. It should be pointed out that the equations for the switching angles calculation are nonlinear and transcendental and thus may not always have a solution for all values of m_a.

GENERAL LINE DIAGRAM:

The proposed topology for multilevel inverter with a high number of steps associated with a low number of power switches for producing all levels (odd and even) at the output voltage, a procedure for calculating the required dc voltage source is proposed. This unit requires bidirectional switches with the capability of blocking voltage and conducting current in both the directions shown in figure 6. The advantages of this configuration over the previous one is that each bidirectional switch requires or gate driver circuit therefore this configuration is widely used in multilevel inverter [11].

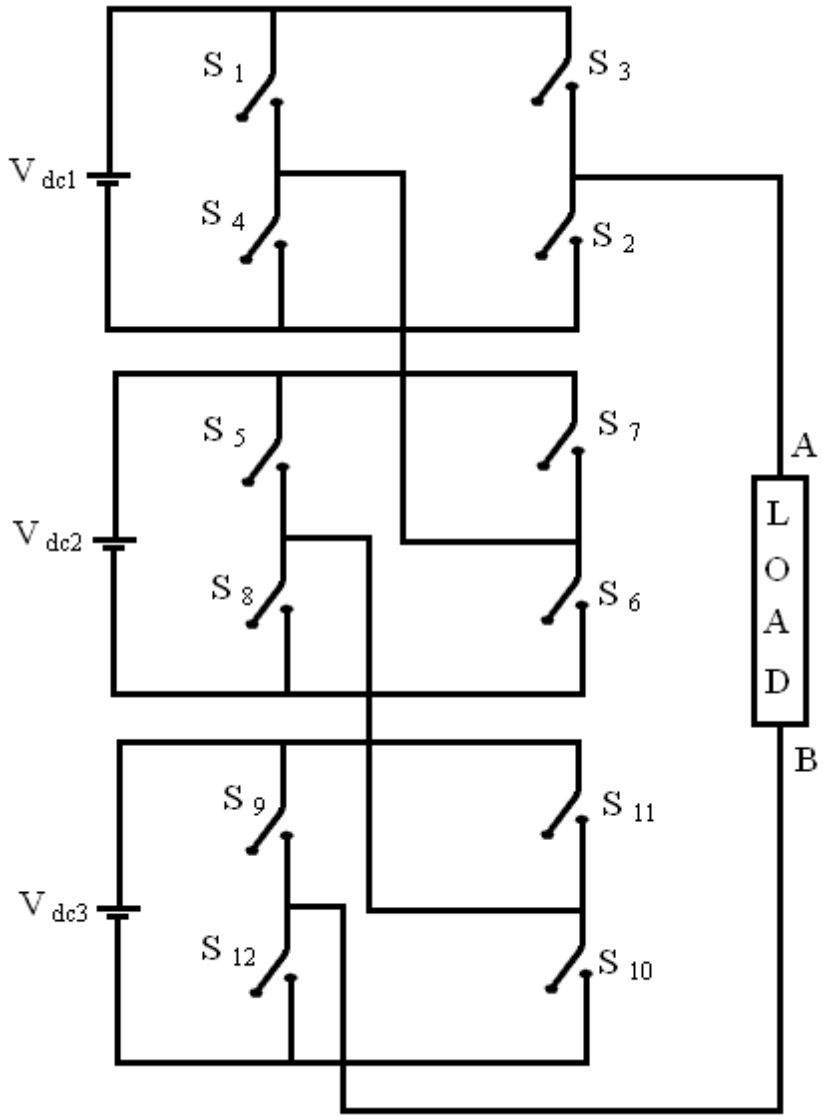


Fig.5: Line Diagram of 7 level MLI

It is possible to achieve the same plane of distortion provided by a higher level inverter, in a lower level inverter, by controlling the switching fashion of the main components i.e. with the help of control strategies it is possible to achieve lower distortion in multilevel inverters with less number of levels (components). Considering the above statement, this project work is done on a seven level inverter (V_3, V_2, V_1, 0, - V_1, -V_2, -V_3).

Multilevel inverters incorporate an array of power semiconductors and capacitor voltage sources, the output of which generate voltage with stepped waveforms. The distortion in the output gets lowered still more, if the number of level

increases. But this increase in the number of level increases the complexity of the circuit and control.

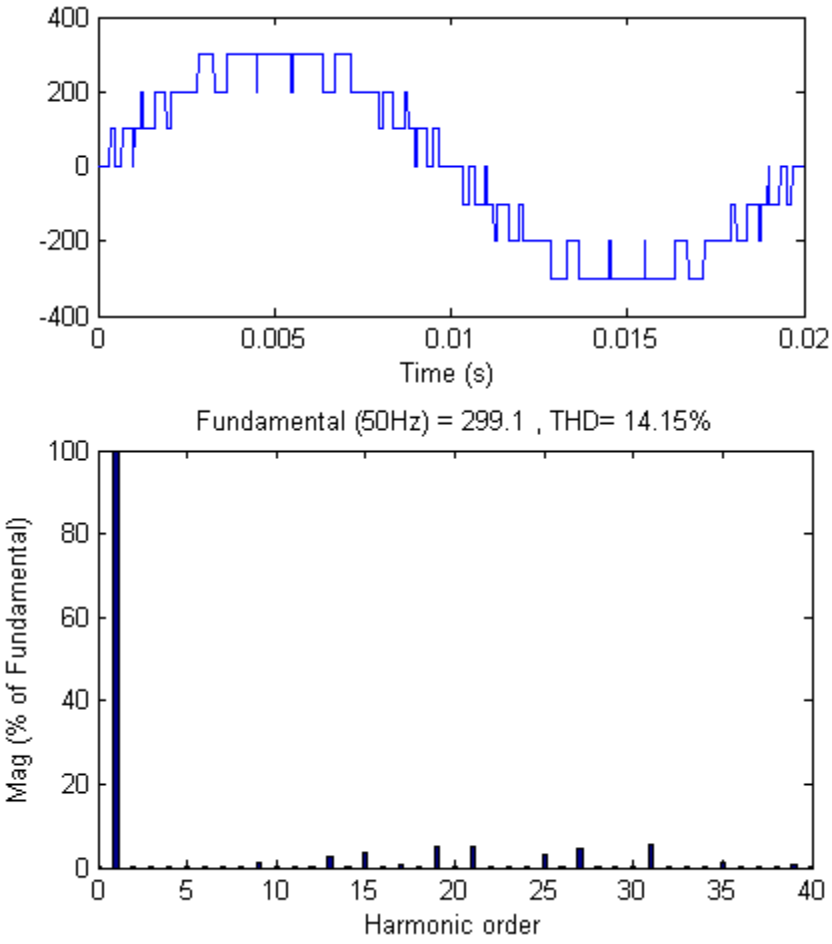


Fig.6: Output of 7 level MLI

Variation of SHPWM:

Sub-Harmonic PWM is an exclusive control strategy for multilevel inverters and has further classifications.

They are:

- Phase Disposition (PD)
- Alternative Phase Opposition Disposition (APOD)
- Phase Opposition Disposition (POD)
- Phase Shifted Carriers (PSC)
- Carrier Polarity Variation (CPV) and
- Variable Frequency Carrier Bands (VFCB)

IV VARIABLE FREQUENCY CARRIER BANDS SHPWM

It can be inferred that the numbers of switching in all levels are not equal and this introduces the problem of shortening the life of some of the devices The devices operating for the higher level gets short its life because they are subjected to more number of switching that too at higher voltages. This problem stands as a big hindrance when module of bridges is used in hardware implementation. It is not used to change few components in a module which are worn out instead of changing the whole module.

Making number of switching in all levels equal, equalizes the switching loss (heating) and hence equal life and circuit reliability. This can be achieved by having different carrier frequency (M_f) in different levels. The lower level should contain carriers of high frequency and the succeeding level carriers with considerably lower frequency. Making of Switching in All the Levels Equal, equalizing the Switching Losses and Equal Life of All the Devices, Hence Variable Frequency Carrier Bands

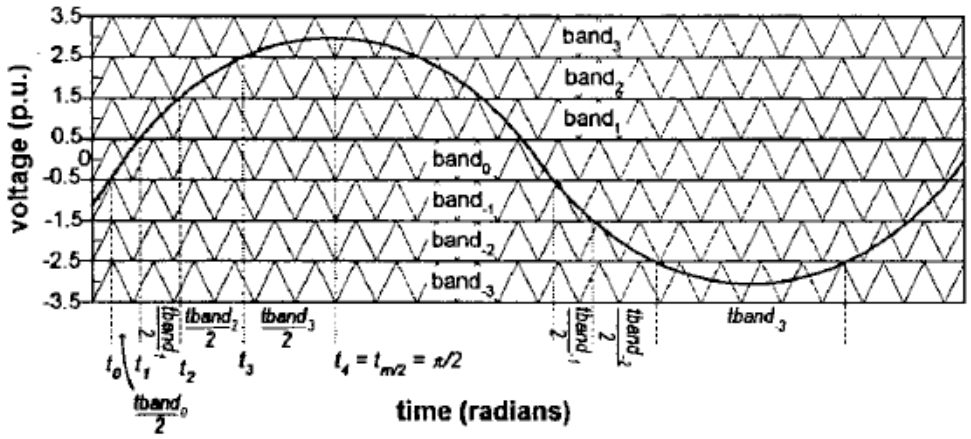


Fig.7: SHPWM

For a sine-wave modulation (reference) waveform centred in the carrier bands, the duration of time that the waveform exists during each of the bands occupied can be computed as follows. Using the amplitude symmetry of the sine wave about the time axis, the band crossing times where the reference waveform crosses from one band to an adjacent band, for bands above (or containing the zero axis in the case that is even) can be computed from The band dwell times in radians (starting at the band adjacent to the zero axis in the case that is odd or the band occupying the zero axis in the case that is even) are then Calculated Because of the symmetry of the sine wave about the zero axes.

$$t_n = \arcsin\left[\frac{2n - \operatorname{mod}\left(\frac{m-1}{2}\right)}{m_a * (m-1)}\right]$$

n= 1, 2, 3,..... $\left[\frac{m-1}{2}-1\right]$,for m odd

n= 1, 2, 3,..... $\left[\frac{m}{2}-1\right]$,for m even

The existence of the reference in each band is,

$tband_n = 2 * (t_{n+1} - t_n)$

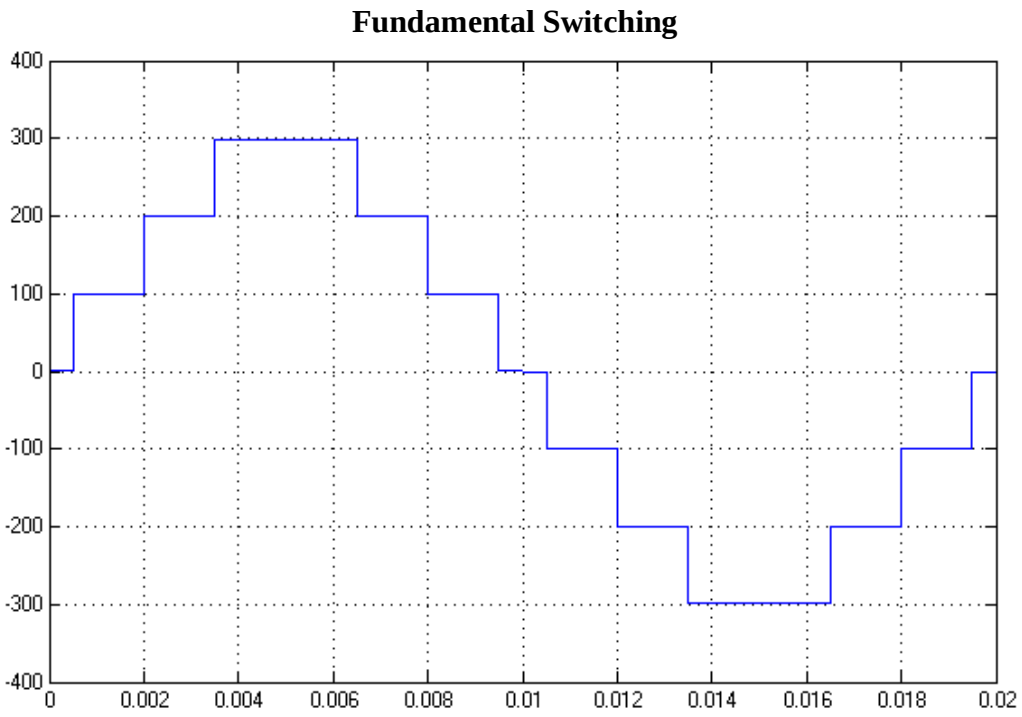
n= 0, 1, 2,..... $\left[\frac{m-3}{2}-1\right]$,for m odd

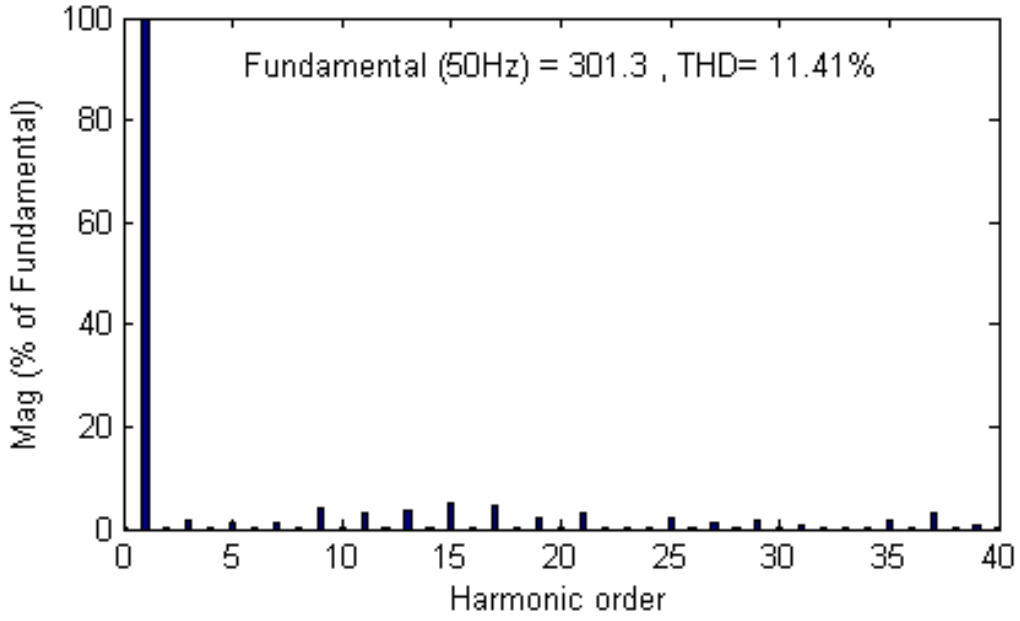
n= 0, 1, 2,..... $\left[\frac{m-2}{2}-1\right]$,for m even

And thus the frequency of the carrier in each band is,

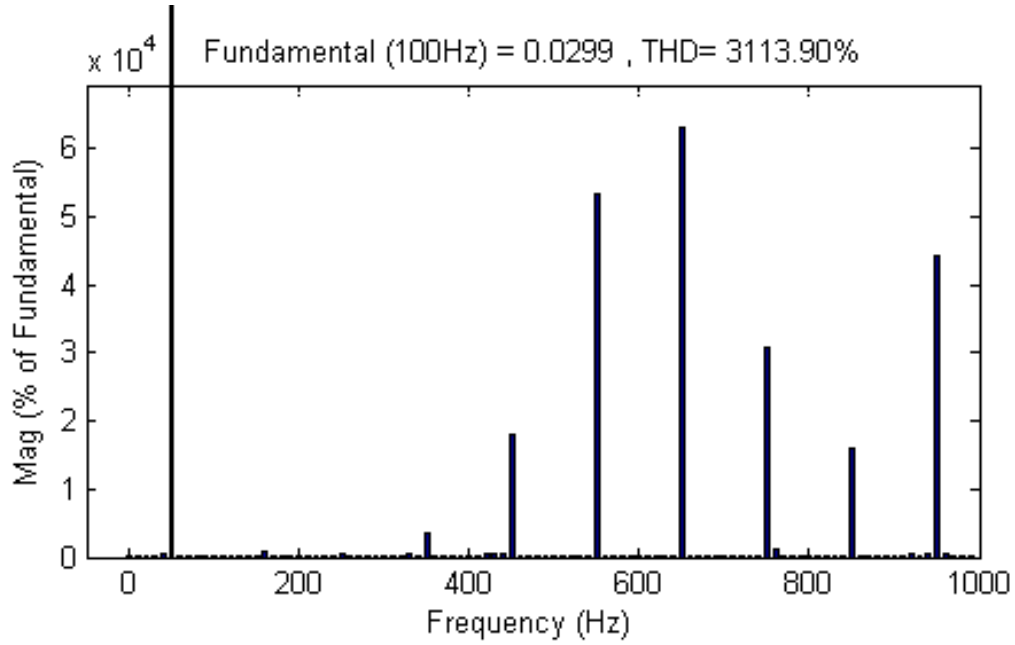
$$M_{fn} = \frac{\pi * N_{sw}}{tband_n}$$

V SIMULATION RESULTS

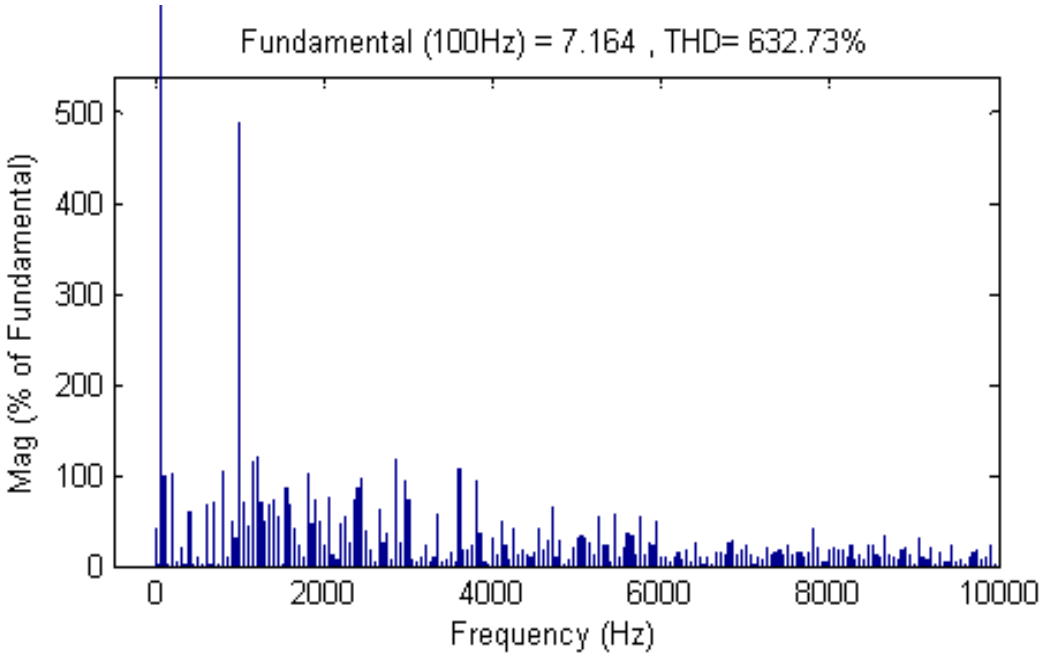



Fundamental (50Hz) = 301.3 , THD= 11.41%
Mag (% of Fundamental)
Harmonic order
0
20
40
60
80
100
0
5
10
15
20
25
30
35
40

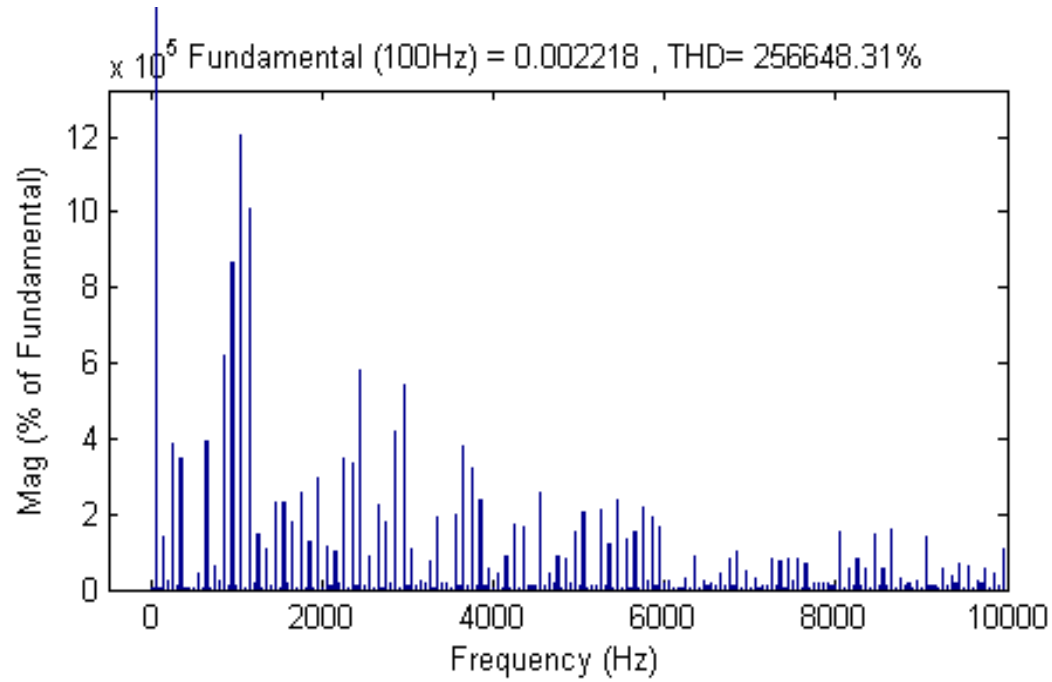
APOD


x 10^4
Fundamental (100Hz) = 0.0299 , THD= 3113.90%
Mag (% of Fundamental)
Frequency (Hz)
0
1
2
3
4
5
6
0
200
400
600
800
1000

PD


Fundamental (100Hz) = 7.164 , THD= 632.73%
Mag (% of Fundamental)
Frequency (Hz)
0
100
200
300
400
500
0
2000
4000
6000
8000
10000

POD


x 10^5 Fundamental (100Hz) = 0.002218 , THD= 256648.31%
Mag (% of Fundamental)
Frequency (Hz)
0
2
4
6
8
10
12
0
2000
4000
6000
8000
10000

VI CONCLUSIONS

This paper has demonstrated the Novel method for Invariable Carrier Frequency PWM Scheme for Balancing Switching Transitions in Multi Level Inverter. This Invariable multilevel inverter structure and its basic switching operations have been discussed. A procedure for equalizing the switching of the multilevel inverter using variable frequency carrier band has been described. In the conventional methods as the number of levels are increased the required number of switches also increased in abnormal conditions. Due to involvement of high number of switching operations thereby increasing the harmonics, switching losses, cost and the total harmonics distortion the proposed method dramatically reduces the switches for high number of levels. But the proposed topology involves considerably less number of switching operation for higher levels.

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