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High Speed And Area Efficient Network On Chip

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Abstract

As the technology is getting integrated, the power dissipation, latency and performance gets affected. Delay and area is an important concern in all the technology fields. Many techniques and routing algorithms have been used to earlier to reduce the power dissipation and area occupied at the link of an NOC, but area and delay is also a major concern. In this paper the main emphasis is given on reducing the delay and area coverage during the transfer of data especially during the encoding process. Therefore the minimization of switching activity at the I/O interfaces can reduce the area as well as increase the speed. This paper puts forward innovative encoding techniques suitable for minimizing the switching activity of system level address buses. In particular the schemes such as the various bus invert techniques like- full invert, half invert and odd/even invert reduce the power consumption and delay. But for performance issue to further reduce the delay and area coverage an innovative encoding technique 'Modified Bus Invert Transition Signalling (MBITS)' have been used at the links of NOC. Experimental results of this encoding technique have demonstrated the effectiveness of the proposed method.

KEYWORDS- I/O interfaces, Bus invert techniques, Modified Bits Technique.

I. INTRODUCTION

NETWORK ON CHIP (NOC):

In systems with intensive parallel the required bandwidth, latency and power consumption may not be provided by the buses; in such cases the solution will be the use of an embedded switching network called Network-on-Chip, to interconnect the IP modules in SOCs. NOCs normally cover more space as compared to bus based solution. The architecture of NOC is m*n mesh of switches where resources are placed on the slots formed by the switches.[4]

The architecture of NOC is an on chip communication infrastructure which consists of the physical layer, data link layer and network layer of the OSI protocol stack. An NOC mainly consists of three building blocks –

1. Links
2. Router and
3. Network adapter or network interface (NI).

Links physically connect the nodes and helps in implementing the communication. ***Router*** also implements the communication protocol and also acts as a smart buffer. The last block ***Network Interface*** makes the logical connection between the IP cores and the network.

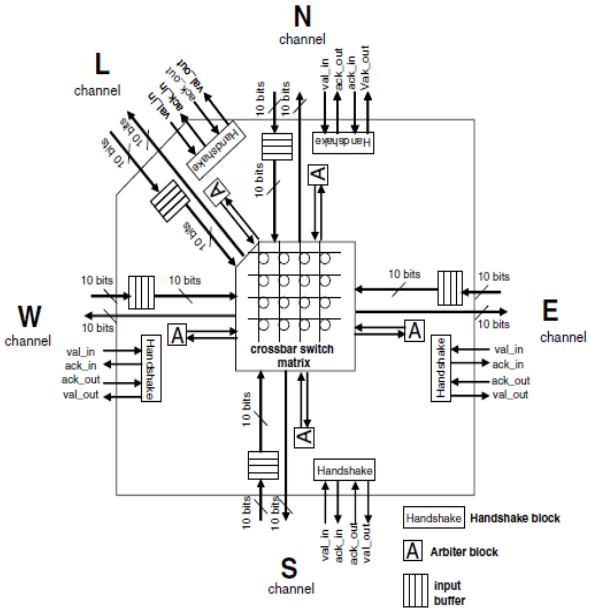


FIG 1: ARCHITECTURE OF A TYPICAL ROUTER

NOC TOPOLOGIES:

There are two different topologies in which a router of NOC can be connected and those are-

1. Direct topology
2. Indirect topology

In ***Direct topology*** each node is connected to a fixed number of neighbour nodes and information between two nodes goes through one or more intermediate nodes. In this topology only the routers are engaged and further communication is based on the routing algorithm implemented by the routers. In ***Indirect topology*** only some routers are engaged in propagating the messages through the network. [4]

PERFORMANCE PARAMETERS OF NOC:

NOC performance is evaluated based on three parameters, that are-

1. Bandwidth
2. Latency and
3. Throughput.

The maximum rate at which a data is propagated when a message is in the network is called its ***bandwidth*** and is calculated in terms of ***bit per second.*** The maximum amount of information delivered per unit time is called its ***throughput*** and is measured in terms of ***messages per second. Latency*** is defined as the time required or taken between the beginning of transmission of a message and its reception at the target node and is measured as the units of time.[4]

The rest of the paper is organized as follows. The related works are briefly discussed in SECTION II, while SECTION III presents an overview of the proposed data encoding schemes. The simulation results of the proposed encoding scheme have been discussed in SECTION IV and the comparison and results are described in SECTION V. Finally this paper is concluded in SECTION VI

II. RELATED WORKS AND CONTRIBUTIONS:

DIFFERENT TECHNIQUES AND ROUTING ALGORITHMS USED IN NOC:

Many techniques and routing algorithms have been used in NOCs to upgrade its performance by reducing the energy consumption and delay. Some of the technique used so far are- Deterministic routing, Adaptive routing, Switching, Store and forward strategy, Wormhole strategy, Virtual cut through mechanism, Buffering mechanism etc.

In Store and forward mechanism the data which is transferred is splitted into packets, each packet containing routing information. As soon as a packet reaches a node, it is stored in a buffer and hence to determine the exact output port routing information is extracted. This technique helps in reducing the switching activities thereby reducing the power dissipation at the nodes [2].

The Efficient RC low power bus encoding method was generally used for crosstalk reduction which in turn reduces the dynamic power dissipation as well as the wire propagation delay. Hence this technique eliminates the worst crosstalk types and reduces more total power consumption [3].

In Wormhole strategy, a novel end-to-end data encoding schemes has been used which exploits the wormhole technique to reduce the power dissipation by the NOC links. It reduces the power dissipation due to both self switching and the coupling switching activities [6].

In Virtual cut-through technique information of the routing process is in the first bytes of the packet. As soon as the output port is determined, the packages are sent instead of saving the entire package as in the case of store and forward mechanism [2].

BUS INVERT TECHNIQUE:

The Bus invert method has shown a positive upgrade in performance of NOC by reducing the power consumption as well as delay and area. In the Bus invert technique they are using half invert, full invert and odd/even invert during the encoding schemes at the links of NOC [1]. In the encoding scheme if the select line is 00 then the transition type will be full inversion which means the data will be fully inverted, (e.g.- Consider the data 01010101 so after applying full inversion the output data will be 10101010). If the select line is 01 then inversion of the data takes place at the odd places of the data, (e.g.-Consider the data

10101010 so the odd inverted data will be 11111111). Same will be in the case of even and half invert. Table 1 shows different types of bus invert and their corresponding conditions-

TABLE 1: DIFFERENT TYPES OF BUS INVERT TECHNIQUES

SELECT LINES	INVERSION TYPE	INPUT DATA	ENCODED DATA
00	Full inversion	10101010	01010101
01	Odd inversion	10101010	11111111
10	Even inversion	10101010	00000000
11	Half inversion	10101010	01011010

This technique allows saving up to 51% power dissipation and also performance upgrades. By simulating the technique the performance parameters thus obtained are shown in TABLE 2 and TABLE 3

ENCODER

TABLE 2: AREA, DELAY AND POWER VALUES OBTAINED BY USING BUS INVERSION TECHNIQUES IN THE ENCODER.

TYPES	AREA	DELAY	POWER
Half invert	61	3.1ns	56.87mW
Full invert	59	3.5ns	56.87mW
Odd/Even invert	60	3.5ns	56.87mW

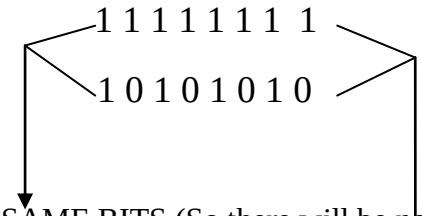
DECODER

TABLE 3: AREA, DELAY AND POWER ANALYSIS BY USING BUS INVERSION TECHNIQUES IN THE DECODER

TYPES	AREA	DELAY	POWER
Half invert	39	3.5ns	57.05mW
Full invert	36	3.4ns	57.05mW
Odd/Even invert	38	3.5ns	57.05mW

III. PROPOSED METHODOLOGY:

Modified bits technique is used to decrease the area overhead and time delay. In this methodology a predefined set of one's is taken for reference and any data input is given to the encoder. In this particular technique only the bits which are different between the input data and the predefined reference data will be transmitted. Suppose 11111111 is the predefined data and the input data is 10101010 so the output of the encoder will be 01010101. This can be explained briefly as given below-



SAME BITS (So there will be no transition and the output will be 0).

DIFFERENT BITS(So transition occurs and output will be 1)

So the final output is obtained as- 01010101

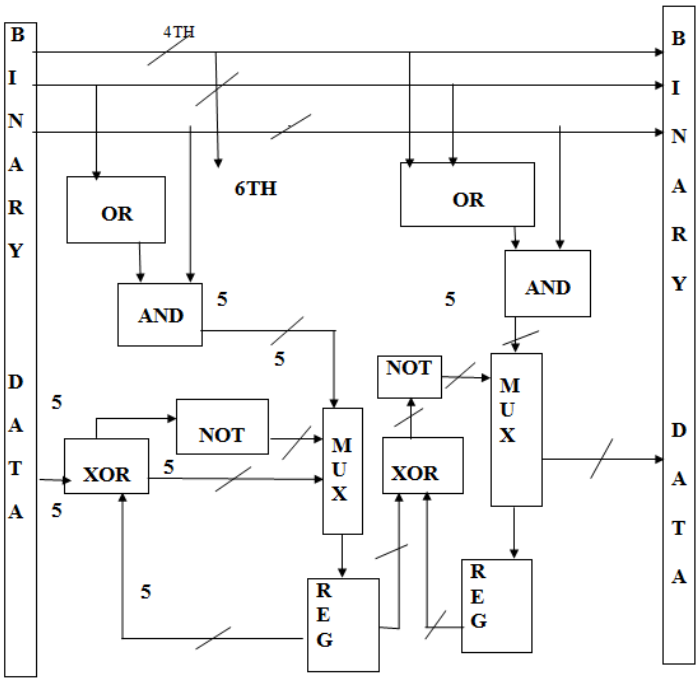


FIG 3: MODIFIED BITS ENCODER AND DECODER

FIG 3 shows the encoder and decoder to be used in the Modified Bits technique in a NOC. A reference data is taken which will be predefined and any binary input is given to the encoder. In the encoder the input data will be compared with the reference data and only the bits which are different will be transmitted hence reducing the number of transitions.

As the number of transitions is reduced, the power consumption will be reduced to a less extent and area and delay will be reduced. By simulating the process we get the desired reduced area as well as delay. Hence this technique is much more effective then the previously used encoding technique in NOC's.

This technique has been effectively simulated and desired area and delay reduction has been obtained as compared to the previously used Bus Invert technique.

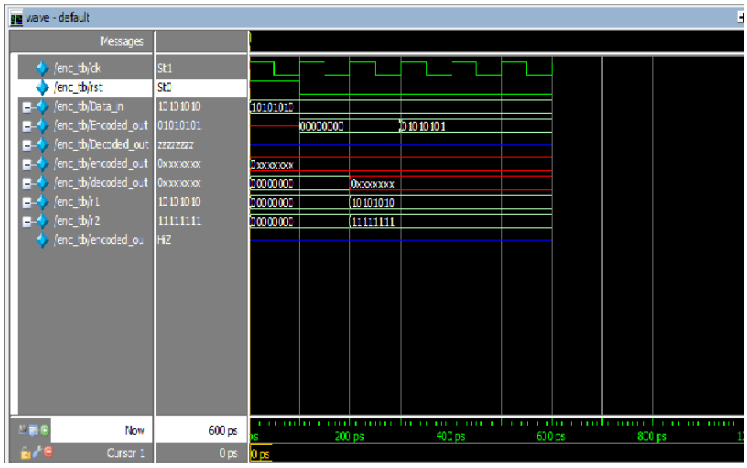
IV. SIMULATION RESULTS:

The simulation of the proposed Modified Bits technique has been done using the ModelSim-Altera 6.4a (Quartus II 9.0) Starter Edition. The simulation results of both the encoder and decoder by using the Modified Bits Technique has been shown below-

ENCODER

INPUT=10101010

OUTPUT=01010101

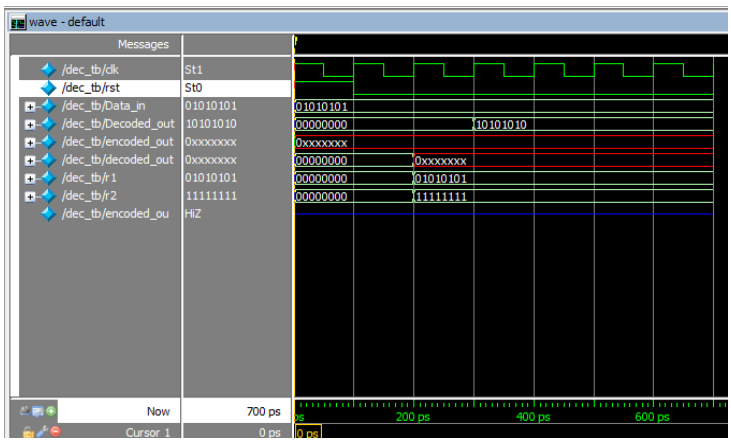


Input is given as 10101010 so after comparing with the predefined data 11111111 by using the Modified Bits technique the output is obtained as 01010101. By using this technique only the different bits to the predefined data will be transmitted hence reducing the number of transitions.

DECODER

INPUT=01010101

OUTPUT=10101010



Same is in the case of the decoder, the encoded data will be given as input and the output will be obtained which was the input to the encoder. Here the encoded output was 01010101 so the decoded data is 10101010.

PARAMETER ANALYSIS:

After doing the simulation of the encoder and decoder by using the modified bits technique the parameters like- Area, delay and power has been calculated using the Quartus II 9.0 Web Edition software. TABLE 4 shows the values of Area, Delay and Power obtained by using the proposed methodology.

TABLE 4: AREA, DELAY AND POWER ANALYSIS FOR ENCODER AND DECODER BY USING MODIFIED BITS TECHNIQUE.

TYPES	AREA	DELAY	POWER
ENCODER	25	1.6ns	56.68mW
DECODER	28	1.18ns	56.68mW

V. RESULTS AND DISCUSSION:

Thus, by using the Modified Bits technique the area and delay has been reduced as compared to previously used techniques. Also a small amount of power reduction has also been obtained but it is very less. So this technique will improve the performance of a Network on Chip by reducing the area as well as delay. The simulation has been done by using **ModelSim-Altera 6.4a (Quartus II 9.0) Starter Edition** and the parameters are obtained by using **Quartus II 9.0 WEB EDITION** software. Below is listed the comparison of Area, Delay and Power for the previously used Bus invert techniques and the proposed modified Bits technique.

ENCODER

PARAMETERS	BUS INVERT	MODIFIED BITS
AREA	60	25
DELAY	3.5ns	1.6ns
POWER	56.87mW	56.68mW

DECODER

PARAMETERS	BUS INVERT	MODIFIED BITS
AREA	47	28
DELAY	3.2ns	1.18ns
POWER	57.05mW	56.68mW

Below is given two charts showing the parameters obtained by using the Bus Invert and Modified Bits Technique in both the encoder and decoder. Chart 1 shows the Area, delay and power comparison of the Encoder whereas Chart 2 shows the same for the Decoder.

COMPARISION CHARTS:
ENCODER

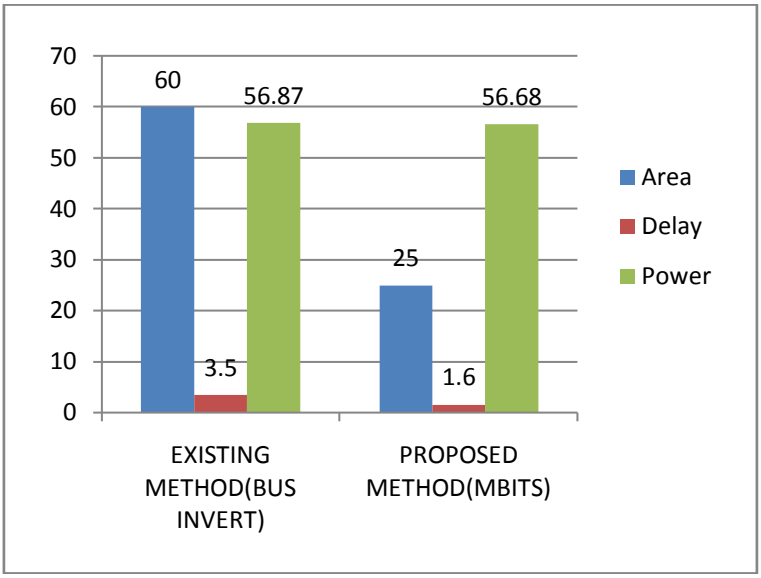


CHART 1: AREA, DELAY AND POWER COMPARISION FOR ENCODER BY USING BOTH EXISTING AND PROPOSED METHODS.

DECODER

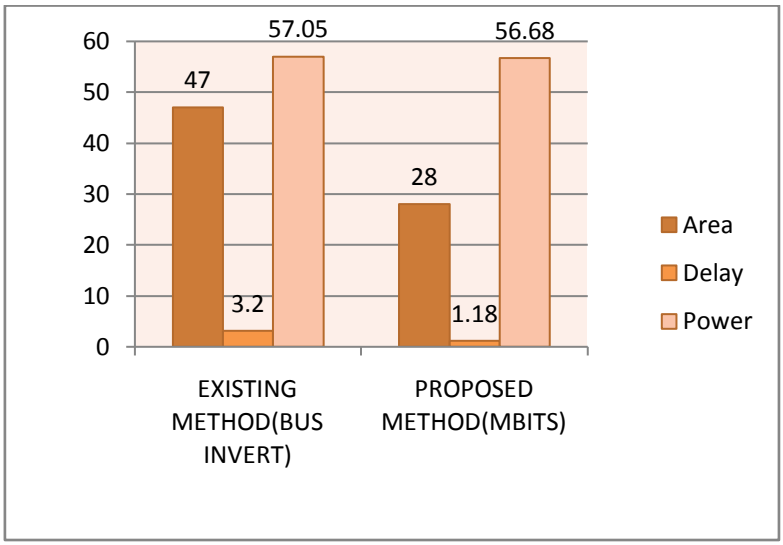


CHART 2: AREA, DELAY AND POWER COMPARISION FOR DECODER BY USING BOTH EXISTING AND PROPOSED METHODS

By comparing the parameters obtained by using the bus invert and Modified bits technique in the NOC we found that there is a decrease in the area coverage as well as delay but the power dissipation is not reduced to a great extent, only a small reduction in power dissipation is obtained.

VI. CONCLUSION:

In this paper a new set of encoding schemes have been presented focussed at reducing the area coverage and delay by the links at the nodes of an NOC. As compared to the previous encoding schemes proposed in the literature, the main aim behind the proposed methodology is to reduce the area and delay, thereby enhancing the performance of the NOC. Hence by using the proposed Modified Bits technique area and delay has been reduced without any significant performance degradation.

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