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Complex Circuit Model Analysis Using CDTA and SNAP

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Abstract

The paper deals with the implementation details of a symbolic analysis of complex circuit models including the transistor level in the symbolic simulator SNAP. Recent advances in approximate symbolic analysis enable applying the analysis to circuits with tens of transistors. The SNAP simulator allows combining high-level behavioral models with transistor-level ones. All models are defined in a text-based library, which can be easily extended by the user. Each model in the library is represented by its matrix-stamp for the Generalized Modified Nodal Analysis. Two algorithms of approximate symbolic analysis are implemented. The first algorithm simplifies the circuit model and the second simplifies the generated formula. The paper describes the modeling style and a procedure for automated extraction of small-signal models of semiconductor devices from the output file of the PSpice simulator.

Keywords: Symbolic analysis, frequency domain, transistor-level circuits, small-signal model, CAD, matrix methods

I INTRODUCTION

The applicability of exact symbolic analysis of linear circuits in the frequency domain is constrained to relatively small circuits, as the size of the resulting expression grows exponentially with the number of nodes and components. If we appropriately restrict the range of frequency and network parameters, the majority of symbolic terms can be removed from large expressions without any significant numerical error. Negligible symbolic terms are identified numerically, based on the known parameters of circuit components [1].

Simplification methods can be divided into three classes according to the stage of analysis at which the simplification is performed: *Simplification Before Generation* (SBG), *Simplification During Generation* (SDG), and *Simplification After Generation*

(SAG) [2]. The SAG methods are algorithmically simple but very expensive in terms of computation and storage. The rather mathematical methods of the SDG type [3] have problems with the interpretability of resulting expressions. In addition, their implementation is very complex. The SBG methods simplifying the circuit equations or graphs are the most effective, as they work with a relatively small number of circuit equations. Since SBG techniques directly operate on the network model, the simplification is inherently more appropriate and intuitive from the point of view of the expression interpretability.

There are two commercial programs for symbolic analysis nowadays. *Analog Insydes* [4] implements the SBG method of [2] consisting in the deletion of circuit equation coefficients. The program is designed as an add-on to the Wolfram MATHEMATICA system, which is not easy to use for a beginner. Symbolic algorithms implemented in the *Tina* simulator [5] are suitable for small circuits. In addition, there are several public-domain programs. An interesting program is *SIASCA* [6], in which, however, the set of available active elements is limited and the program requires MAPLE for its operation. The *SAPWIN* program [7] provides a simple symbolic approximation. Models of new elements can be created only in the form of SPICE-like subcircuits.

With respect to the limited size of circuits being analyzed by the above-mentioned programs, the variety of active circuit elements [8] whose behavioral models should be included in the libraries or the prohibitive price it seems useful to create a software tool with the aim of overcoming all these limitations. With respect to the large number of the variants and modifications of present-day active elements, and with respect to the future development in this area, the library of such a simulator should be open and give the possibility of easy definition of behavioral models for new circuit elements. At the same time, the program should allow the use of complex SPICE transistor-level models and be able to extract linear models at a given operational point for subsequent approximate symbolic analysis.

The paper describes SNAP (Symbolic Network Analysis Program), which is currently being redesigned to comply with the above-mentioned requirements. At present the program implements SBG and SAG simplification algorithms [9]. Section 2 of the paper deals the implementation of open modeling and Section 3 provides an example analysis.

II IMPLEMENTATION OF OPEN MODELING

2.1 Circuit Model

The linear circuit being analyzed is considered without independent sources. Then it can be represented by the Generalized Modified Nodal Analysis in the form

$$H\,x = 0\,, \qquad (1)$$

where H is the indefinite hybrid circuit matrix, and x is the column vector of unknown voltages and currents. The indefinite matrix is singular (det(H) = 0) as no element is connected to the virtual reference node [10]. This is in order to avoid using different

computational procedures for floating and grounded input and output ports.

The circuit is always considered a two-port network. All network functions can be expressed symbolically by means of algebraic cofactors of H [10].

Each network element is defined by its "stamp" in the simulator library. The stamp describes how the parameters of an element appear in the hybrid network matrix, which allows defining symbolic behavioral models. Each matrix entry can be a rational fraction function containing element parameters, constants, and complex frequency *s*. A simplified small-signal model of a current conveyor whose ideal behavior is described by the equations

$$Vx\ Vy,\ IZ\ ^{I}x \bullet \qquad (2)$$

The conveyor's non-ideal properties are described by parasitic elements C_x, C_Z, R_z, and the frequency-dependent 1 l+sz$^{-}_{z}$

$$Y_x(s) = R_x\ 1 + sr\ P$$

where R_x, ;, and ; are parameters of the admittance model.

Figure 1 shows the matrix-stamp of the model. The first four rows and columns correspond to nodes *x*, *y*, *z*, *g (1* to 4). The fifth row and column is for internal node 5, and the sixth row and column is for the controlled voltage source.

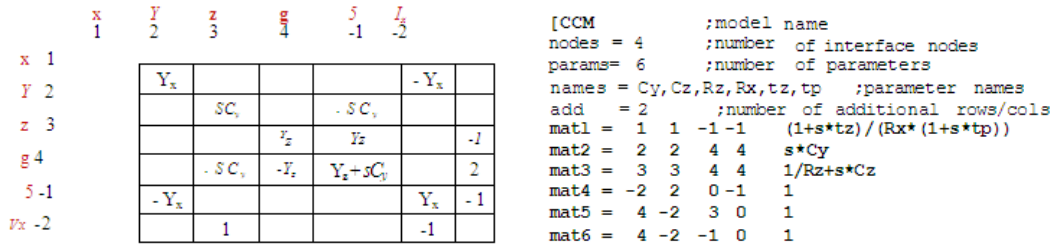


Fig. 1 Conveyor model

The stamp element P_i (from mat_s= *abcd:* P_i) appears with the positive sign in positions *(a,b)* and *(c, d),* and with the negative sign in *(a,d)* and *(c,b).* The coordinates are numbered according to the local numbers of the device nodes. The first additional row and column are denoted "-1" while "0" means "no entry" to the matrix, i.e. "-1" corresponds to node 5. The line *mat4* defines the coefficients +1 and -1 in the sixth row of the matrix, and *mat5* and *mat6* define the current coupling coefficients in the sixth column.

2.2 Small-signal parameter extraction

The parameters of linear circuit elements can be easily set by the user. However, small-signal parameters of nonlinear elements depend on the DC operating point, whose computation represents a nontrivial problem. For this reason, it is more convenient to use a standard Spice simulator to obtain small-signal parameters.

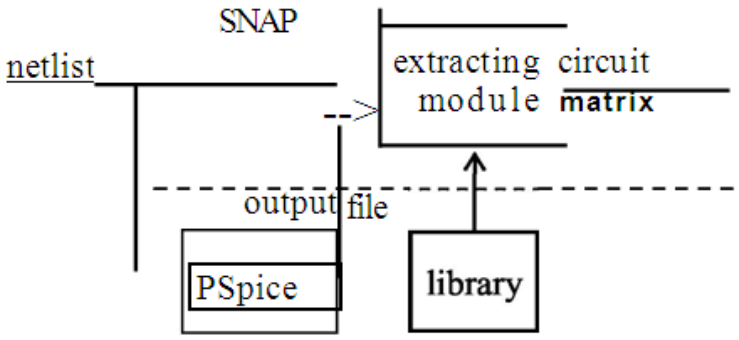
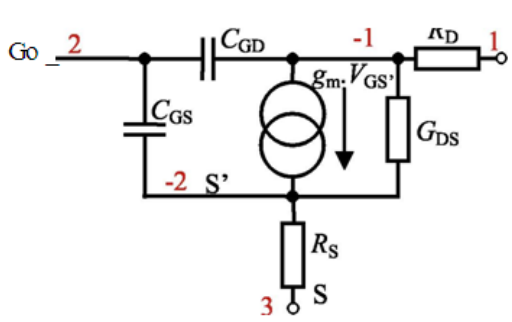


Fig. 2 Extraction of small-signal circuit model.

In the case of transistor-level circuits, SNAP accepts a Spice-compatible netlist where the input and output ports are identified by special schematic symbols. Each port has two variants, *DC-open* (implemented as an independent current source with zero current) and *DC-short* (implemented as an independent voltage source with zero voltage), to allow correct biasing of the circuit.




```
[JPI]
nodes  = 3
params = 6
names  = gm, gds,  Cgs,  Cgd,  Rd,  Rs
add    = 2       ;two internal nodes
matl   = -1  2    -2   -2  : gm
mat2   = -1  -1   -2   -2  : gds
mat3     2  2     -2   -2  : s*Cgs
mat4   = -1  -1    2    2  : s*Cgd
mat5     1  1    -1   -1  : 1/Rd
mat6   = -2  -2    3    3  : 1/Rs
```

Fig. 3 Small-signal model of J-FET and its library defmition.

After reading the netlist, SNAP calls the PSpice simulator to perform the operating point analysis **(.OP).** The PSpice output file, which contains small-signal parameters of all semiconductor elements, is read back to SNAP. The extracting module creates a linearized circuit matrix (1). Independent sources are removed during the process, and simple elements like R, L, or C are copied directly from the netlist. Small-signal models for all semiconductor devices implemented in PSpice are defined in the SNAP library. Fig. 5 shows an example for J-FET with two internal nodes denoted here as -1 and -2.

III EXAMPLE ANALYSIS

Fig. 4 shows the internal structure of the CDTA network element implemented in the

TSMC 0.35um CMOS technology [11]. CDTA contains an input Current Differencing Unit followed by a multiple-output OTA. The number *N* of symbolic terms of the nodal matrix determinant, i.e. the number of terms in the denominator of exact network functions, can be estimated from [2]

$$\det(A_i\, A^T{}_v\, N\, min(clet(A_v\, A^T{}_v), \det(A_/A_i{}^T\, 1.2210^{15}\, N$$
$$\min(3.75\ 10^{15}, 5.86\ 10^{15}) \qquad (4)$$

where $A_/$ and A_V are the incidence matrices of the current graph and the voltage graph, respectively [12].

With respect to the astronomical size in (4), the approximate symbolic analysis is the only means how to obtain a reasonable result. Using two control frequencies with allowed tolerances AM and AP

f_l = 100kHz: AM_1 = 1 dB, AP_1 = 5°,

f_2 = 700MHz: AM_2 = 2dB, AP_2 = 20°

we obtain the following simplified formula for the output impedance of the *z* terminal:

$$z = \frac{1}{g_{ds09}\, g_{ds14}\, s(C_{gs21}\, C_{gs22})} \qquad (5)$$

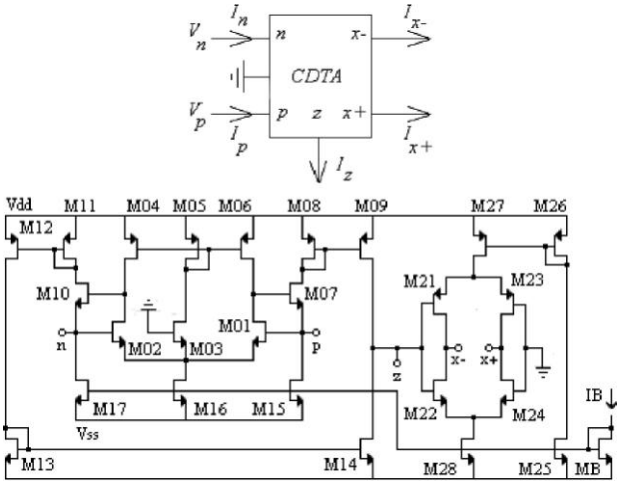


Fig. 4 Symbol of CDTA and its implementation in TSMC 0.35um CMOS technology [11].

IV CONCLUSIONS

The approximate symbolic analysis is a valuable tool for obtaining reasonable results for transistor-level electronic circuits. The procedure for automated extraction of small-signal models helps the user to speed-up the analysis and to avoid error-prone hand extraction from output files of Spice simulators.

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