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Applying G_m/I_D Methodology For The Designing of Self Biased OTA With Load Variation

Vikas Mittal
Asst. Professor
[a]Deptt. of Electronics & Communication Engg., MMEC, M.M.University, Mullana, Ambala, India, Vikasmittal2k7@rediffmail.com

Abstract

The present work addresses the design of power efficient fully self biased OTA using a design methodology based on the g_m/I_D transistor characteristics. This analog module was analyzed, designed and prototyped in TSMS 0.35μm CMOS technology. Experimental results are presented, in order to validate the methodology. The proposed OTA has enhanced Gain at 3db bandwidth and the UGB with lesser current consumption. The circuit does not need any DC external biasing circuit, only V_{DD} has to be applied. Here self biasing has been introduced with lesser power consumption. The results have been taken with load variations. This circuit is used in real time high frequency applications as in RF communication.

Keywords: Operational Trans conductance Amplifier (OTA), Trans conductance/Drain Current (gm/I_D), Self Biasing, Common Mode Feedback (CMFB), Analog Circuits.

Introduction

The development of ultra-scaled VLSI technologies, coupled with the demand for more signal processing integrated in a single chip, has resulted in a tremendous potential for design of analog circuits. Most VLSI systems require analog sub-systems such as amplifiers, comparators, filters, oscillators, digital-to-analog and analog-to-digital converters. Most often the technology process imposes design tradeoffs between designer's experience and analog design. More critical in deep sub-micron CMOS mixed-signal ICs, are the specifications of analog circuits that are sensitive to the random variations of the size and technology parameters . A conventional design approach achieves a similar performance with similar area, hence incurring much larger power dissipation and to deal with this problem a design based on gm/I_D methodology and characterization had been proposed [1].This proposed circuit was used for designing bandpass Gm-C filter. The simulated results encouraged for

experimental verification, of which good results were obtained & was concluded that the proposed methodology was able to achieve fast analog design with high level of automation . But it too had following limitations:

a) Need of external biasing circuitry for OTA.
b) High total current consumption & Power consumption.
c) Low gain of OTA.

In this paper we will identify a self biased OTA which will respond to load variations and its response will be seen on basic IC parameters viz. gain, bandwidth, slew rate , power dissipation etc The proposed self biased OTA shall meet the following objectives:

a) No Need for any external biasing circuitry.
b) Maintaining gain stability with overall increase in gain.
c) Decrease in Power consumption.

This Paper is organized in five sections. The first section introduces the role of self biasing for gain and power efficiency. The second section addresses the design methodology. The application of the methodology for the design of OTA is presented in section 3. The validation of identified self biased OTA for various load variations is given in fourth section followed by the conclusion in Section 5.

The G_m/I_D Design Methodology

Most methods for analytical synthesis of analog circuits assume that the MOS transistors are in either strong inversion or weak inversion. The design methodology based on gm/I_D transistor characteristic, allows a unified synthesis methodology which is valid in all regions of operation of the MOS transistors [2]. In this proposed work , the relationship between the ratio of the Transconductance gain g_m over the DC drain current I_D and normalized drain current $I_D(W/L)$ will be used as a fundamental design relationship to explore the entire design[3][4]. The choice of g_m/I_D is based on its relevance for the following reasons:

a) It is strongly related to the performances of analog circuits.
b) It gives an indication of the device operating region.
c) It provides a tool for calculating the transistor dimensions.

Considering that the g_m/I_D ratio and normalized current $I_D(W/L)$ are independent of the transistor sizes [2], the relationship between them represent a unique characteristic for all the transistors of the same type (NMOS and PMOS) in a specific technology. This universal quality of gm/I_D vs $I_D(W/L)$ curve is used during the design phase, when the transistors aspect ratios(W/L) are unknown. Once the value of the gm/ID ratio is chosen i.e the device operation region is determined, the W/L of the transistor can be determined.

Applying The Methodology In The Design Of Self Biased OTA

The circuit for self biased OTA is shown in Fig.1. The biasing for the input transistors MN1 and MN2 are provided by the drain terminal (node P) of MP1, there is no need of external biasing circuit for operating this OTA. Here, there is only need to apply

AC input. Designing is in such a manner that the voltage at point P is 1.6534 Volt. Here MP1 is using also as a current source for providing current to MN3 and which is mirroring in MN4.

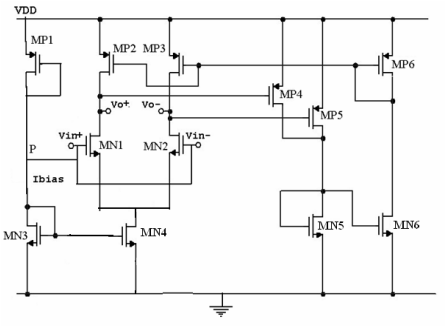


Figure 1: Self Biased OTA

Design Procedure by applying gm/I_D methodology for OTA

Considering the OTA design specifications and the chosen OTA architecture, the transconductor is calculated using the g_m/I_D methodology. For each transistor, the g_m/I_D factor is chosen, and then the normalized current $I_D/(W/L)$ is determined from the gm/I_D vs. $I_D/(W/L)$ curve for the target technology. Then, with the determined drain current value, the W/L of each transistor can be obtained. The transistors Length L are determined by a trade-off between area and Dc gain requirement(due to the dependence of the Early voltage on the transistor length).

Results

The circuit is simulated with the parameters obtained from the identified methodology. All values have been measured at load capacitance of 3pF. Prepared circuit of OTA is simulated at Tanner, T-SPICE tool at 0.35µ technology. Based on the OTA, input stage is fully self biased. The simulations include AC response, Transient analysis, DC Response. The responses have been checked for Load capacitance variation.

AC Analysis:

Here 1V AC is applied at input terminal of designed OTA. Here V_{DD} is 3.3V with respect to ground.

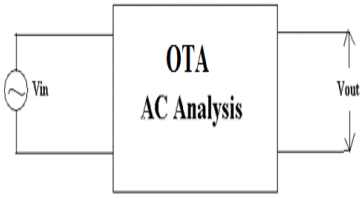


Figure 2: AC Analysis for a OTA

The netlist and the simulated AC results for the gain (magnitude in dB) with respect to frequency(Hz) has been shown in Fig.3. The parameters obtained are tabulated in Table 1.

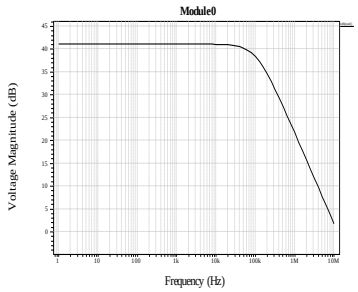


Figure 3: Plotted AC Response of OTA

Table 1: Obtained Parameters for AC Analysis

Gain	**41.35 dB**
3dB Bandwidth	**138.73 kHz**
UGB	**12.40 MHz**
Power Dissipation	**216.15 µW**

Transient Analysis

For observing the transient response of the OTA the test setup of Fig. 4 is used. In this setup sinusoidal signals are applied to the two inputs and the effective value of input signal is the difference of the voltage at the two terminals. No DC potential is applied along with the sinusoidal signal because the circuit is fully self biased.

Peak to Peak Voltage:

The simulated transient result for the magnitude in volt with respect to time (sec) is shown in Fig. 5. On applying 1mv (peak to peak) voltage as input, the output of 220mv (peak to peak) of 220mv has been obtained. Here max voltage swing is 1.72V and min voltage swing is 1.50V.

Slew Rate

The simulated transient results for the magnitude in volt with respect to time(sec) is shown in Fig. 5. On applying the input voltage peak to peak of 1mv, slew rate of 9.992 µs has been obtained.

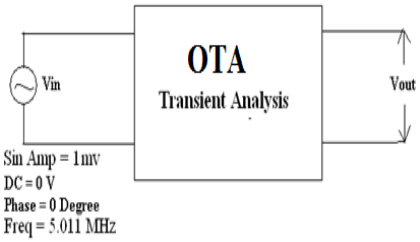


Figure 4: Transient Analysis for a OTA

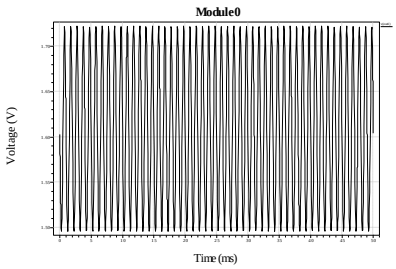


Figure 5: Simulated Transient Response for the OTA

DC Analysis

The main response of this circuit is the DC response. As no biasing voltage at the input is used, single voltage source i.e; power supply (V_{DD}) provides the necessary DC voltage at the input. Here the voltage of every node is almost equal to 1.65 volt.

(a) DC Value of V_{OUT1}

The voltage of node V_{OUT1} is plotted in Fig 6, When the value of V_{DD} is 3.3 volt, then on this value, the voltage at node V_{OUT1} is 1.61 volt

(b) DC Value of V_{OUT2}

The voltage of node V_{OUT2} is plotted in Fig 7, When the value of V_{DD} is 3.3 volt, then on this value the voltage at node V_{OUT2} is 1.61 Volt.

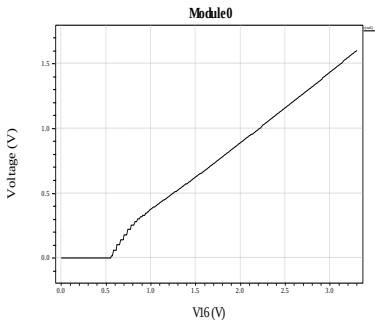


Figure 6: Voltage of Node V_{OUT1}

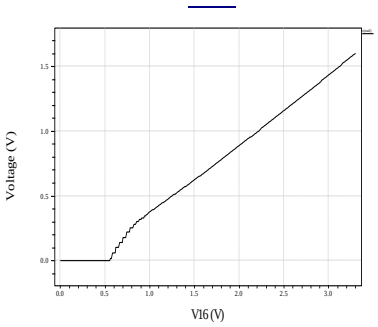
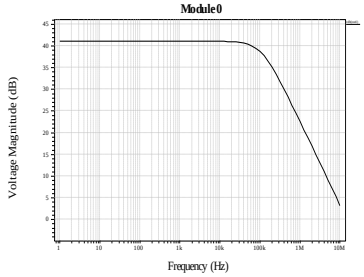


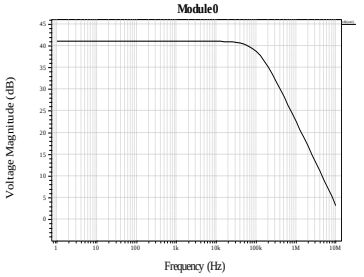
Figure 7: Voltage of Node V_{OUT2}

Load Variations

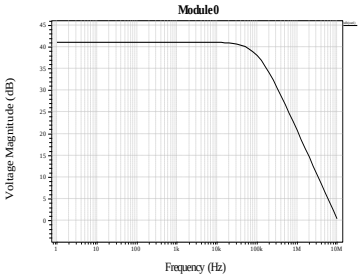
On applying different values of load capacitance differences in all the achieved parameters have been obtained. The achieved parameters have been plotted in the following figures for three different (2.5 PF, 3 PF, 3.5 PF) values..



At C_L = 2.5 pF



At C_L = 3 pF



At C_L = 3.5 pF

Figure 8: AC Analysis at different values of C_L

From the above plots, the following parameters have been obtained and are tabulated in Table 2.

Table 2: Obtained Parameters for different Loads

Achieved Parameters	**C_L = 2.5 pF**	**C_L = 3 pF**	**C_L = 3.5 pF**
Gain	41.27 dB	41.35 dB	41.13 dB
3dB Bandwidth	155.33 kHz	138.73 kHz	112.68 kHz
UGB	15.66 MHz	12.40 MHz	9.84 MHz
Power Dissipation	216.15 µW	216.15 µW	216.15 µW

From the tabulated results we can say that our prime objective of increasing the gain (over the previous papers) maintaining the gain stability has been done successfully.

Conclusion

Self biasing is the area of biasing, which reduces the area requirement of the circuit. As the technology is scaled down it is more important for a OTA to work at any CM level. Here in this thesis work, fully self biased OTA using a design methodology based on the g_m/I_D transistor characteristics is designed and simulated with the schematic of the circuit. The OTA has Gain of 41.35 dB and 3db bandwidth of 138.73

kHz and the UGB of 12.40MHz with the current consumption of 65.50 μA. The circuit does not have need of any DC external biasing circuit, only need to apply V_{DD} (3.3 V). Here self biasing has been introduced with power consumption of 216.15μW. Simulation result for load variations shows that the circuit can be used for wide range of load variation.

References

[1] Cortes, F. P., Fabris, E., and Bampi, S., "A band-pass Gm-C Filter Based on gm/ID Methodology and Characterization", SBCCI'06,Minas Gerais,Brazil, Aug28-Sept1, 2006.

[2] Silveira, F., Flandre. D., Jespers, P.G.A., A gm/I_D Based Methodology for Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon on Insulator micropower OTA. IEEE Journal of Solid- State circuits, vol.31, no.9, September 1996.

[3] Cortes, F. P., Fabris, E., and Bampi, S., "Applying the gm/I_D Method in the Analysis and Design of Miller Amplifier, Comparator and Gm-C filter", Proceedings of IFIP VLSI-Soc 2003, Germany, December 2003.

[4] Cortes, F. P., Fabris, E., and Bampi, S., "Analysis and Design of Amplifiers and Comparators in CMOS 0.35μm Technology", Microelectronics Reliability, Eselvier Ltd, vol. 44, pp. 657 – 664., April 2004.