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Simulation And Implementation Of Passive Soft-Switching Snubber Based PWM Inverters For Energy Recovery Applications

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ABSTRACT

It presents a regenerative passive snubber circuit for pulse-width modulation (PWM) inverters to achieve soft-switching purposes without significant cost and reliability penalties. This passive soft-switching snubber (PSSS) employs a diode/capacitor snubber circuit for each switching device in an inverter to provide low dv/dt and low switching losses to the device. The PSSS further uses a transformer-based energy regenerative circuit to recover the energy captured in the snubber capacitors. All the components in the PSSS circuit are passive, thus leading to reliable and low-cost advantages over those soft-switching schemes relying on additional active switches. The snubber can be incorporated in to a 150 KVA PWM inverter. Simulation and experimental results are given to demonstrate the validity and features of the snubber circuit.

I. INTRODUCTION

To reduce switching stresses, losses, and electromagnetic interference (EMI), soft-switching techniques have been developed for power converters since the 1970s. There are many topologies of soft-switching inverters, such as resonant dc link, resonant snubber, and zero-current transition inverters. Soft-switching inverters can be grouped into two main categories: resonant dc link and resonant snubber. The resonant dc link provides zero dc-link voltage or current intervals to all phase legs during switching instants, whereas the resonant snubber diverts current from and/or provides zero voltage intervals to each main device at switching instants. The active clamped resonant dc link converter and the auxiliary quasiresonant dc link converter, are examples of resonant dc link inverters. Auxiliary resonant snubber inverters such as the auxiliary resonant commutated pole (ARCP), zero voltage transition, and resonant snubber inverters belong to the second resonant snubber category.

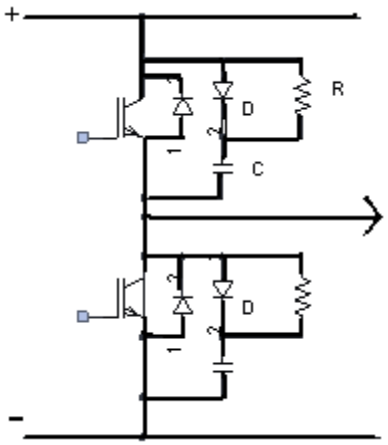


Fig 1 Inverter phase leg with RCD snubbers

An auxiliary quasi-resonant dc tank (AQRDCT) inverter is presented for achieving soft-switching. An AQRDCT circuit is coupled directly across a dc bus to the inverter to generate a quasi-resonant dc bus voltage. It consists of two auxiliary switches connected in the common phase leg as auxiliary switch leg a pair of dc capacitors connected in series as a dc tank and a resonant inductor in series with the lower devices of a auxiliary switch leg.The auxiliary switches are turned on and off softly .The AQRDCT circuit absorbs only ripples of the inverter dc bus current thus having less central stress.The ACRDCL resonates periodically bringing the dc link voltage to zero once each cycle.

The resonant dc link circuit acts as an interface between the dc power supply and the inverter and needs to transmit real power and to carry dc current from the dc power supply to the inverter or from the inverter back to the dc power supply via switches and/or resonant components which can lead to significant power losses. The voltage clamping,voltage control,& charge balancing become difficult due to the real power transmission.The current stress on the auxiliary switches and clamping switches is at least as high as that on the inverter main switches High voltage stress across the inverter switches and continuous resonant operation of the dc link.

Resonant DC link converters are showing tremendous promise for next generation adjustable speed AC machine drives. This paper presents bidirectional initial current control concept in the resonant circuit which solves the voltage overshoot problem in the resonant link and establishes reliable zero voltage crossing for smooth inverter operation. The resonant circuit for initial current selection. A circuit has been proposed to establish the bidirectional initial current. The improved inverter permits successful operation at 50KHz resonant frequency, and even promises upto 100KHz. The control of the inverter that involves prediction of the inverter input current has been formulated. A complete inverter-fed induction motor speed control system has been simulated on computer using PC-SIMNON. The simulation study at both 50KHz and 25KHz resonant frequency indicates the

superiority at higher resonant frequency.

Voltage over shoot high voltage stress is a generic problem in a resonant link inverter.Resonant delay at every cycle reduces the resonant frequency causing performance degradation of the inverter systemVoltage clamping limits the peak voltage volt second area of a pulse becomes larger aggravating the phase current ripple problem. A delta configured auxiliary resonant snubber inverter is developed to overcome the voltage floating problem in a wye configured resonant snubber inverter. The proposed inverter is to connect auxiliary resonant branches between phase output to avoid a floating point voltage which may cause over voltage failure of the auxiliary switches. It consists of resonant inductor and a reverse blocking auxiliary switch.Instead of using an anti-parallel diode to allow resonant current to flowing the reverse direction as in Y-configured version the resonant branch in delta configured version must block the negative voltage typically done in a series diode.

It requires dc link capacitor branch, which is center, tapped to accomplish commutation. It also requires voltage clamping devices to prevent over-voltage across the auxiliary resonant switch during resonant current resetting.

Existing zero current transitions converters do not solve main switch turn on problems and require auxiliary switches to be turned off with high current and therefore are not suitable for high power applications the zero current switching at both turn on and turn off not only reduces switching losses significantly but also eliminates the need for passive snubbers due to much reduced switch stress.It is suitable for dc-dc and three phase converters with IGBT's,MCT's,GTO's. Current commutation technique is not suitable for SCR converters are not suitable for gate controlled devices because they do not solve reverse recovery problem, have high power loss in auxiliary circuit some of them increases switch voltage stress or require switches to block negative voltage.

A new discrete pulse modulated current regulator which controls space vector that describes load current is introduced here. The new adjacent state discrete time current regulator, which switches between adjacent switching vectors and the zero state based on the state chosen by CRAM scheme Contains most of the operating characteristics of a cost function regulator which utilizes full state feedback. Hardware implementation is difficult.Controller does not require high speed. Additional control is required to maximize transient performance.

However, all existing soft-switching inverters use additional active devices to achieve soft switching, thus increasing costs and control complexity and decreasing reliability. Prior to the soft-switching technology, the RCD snubber circuit that consists of a resistor (R), capacitor (C), and diode (D), as shown in Fig. 1, had been widely used in PWM inverters to reduce switching stresses and EMI. The traditional RCD snubber is lossy and bulky, and it is difficult to apply to high-frequency switching PWM inverters because the losses in the snubber increase proportionally with the switching frequency. This paper presents a regenerative passive snubber circuit for PWM inverters that is able to achieve the aforementioned soft-switching objectives without significantly increasing the cost. This passive soft-switching snubber (PSSS) employs a snubber circuit consisting of diodes and capacitors for each phase leg to provide low dv/dt and low switching losses to the switching devices. The

PSSS further uses a transformer-based energy regenerative circuit to recover the energy captured in the snubber capacitors. All components in the PSSS circuit are passive, making it reliable and low in cost. The snubber has been applied to a 150 kVA PWM inverter. Simulation and experimental results are given to demonstrate the validity and features of the snubber circuit.

II. PSSS CIRCUIT AND OPERATING PRINCIPLE

The proposed PSSS circuit, which consists of a diode/capacitor soft-switching snubber (SSS) circuit for each phase leg, and an energy recovery circuit shared among all the phase legs, for a three-phase inverter application. The SSS circuit includes a snubber diode, Dsp, and a snubber capacitor, Csp, for the upper main device, Sp, and, symmetrically, Dsn and Csn for the lower main device, Sn .The functions of the snubber diodes, Dsp and Dsn, and snubber capacitors,Csp and Csn , are very similar to those of the traditional RCD snubber. They are, however, arranged differently so that both snubber capacitors are connected to the midpoint of the phase leg. Because the upper and lower main devices always operate complementarily to each other during normal PWM operation, the sum of both snubber capacitors' voltages should remain constant and equal to the dc link voltage, which is further guaranteed by a larger snubber bus capacitor, Cso, connected across the two snubber capacitors

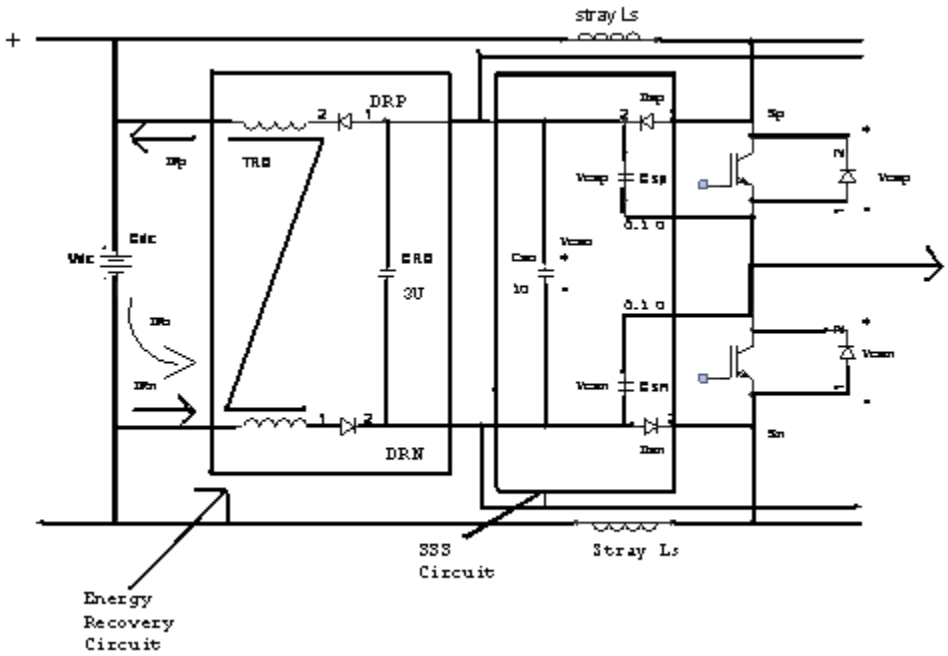


Fig 2 PSSS circuit

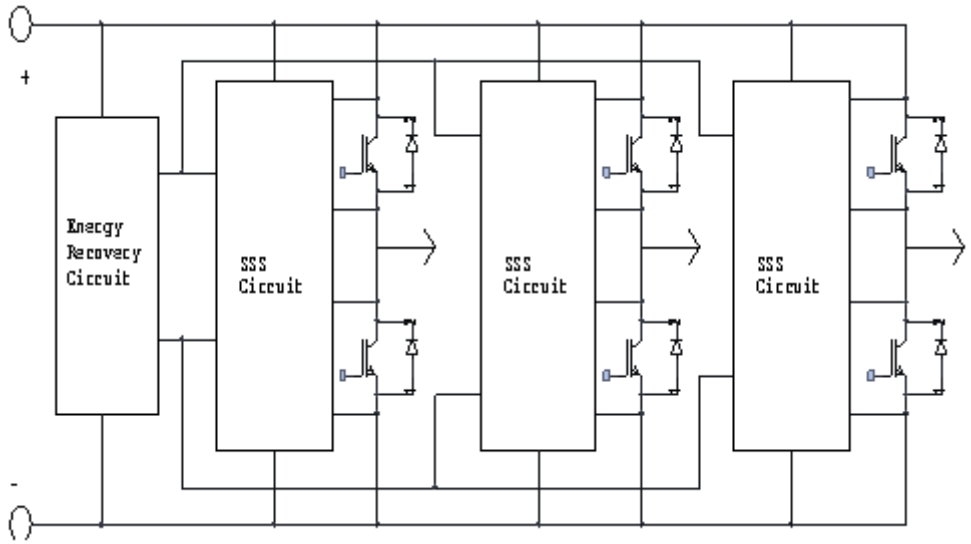


Fig 3 Block diagram

The energy recovery circuit that is shared by all the snubber circuits includes a capacitor, CRO, two diodes, DRp and DRN, and a transformer,TRO. The transformer, TRO, makes IRP equal to IRn so that a recovery current, IRO, flows into the dc link capacitor, Cdc.The two diodes, DRP and DRN, guarantee the energy recovery current (power) flows in one direction, i.e., from the snubber back to the dc link.

OPERATING MODES

Fig 4 explains the different operating modes in that Fig (a) Explains the equivalent circuit of the circuit while switching Fig (b) Explains the mode 0+ operation where Switch Sp is on and the conducting load current iL1 flows Fig (c) Explains the Mode 1 Where Switch Sp is turned off and the capacitor Csp is charged and Capacitor Csn is discharged Fig (d) Explains the mode 2 where diode Dsp and Diode Dsn clamp Vcsn to zero voltage and it carries current.

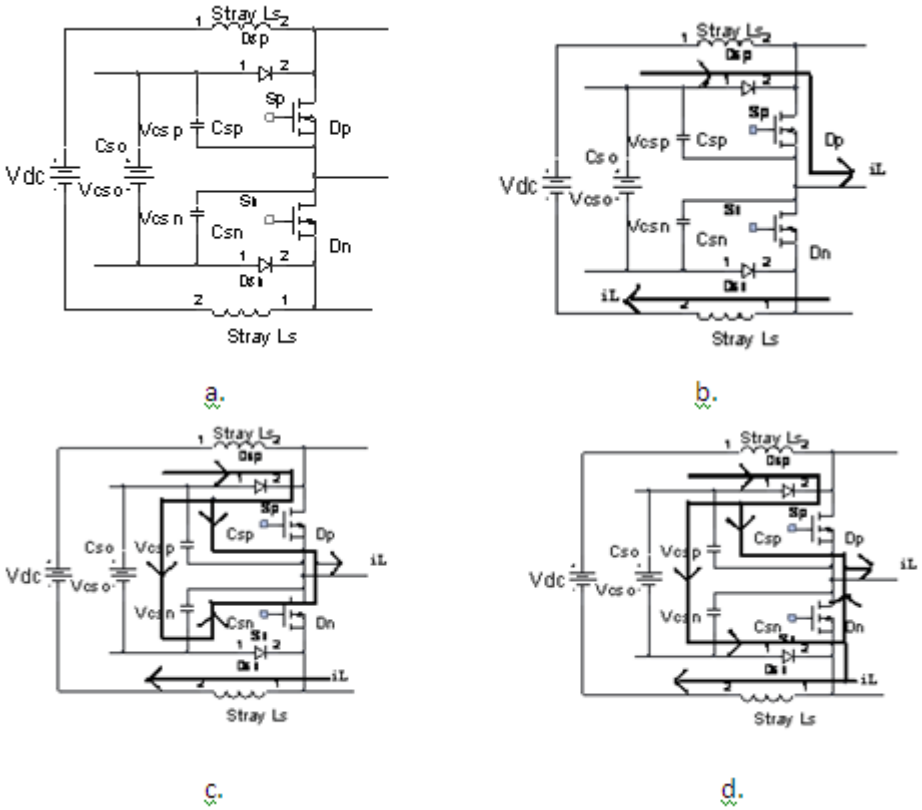


Fig. 4. Operating modes. (a) Equivalent circuit of the snubber circuit during switching. (b) Mode 0+: Sp is on and conducting load current. (c) Mode 1: Sp is turned off, charging Csp and discharging Csn . (d) Mode 2: Dsp and Dsn clamp Vcsn to zero voltage and carry current.

ENERGY RECOVERY CIRCUIT

The operating principle of the energy recovery circuit is shown here. The circuit has three current loops. Loop I includes the stray inductance of the positive dc link, the diodes Dsp and DRp and one of the transformer windings. Loop II is the energy recovery path and consists of the diodes Dsp and DRn, the capacitor CRo, the dc source, and the transformer. Loop III is the negative counterpart of loop I and includes the stray inductance of the negative dc link, the diodes DSn and DRn, and the other transformer winding. The transformer is connected like a common mode choke and thus presents a large inductance to Loops I and III to minimize the loop circulating currents. On the other hand, only the leakage inductance of the transformer is connected like a common mode choke and thus presents a large inductance to Loops I and III to minimize the loop circulating currents. On the other hand, only the leakage inductance of the transformer is seen in loop II, thus maximizing the energy recovery current and efficiency

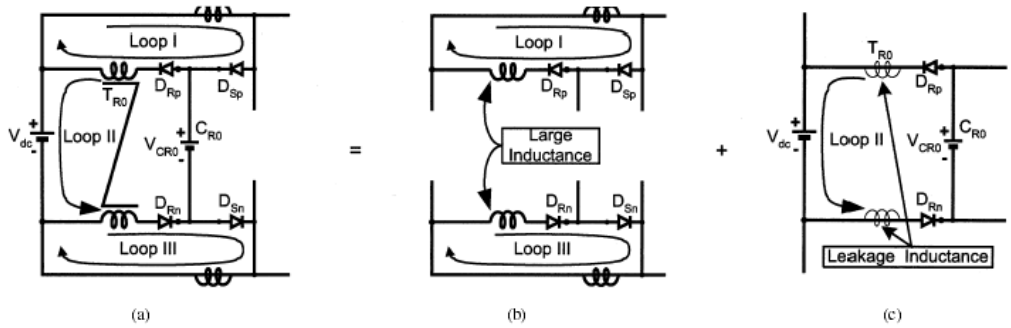


Fig 5 Energy Recovery Circuit (a)Equivalent circuit of the energy recovery circuit., (b)The transformer acts as a large inductance to Loops I and III to minimize circulating current. (c)The transformer has zero (or minimal leakage) inductance toward Loop II to maximize energy recovery current and efficiency.

ADVANTAGES:

(i) Employs only passive components
(ii) Requires no additional control
(iii) Allows any PWM schemes
(iv) Eliminates dc bus plane layout
v) Utilizes stray inductance Reduces dv/dt and di/dt

(vi) Lowers total inverter cost and improves reliability.

III. SIMULATION CIRCUITS

The proposed circuit is simulated using MATLAB

The diagram shown in Fig 6 is a passive soft switching snubber for pwm inverters. Here totally 6 gate pulse are given as input and 6 gate pulse are obtained as output. Here the voltage VDC is given as 330 V and a common ground is given to input voltage. A RL load is considered.

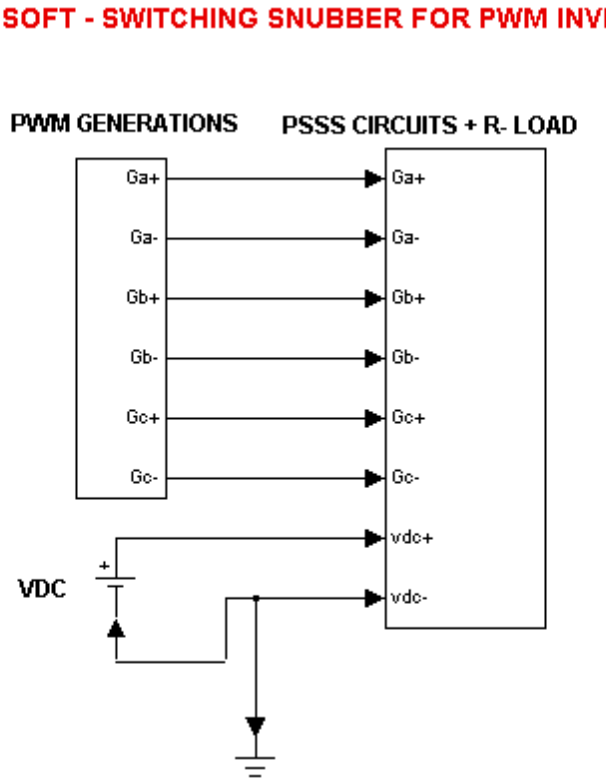


Fig 6 A passive soft switching snubber for pwm inverters

The diagram shown in Fig 7 is a PWM generation, in this a triangular pulse is compared with a sinusoidal pulse and the output is obtained. A phase shift of 120 degree is given. The output is obtained in the scope.

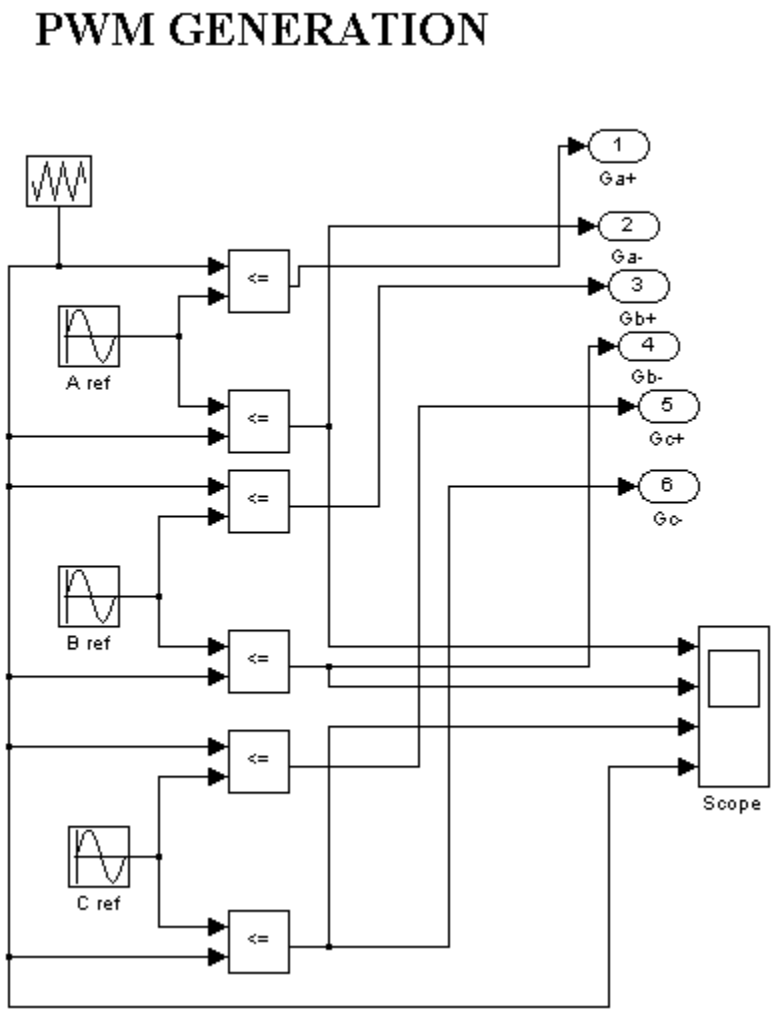


Fig 7 PWM generation

The diagram shown in Fig 8 is the gate pulses and here voltage both positive& negative is given to PSSS circuit and the output is obtained in the scope 1& 4 with filter and without filter respectively.

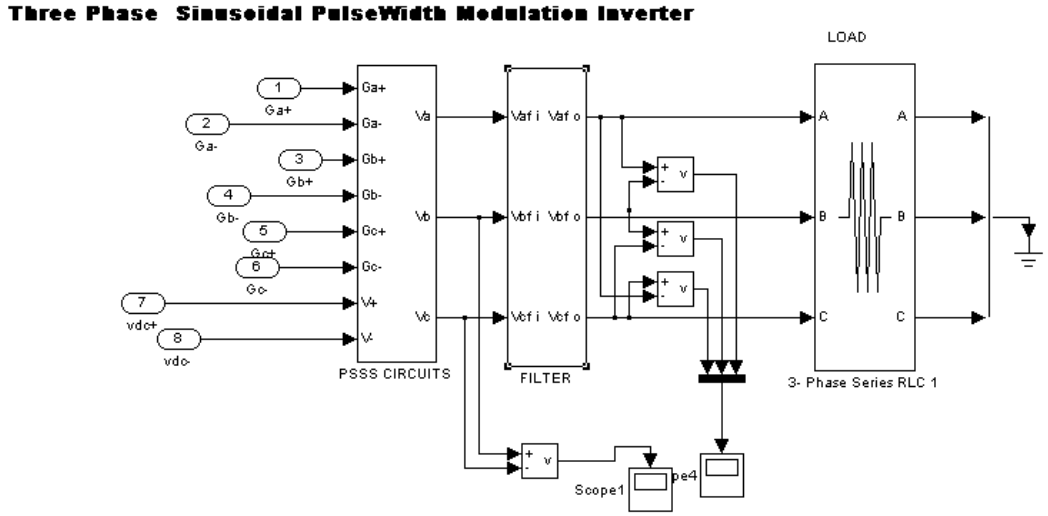


Fig 8 Three phase PWM inverters

The diagram shown in Fig 9 is a proposed PSSS circuit for all the three phase with MOSFETS as a switch.

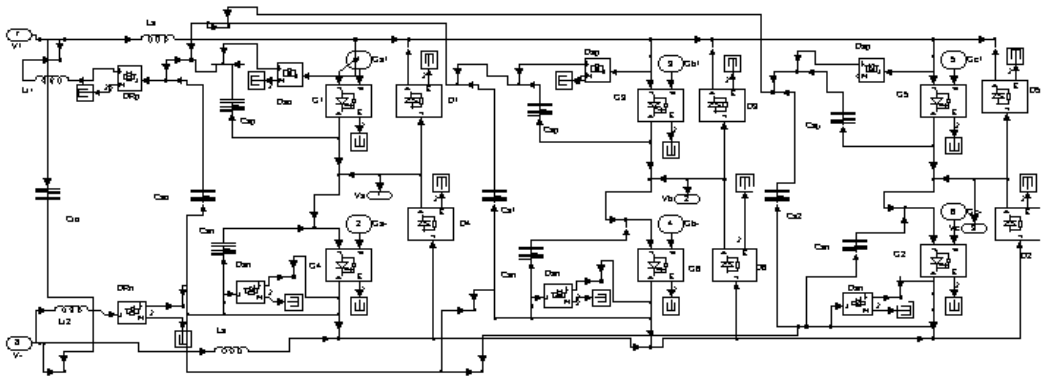


Fig 9 PSSS circuit

The diagram shown in Fig 10 is the filter used is LC. By using this filter harmonics are reduced.

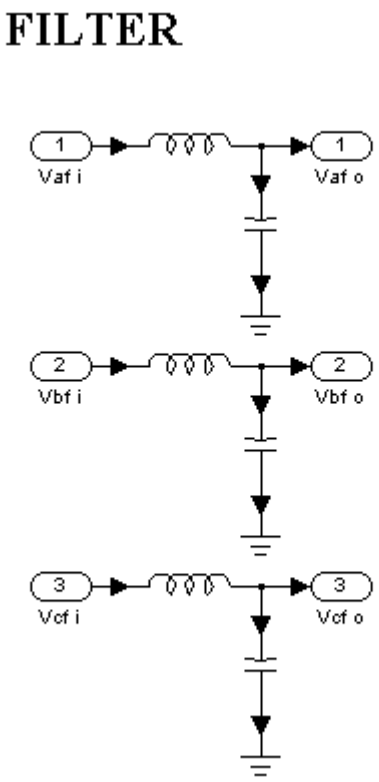
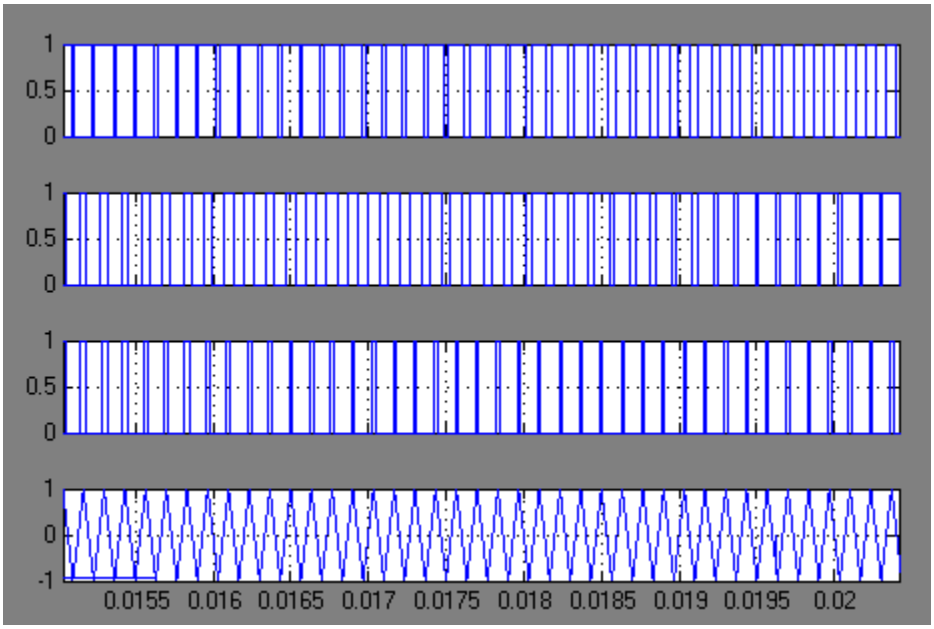


Fig 10 filter

TABLE 1: CIRCUIT DETAILS

G1, G2, G3, G4, G5, G6	Mosfets
D1, D2, D3, D4, D5, D6	Diodes
Ls	1uH
Cs	1uF
Switching frequency	2.5KHz
Supply voltage	330v

SIMULATION RESULTS



↑Voltage
In volts Time in sec →

Fig 11 PWM pulse generated

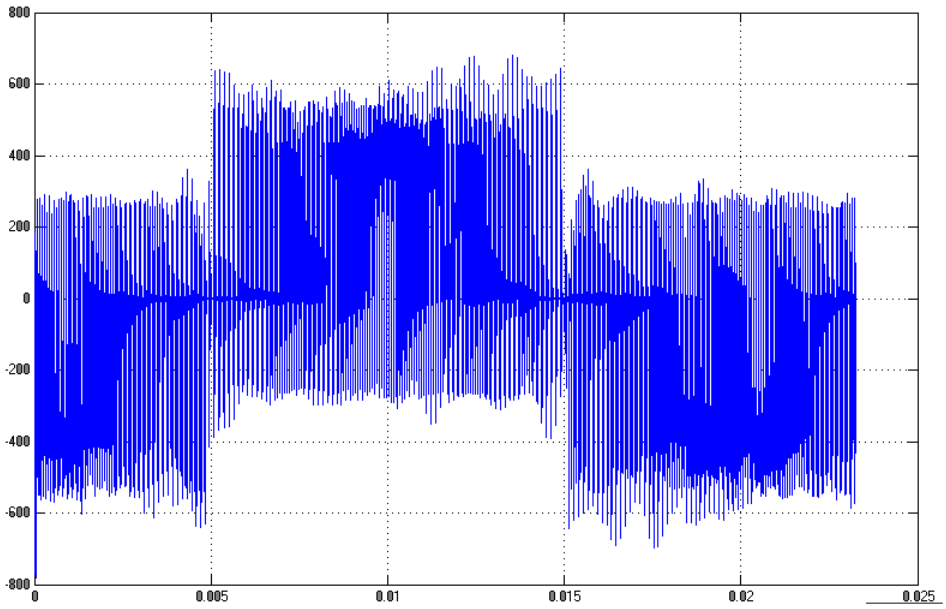


Fig 12 PSSS inverter output

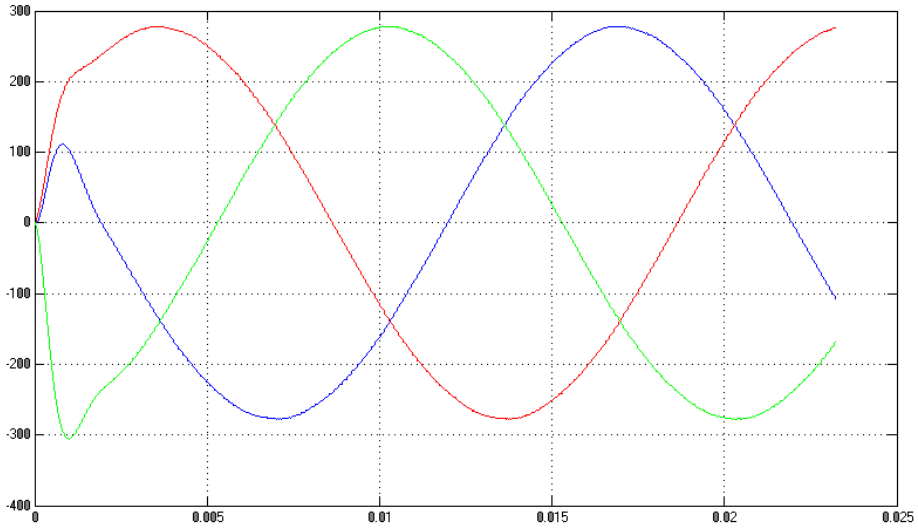


Fig 13 Three phase inverter output voltage

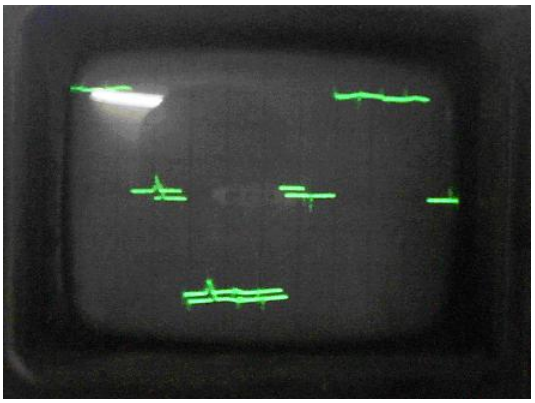


Fig 14 Line voltage between Phase A and Phase B

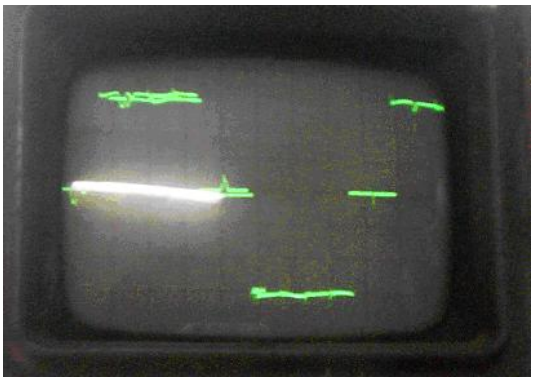


Fig 15 Line voltage between Phase B and Phase C

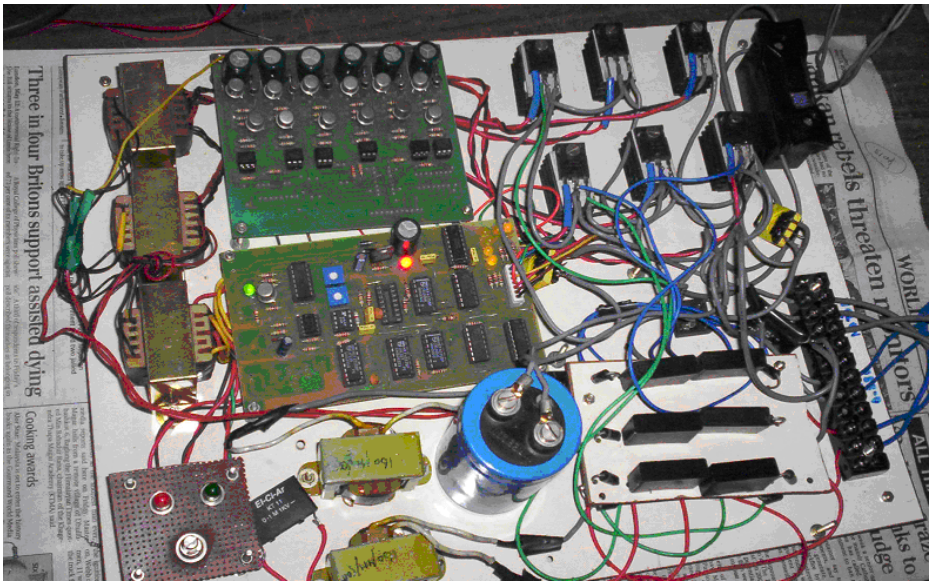


Fig 16 Photocopy of the Kit

IV. CONCLUSION

The presented PSSS circuit has the following features:

- employs only passive components;
- requires no additional control;
- allows any PWM schemes;
- eliminates dc bus plane layout;
- utilizes stray inductance;
- reduces dv/dt and di/dt;
- lowers total inverter cost and improves reliability.

The PSSS provides a viable alternative to existing soft-switching inverters. The PSSS is especially suited for silicon carbide (SiC) device inverters because SiC diodes have no or minimal reverse recovery current, which reduces dv/dt uniformly at both turn-on and turn-off to further soften the switching.

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