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Design of a 2.4 GHz Transmitter Front-End in 0.18um CMOS Technology for Wireless Application

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Abstract

In this paper a 2.4GHz transmitter front-end for wireless sensor applications, in a 0.18µm CMOS technology is presented. The RF components of front-end Transmitter includes two low pass filter, two up-conversion mixer and power amplifier for improving the linearity and less DC current consumption. This parameters employed direct digital modulation scheme to reduce the power consumption of the sensor nodes. The life time of the wireless sensor networks increased by observing the device reliability constraints at low power. The measured results for the 2.4GHz transmitter front-end are 8.478dB of power conversion gain, 3dBm of 1 dB compression output, and the output third-order intercept point (OIP3) of 13.8 dBm, while consuming only 6mA from the supply voltage of 1.8 V

Keywords— Transmitter front-end, low pass filter, mixer, power amplifier and wireless sensor network applications.

I. INTRODUCTION

WLAN (wireless local area networks) is one of the data communication systems that reduces the need for wired connections and makes new applications possible. Mobile WLAN users can access information and network resources as they attend meetings, collaborate with other users, or move to other campus locations. But the benefits of WLANs extend beyond user mobility and productivity to enable portable LANs. With WLANs, the network itself is movable. The benefits of WLANs are range/coverage, throughput, multipath effect, reliability, interoperability with wired infrastructure, simplicity/ease of use, security, scalability, battery life for mobile platforms and safety.

Nowadays there are more applications need the WLANs. For long range applications, the high data-rate is focused in the wireless networking. Recently, the IEEE 802.15.4 ZigBee concept is highly emerging as compare to the wireless

personal area networking (WPAN).Generally, the 868/915 MHz frequency band is used in Europe and USA countries; but the 2.4 GHz band is used in all over the world. So it is known as 2.4 GHz ISM band (Industrial, Scientific and medical).

There are so many applications for this low date rate standard such as industrial and commercial, home automation, personal health care, and toys and game that should be able to operate via WLANs. This 2.4GHz transmitter is not only focused on the high data-rate. It also depends upon low power constraints. With the motivation of low power, high linearity to fulfil the demand of new trend, this paper presents a 2.4 GHz transmitter front-end for wireless sensor network applications based on 0.18µm CMOS technology. Section II describes the transmitter architecture from a system point of view. Section III presents the detailed circuit design, and the simulation results are given in Section IV. Finally Section V gives the overall conclusions.

II. TRANSMITTER ARCHITECTURE

There are several front-end transmitters focused on the Zero-IF and the dual-conversion architectures. The proposed transmitter front-end architecture is shown in Fig. 1, consisting of low pass filters (LPF), I/Q up-conversion single-balanced mixers and a power amplifier (PA). In this architecture, power amplifier is adopted following the single-balanced mixers. The adoption of a power amplifier eliminates the requirement of balun circuit that is differenti al circuitry to reduce power consumption. It shows in Fig. 1, one of the differential up-conversion mixer output signals is connected to the power amplifier while the second one is connected to the AC ground. From the simulation we have realize that by using this approach the gain of overall RF transmitter front-end is reduced by 3 dB while taking fully advantages of the differential circuitry.

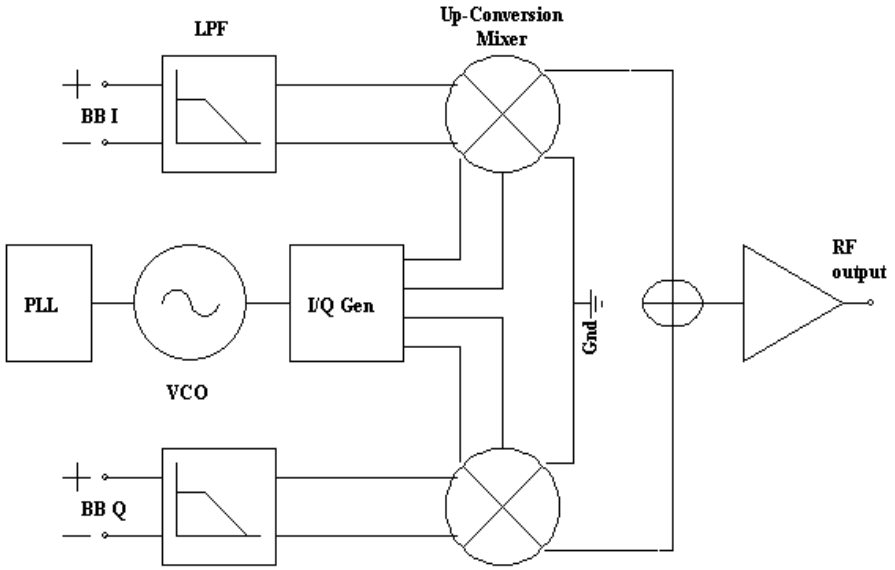

Figure 1. Transmitter architecture

III. CIRCUIT DESIGN A. *LOW PASS-FILTER*:

The proposed second order low pass OTA-C filter is shown in Figure 2. In the structure the OTA has two pairs of
differential input and two outputs with the same current direction. The transfer function of the filter can be derived as

$$H(s) = \frac{Iout(s)}{Iin(s)} = \frac{1}{t1t2s^2 + t2s + 1} \qquad (1)$$

Where,

$$t_1 = \frac{C_1}{g_m} \text{ and } \quad t_2 = \frac{C_2}{g_m}$$

The pole frequency w0 and the selectivity factor Q are given by

$$w_0 = \frac{g_m}{\sqrt{C_1 C_2}} \qquad (2)$$

$$Q = \sqrt{C_2/C_1} \qquad (3)$$

The method is more suitable for low-Q design, as large Q may result in large spread in capacitances. Particularly, when Q=1, we can have C1=C2=C, convenient for practical implementation. In this case, w0 can be easily controlled by a capacitor array C which can further enhance the tuning range. From equations (2) and (3), design can be easily done. For any chosen value of gm, C1 and C2 can be determined from the equations.

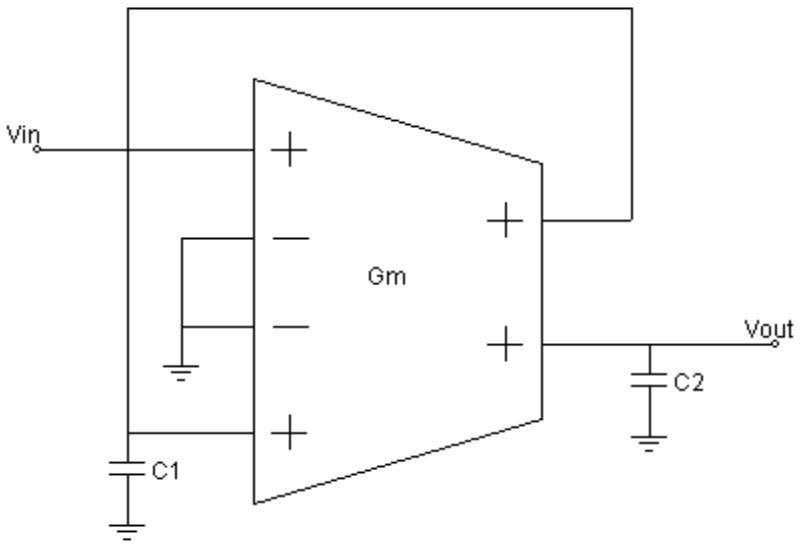

Figure 2 Second-order OTA-C filter using a single current-mode multiple-output OTA

The simulation of the current-mode filter in Figure 2 requires a multiple-input OTA with two output currents both flowing out of the OTA. To benefit from its advantages of linearity and tunability, we use the cross-coupled type OTA in the filter simulation, shown in Figure 3. The OTA contains two cross-coupled CMOS transistor pairs, in which one pair is biased with an additional voltage source of low output impedance. The input stage consists of source - coupled transistors pairs M1-M4 and M5-M8 and biased source coupled transistor pairs M2-M3 and M6-M7. Using the standard square-law model for MOS transistors in their saturation region, output current Ioutj can be expressed as T he transconductance of the proposed OTA is linear and tunable by varying the bias voltage Vb.

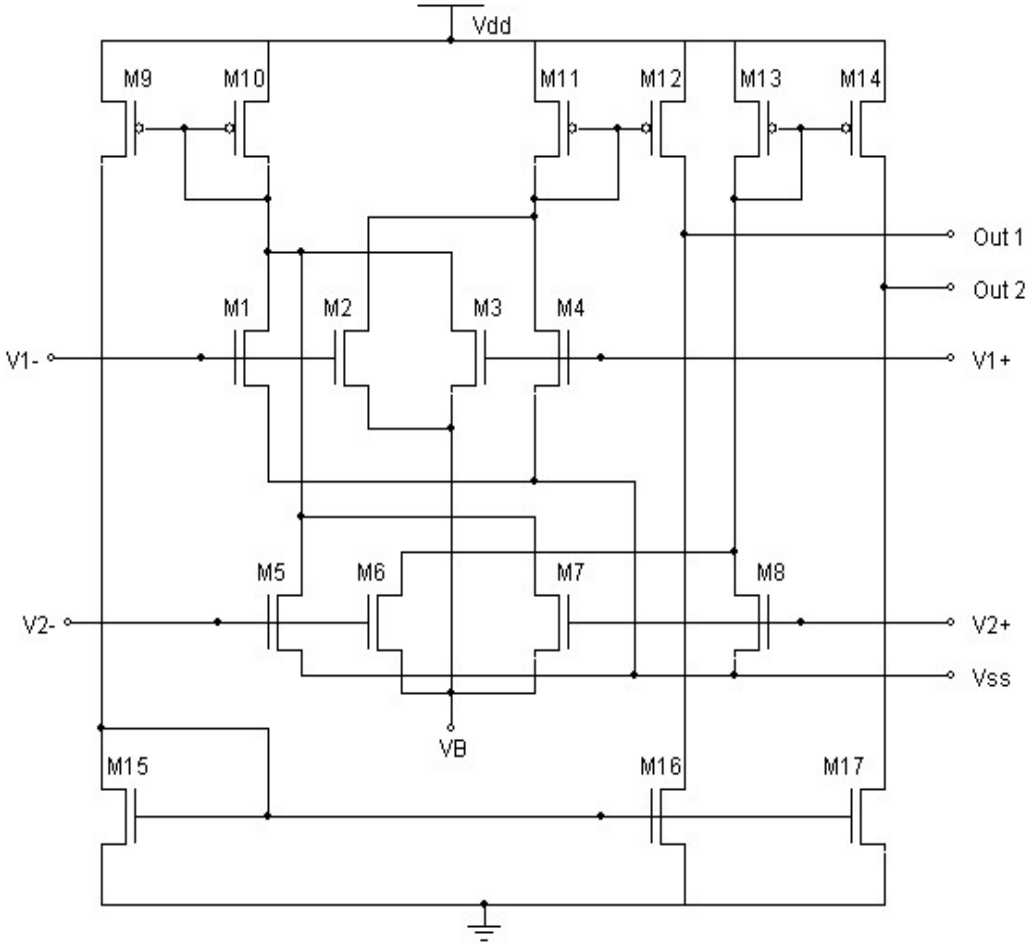

Figure 3. Transistor-level implementation of multiple input OTA

B. *SINGLE-BALANCED UP-CONVERSION MIXER WITH LO CANCELLER*

The up-conversion mixer should be able to operate at low supply voltage and low power consumption. The single balanced configuration exhibits less power dissipation than the double-balanced counterpart, but the LO feed-through occurred at the

intermediate frequency (IF) port. The proposed single-balanced topology with LO cancellation is shown in Figure 4. As a solution to the LO feed-through problem of the single-balanced mixer, an extra LC circuit which is a band pass filter (BPF), is implemented between the differential pair of IF output. Because multichannel LO signals are generated at IF output, the BPF is used for covering from 2.3 to 2.5 GHz. There are two parts in LO signal, one is for the gain the other is for the switch ing. The gain part of LO signal injected in the IF output is too larger to suppress with active low pass filter. Therefore, the LC passive circuit provides a short circuit path to the differential LO signal, multiple LO signals with opposite phases a re cancelled out each other. The third order Chebyshev type BPF from a low pass filter prototype is designed for the LO canceller as shown in Fig. 4. The signal feeding into the receiver from the antenna is mostly single- ended but the baseband signal is usually differential, therefore single-to-differential conversion is easily resolved using this single-balanced mixer.

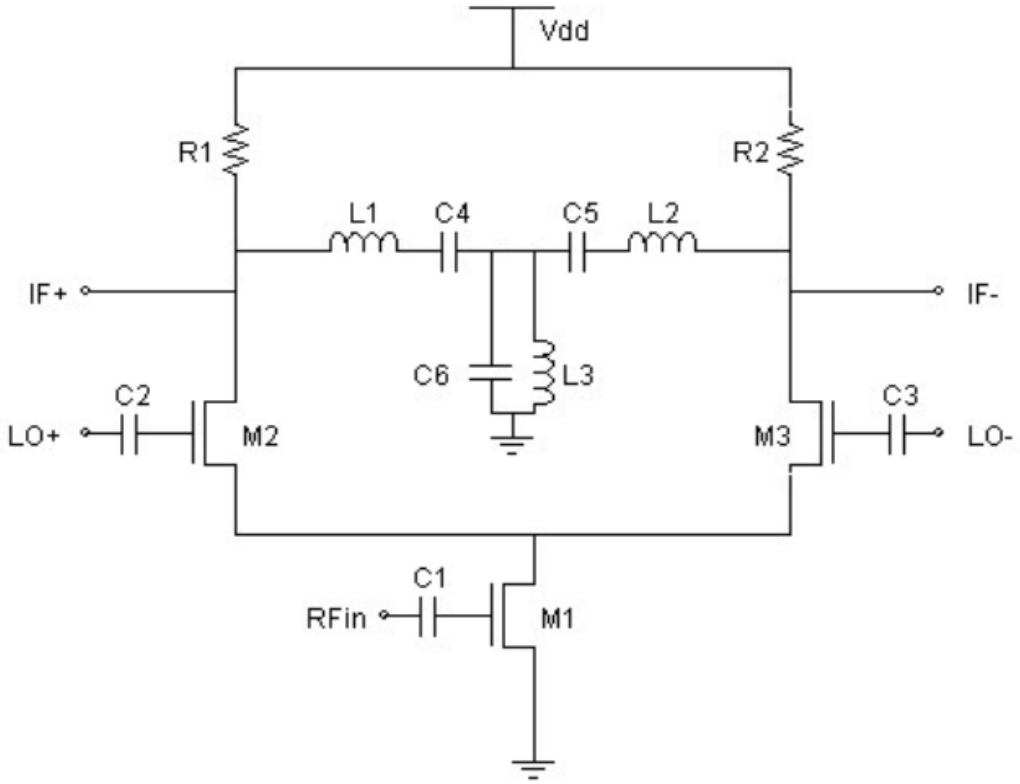

Fig. 4.The single-balanced mixer with LO cancellation

The single-balanced configuration exhibits less power dissipation than the double-balanced counterpart, but the LO feed- through occurred at the intermediate frequency (IF) port as the following Equation. (4).

$$i_0 = i_{01} - i_{02} = \frac{4I_{D1}}{\pi} cos\omega_{LO} t + \frac{2}{\pi} g_m v_{RF}(\omega_{LO} - \omega_{RF})t + \frac{2}{\pi} g_m v_{RF}(\omega_{LO} + \omega_{RF})t + .. \quad (4)$$

To operate the RF section and the time-variant section in saturation region, the bias voltage on M2 and M3,

$$V_{IF} >> V_{RF} - V_{TH1} - V_{GS\_M2,M3} - V_{TH2} \quad (5)$$

The time-variant section affects the mixer noise performance dependent on the size of M2 and M3. C. *POWER AMPLIFIER*:

The power amplifier (PA) driver is a class-A single-stage amplifier, as shown in Fig. 5. The driver uses a cascode structure to provide the isolation from the PA driver output to its input, and to maintain the stability. The driver uses on- chip spiral inductors as its load which also provides the dc current path. For a driver delivering several milliwatts low- Q on-chip inductors can be used. The driver is inductively degenerated to improve its linearity. The PA driver delivers a nominal power of 0 dBm to 50Ω Ql load and reaches saturation at 5 dBm. An off-chip PA with 50Ω Ql input can be used to further boost the driver output to the required power of 16 dBm.

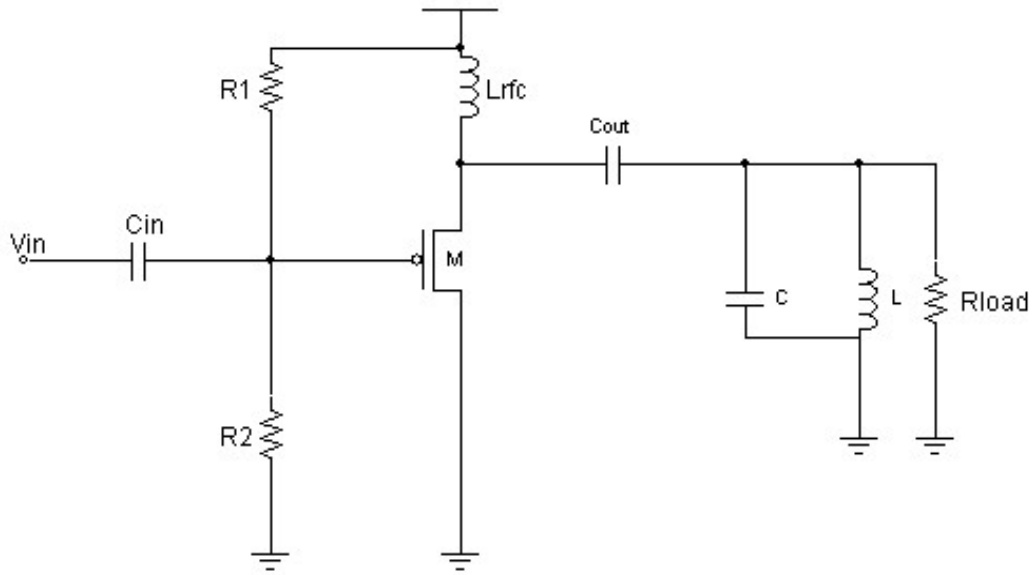

Figure 5. Class-A Power Amplifier

The bias current needed to assurance of class-A operation is given in the below equation (6).

$$I_D = i_{d,peak} = \frac{f_t\sqrt{2p_{in}}}{f_0\sqrt{R_s}} \quad (6)$$

where Rs is the source resistance of the amplifier, ft the cut- off frequency of input transistor, fo the operating frequency.

IV. SIMULATION RESULTS

The output response of the 2nd order Low pass filter is shown in figure 6. In this the cut-off frequency of the Low pass filter is 1.5MHz. The total power consumption is 5.782mW.

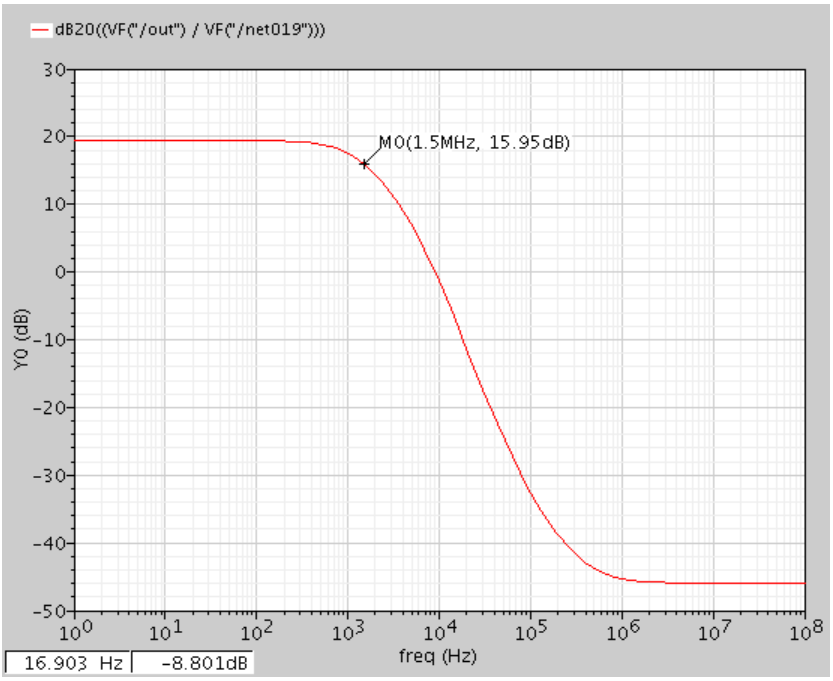

Figure 6. Output response of the 2nd order Low-Pass Filter

The waveform of the single balanced mixer with LO cancellation is shown in figure 7. The 4.7455nW power consumption and 9µA current flow are required for this mixer.

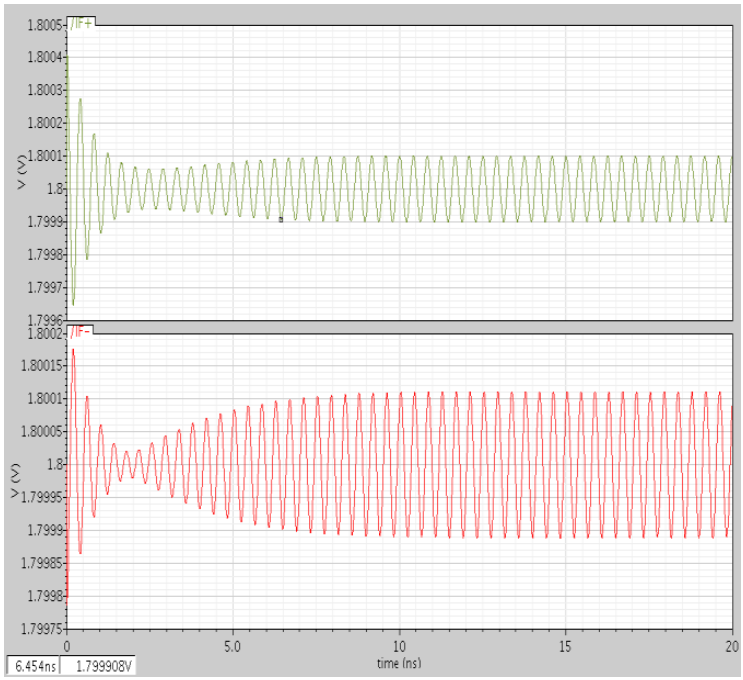

Figure 7 Waveform of the Single Balanced Mixer with LO Cancellation

The output waveform of the Class-A Power amplifier is shown in the below figure 8. The output power is 1.078W. In this, it amplifies the voltage from 20mV to 121.54mV. The current flow in the node is 557mA.

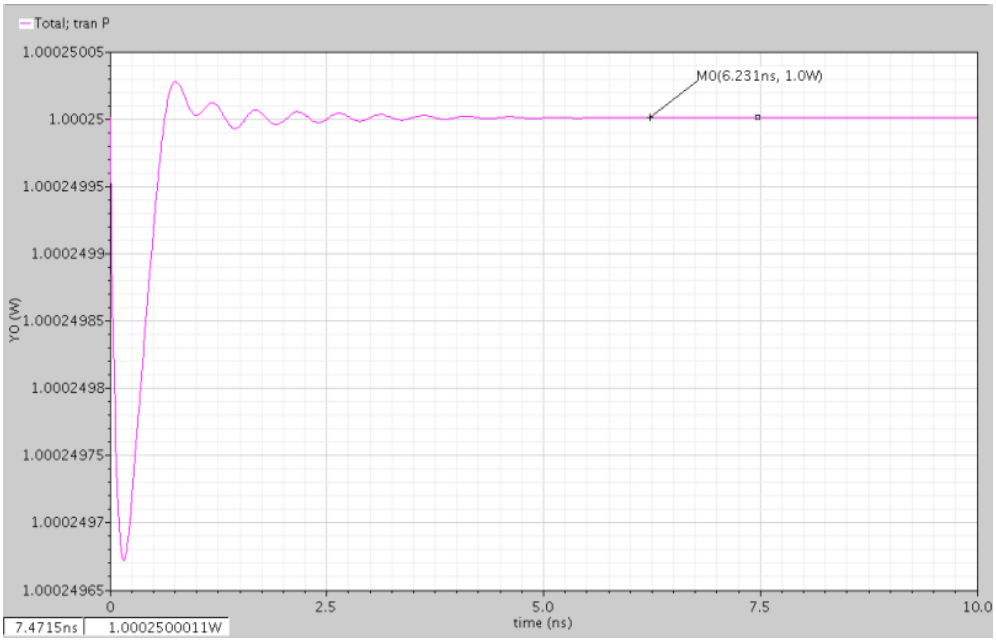

Figure 8. Waveform of Class-A Power Amplifier

Finally the Figure 9 shows the output response of the RF transmitter front-end. It totally consumes only 8.1mW. The table I denotes the measurement parameter of the transmitter front-end.

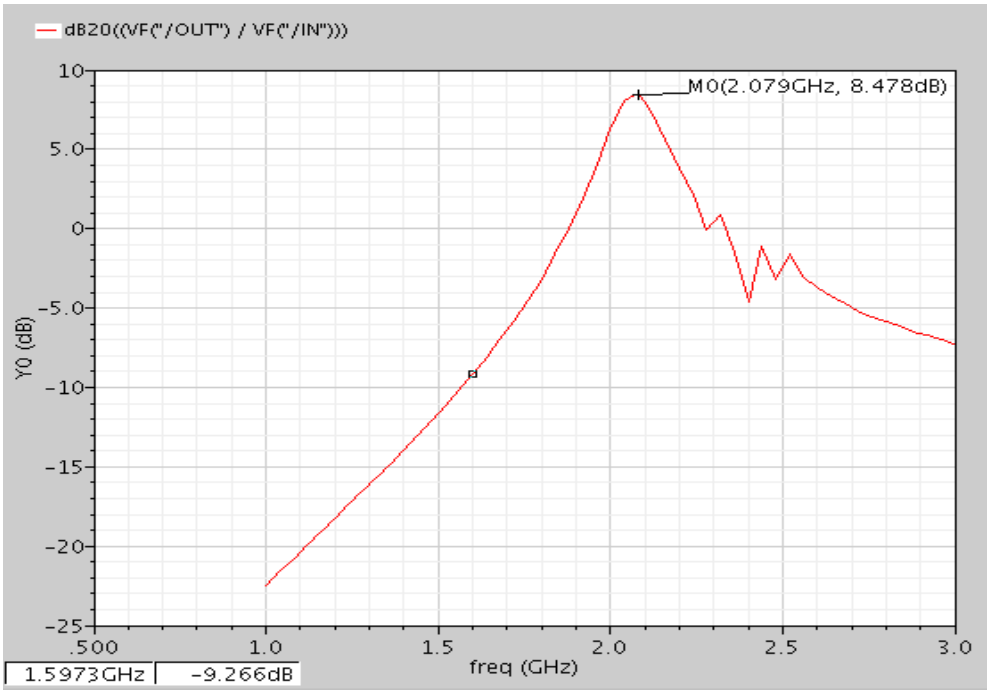

Figure 9. Output response of RF transmitter front-end design

TABLE-1 SUMMARY OF TRANSMITTER FRONT-END SPECIFICATIONS

PARAMETERS	RF TRANSMITTER FRONT-END
Gain [dBm]	8.478
OP-1 [dBm]	3
OIP3 [dBm]	13.8

V. CONCLUSIONS

The 2.4GHz transmitter front-end in 0.18µmCMOS for wireless sensor network applications is presented in this paper. The direct reduces the power consumption. The total power consumption of this architecture is 8.1mW. A programmable gain SSB mixer suitable for low-supply operation is proposed. With the power amplifier, high linearity under low power consumption is archived by using a current mode operational transconductance amplifier. The RF transmitter front-end dissipates 1.8 mA from 1.8 V supply.

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