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Review and Performance Evaluation of Multiplexers Using Different Logic Styles for Sub-Micron Technologies

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Abstract

Multiplexers play a major role in the design and implementation of any logic function. Logic styles play a vital role in determining their performance metrics such as power, propagation delay, power-delay product and output drive capability. In this paper a study of effect of logic styles such as DPL, LEAP, CPL, EEPL, SRPL, CMOS and PTL in the construction of 2:1 multiplexer is done for a much scaled down process technology of 32nm. The simulations are carried out using TSPICE and from the results, it is inferred that modifications in the existing logic styles is necessary to cope up with the changing transistor dimensions. Also, the paper suggests two possible modifications that can be done in CPL and EEPL and proposes one multiplexer that achieve good performance metrics. From the results it is evident that, CPL is found to be 37.8% faster than its modified counterpart, but when power is concerned, the latter is 97% power efficient than the former. Modified EEPL is 72.67% power efficient and 11.5% faster than LEAP. Modified EEPL is 4.4% power efficient then CMOS and modified CPL is 6.72% faster than CMOS. The proposed multiplexer is 73.44% faster and smaller than modified EEPL even though the latter is 77.16% power efficient.

Keywords— low power; logic style; multiplexer;

I. INTRODUCTION

The increasing popularity of portable devices has led to the demand in the development of low power VLSI circuits. Now-a-days, many portable devices exhibit

more features, support numerous add-ons and applications. This puts forth the need for the designs and techniques that reduce the power consumption and power dissipation of VLSI circuits such as microprocessors, digital signal processors, etc. Generally, arithmetic circuits form the basic functional blocks of many of these units. The basic logic gates, adders and multiplexers are used to construct the arithmetic circuits. Among these multiplexers play an important role in the implementation of adders, decoders and any combinational login function for that matter. Thus the design of power efficient and faster multiplexer is very important.

To aid this development, various logic styles that can be used to construct a multiplexer are explored in this paper. Previously, similar analysis was done long ago for 500 nanometer process technology [1]. Here, analysis is carried on to evaluate whether the same logic styles perform up to the expectation for a much scaled down technology of 32 nano meter. Reduction in process technology always features reduction in the transistor sizes and thereby the entire device

size. But at these sizes sub-threshold and gate leakage are the predominant factors that determine the power dissipation and power consumption of the circuits. Hence, few modifications must necessarily be performed in the existing ones to suit the new transistor dimensions, the same is done and discussed in this paper along with a new proposed multiplexer.

In section II, the impact of different logic styles in the design and implementation of 2 : 1 multiplexers and proposed multiplexer are discussed. Section III puts forth the experimental setup and simulation results. Finally, conclusions are drawn in section IV.

II. DESIGN OF MULTIPLEXERS

The size, power and speed of combinational circuits designed by a particular logic style is determined by the number of transistors, transistor sizing, inter and intra cell capacitances, switching activity and node capacitances. These characteristics do vary from one logic style to another and this necessitates the choice of the best to suit the circuit performance. There are two basic logic styles namely, static and dynamic logic styles. Unlike static dynamic logic styles use clock and operate in two phases called pre-charge and an evaluation phase. Dynamic gates are best suited for high speed operations but the presence of large clock loads increase the power dissipation and make it an unsuitable candidate for low power applications. In this paper different static logic styles are analyzed and their performances are evaluated.

A. CMOS Logic Style

Complementary CMOS logic styles employ a PMOS pull-up network and an NMOS pull-down network to implement any logic function. Design of basic logic gates is simple and that of complex gates like XOR and multiplexer are complex but efficient. CMOS circuits are robust against voltage and transistor scaling[3]. They render reliable operation even at reduced supply voltages and reduced transistor sizes due to the use of complementary transistor pairs. The input signals are applied to the transistor gates only and hence characterization of logic cells is much easier. The

CMOS multiplexer in Fig.1 consists of four PMOS and NMOS transistors apart from two inverters used to generate the complementary inputs. Though the CMOS multiplexer is power efficient and faster, its output drive capability is limited due to the presence of series transistors at the output.

B. ***Pass Transistor Logic Style (PTL)***

In pass transistor logic style input signal are connected to the sources of transistors instead of power lines[6]. This is the major difference between CMOS and PTL logic styles. Any one transistor network that is, either PMOS or NMOS network can be used to implement any logic function. NMOS transistor passes a good logic 0 and a bad logic 1 and PMOS vice versa and so full swing cannot be obtained. In order to achieve swing restoration, two MOS networks are added. Also, Pass transistor logic style requires complementary inputs. Thus the transistor count also increases and this style can no longer boast of reduced transistor count as an advantage. The pass transistor multiplexer in Fig.2 is sensitive to voltage scaling and transistor sizing . Thus reliable operation is not achieved at low voltages and small transistor sizes.

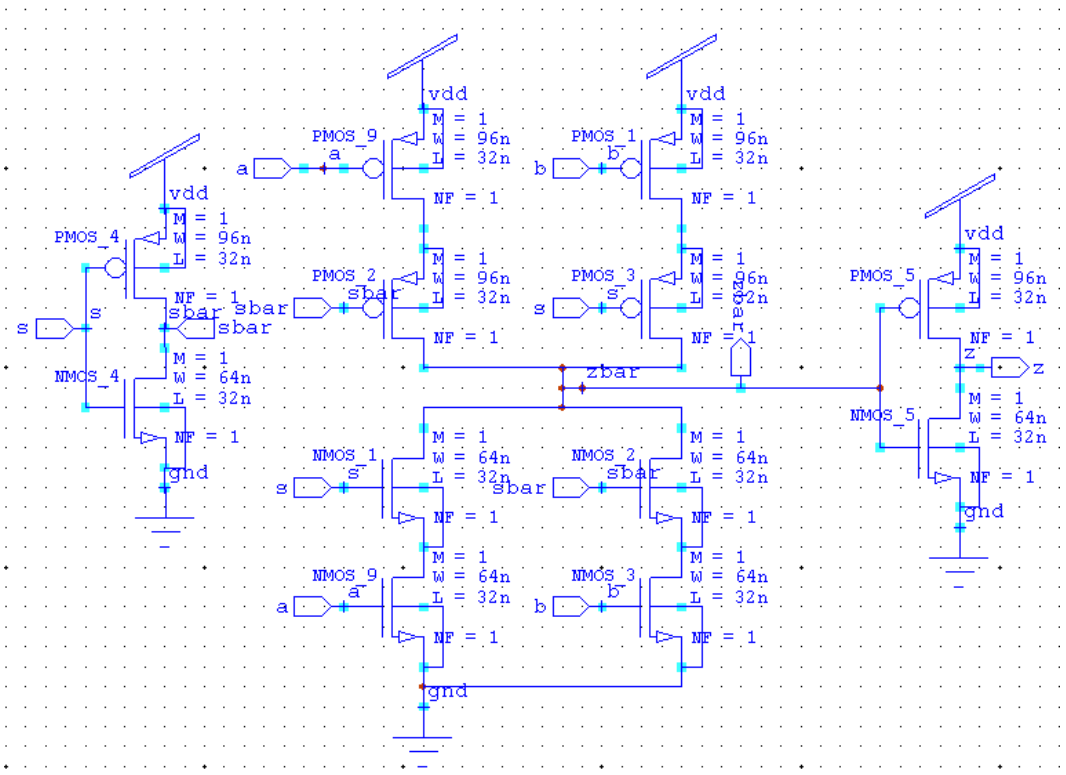

Fig.1 CMOS 2:1 multiplexer

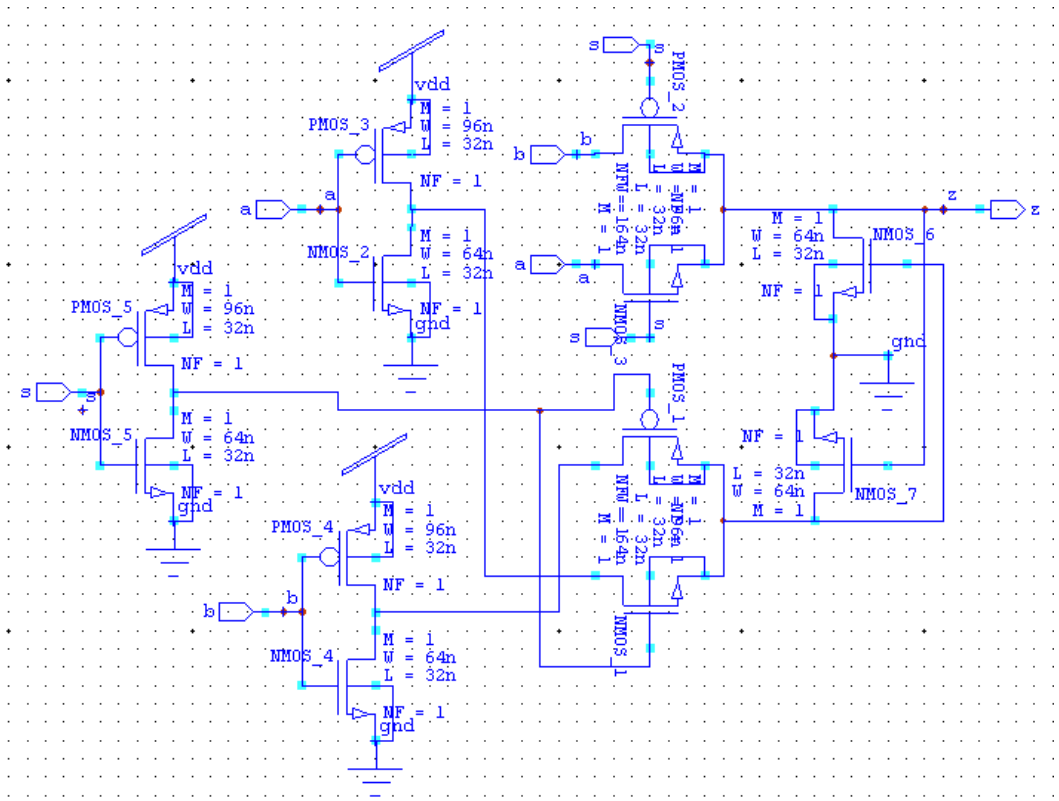

Fig.2. Pass Transistor Logic 2:1 multiplexer

C. ***Complementary Pass Transistor Logic (CPL)***

A CPL logic style uses both NMOS and PMOS transistors to implement a logic function [2],[7]. This logic style can be used to design complex logic gates like XOR and XNOR gates efficiently. The CPL multiplexer in Fig.3 has NMOS gates to implement the logic function and cross coupled PMOS transistors as pull-up network. This circuit features high transistor count, small input loads and good output driving capability due to the presence of inverters.

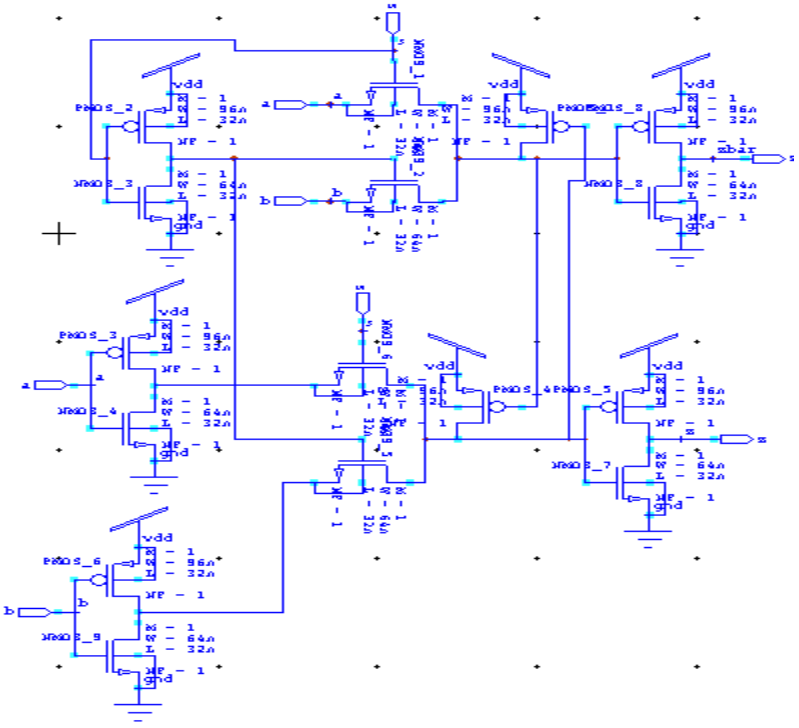

Fig. 3 CPL 2:1 multiplexer

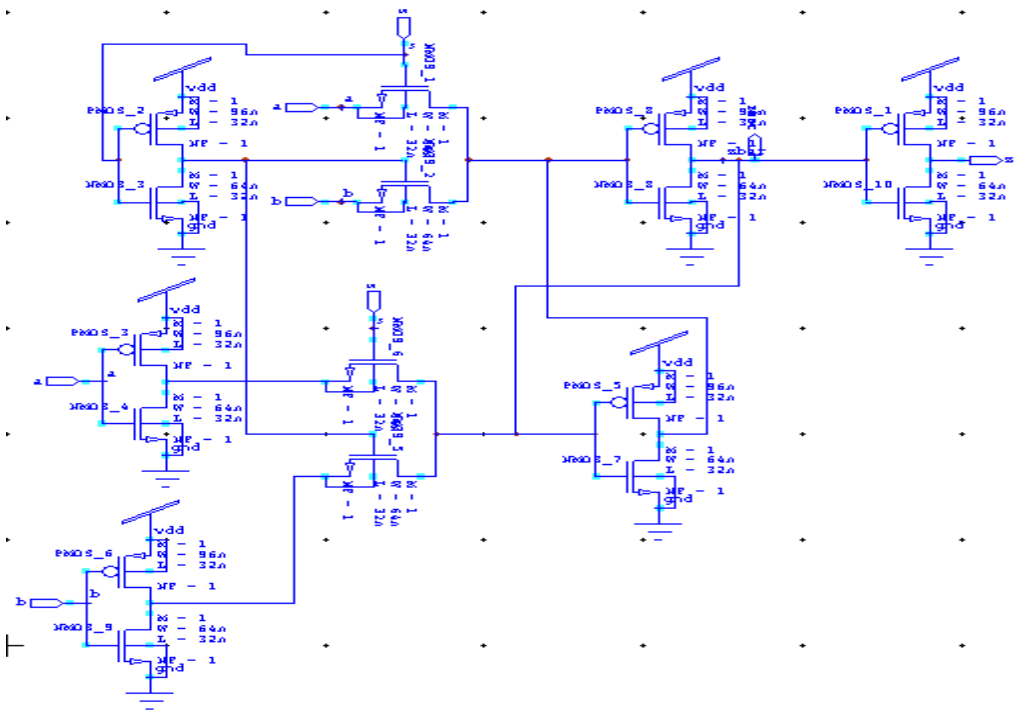

Fig.4 SRPL 2:1 multiplexer

D. ***Swing Restored Pass Transistor Logic (SRPL)***

The SRPL gate is derived from the CPL gate. Here the cross coupled PMOS pull-up network is removed. Instead, the inverter outputs are cross coupled as a step to improve the output driving capability and ensure output swing restoration. With reduced transistor sizing poor output driving capability is witnessed along with slow switching for the SRPL[8] gate in Fig.4. For reduced transistor sizing this multiplexer is sensitive and exhibits acceptable performance only when there is low output load.

E. ***Double Pass Transistor Logic (DPL)***

In this logic style, both NMOs and PMOS logic networks are used in parallel. The DPL multiplexer[4],[9],]10] in Fig.5 is found to possess equal number of NMOS and PMOS transistors. Presence of more number of PMOS transistors and high transistor count has led to increased power consumption at a reduced transistor sizes. There is no need for level restoration as there is full output swing due to both NMOS and PMOS transistors in the circuit.

F. ***Single – Rail Pass Transistor Logic (LEAP)***

In Leap multiplexer in Fig. 6, a single-rail of NMOS transistors form the logic network[5] . The swing restoration part consists of a feedback pull-up PMOS transistor. The pull-up in this swing restoration circuitry is slower compared to its differential part in CPL and hence output switching is slower comparatively. This is evident form the increase in propagation delay.

G. ***Energy Economised Pass Transistor Logic (EEPL)***

The sources of the PMOS pull-up transistor of the CPL multiplexer are connected to the complementary output signal and not to the supply rail Vdd in this Energy Economised Pass Transistor Logic multiplexer[11] shown in Fig. 7. This logic style has the advantage of producing average lower power consumption compared to the CPL gate but, as far as delay is concerned the latter is better than the former.

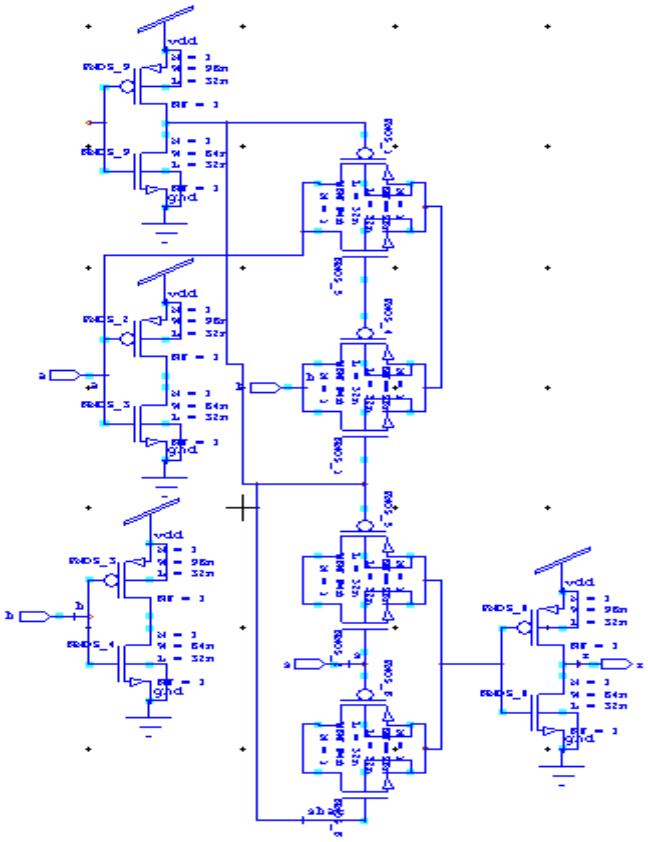

Fig.5. DPL 2:1 multiplexer

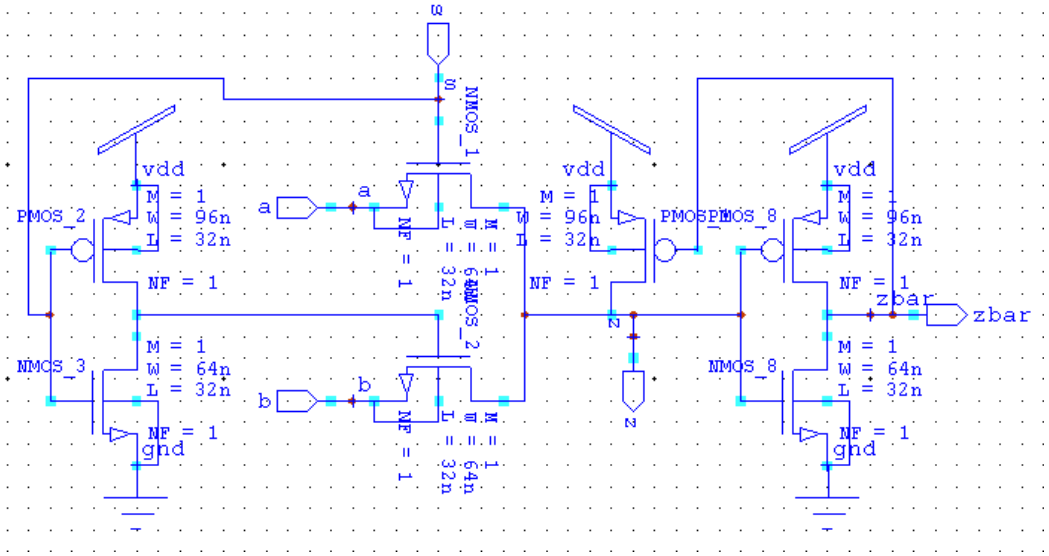

Fig.6 LEAP 2:1 multiplexer

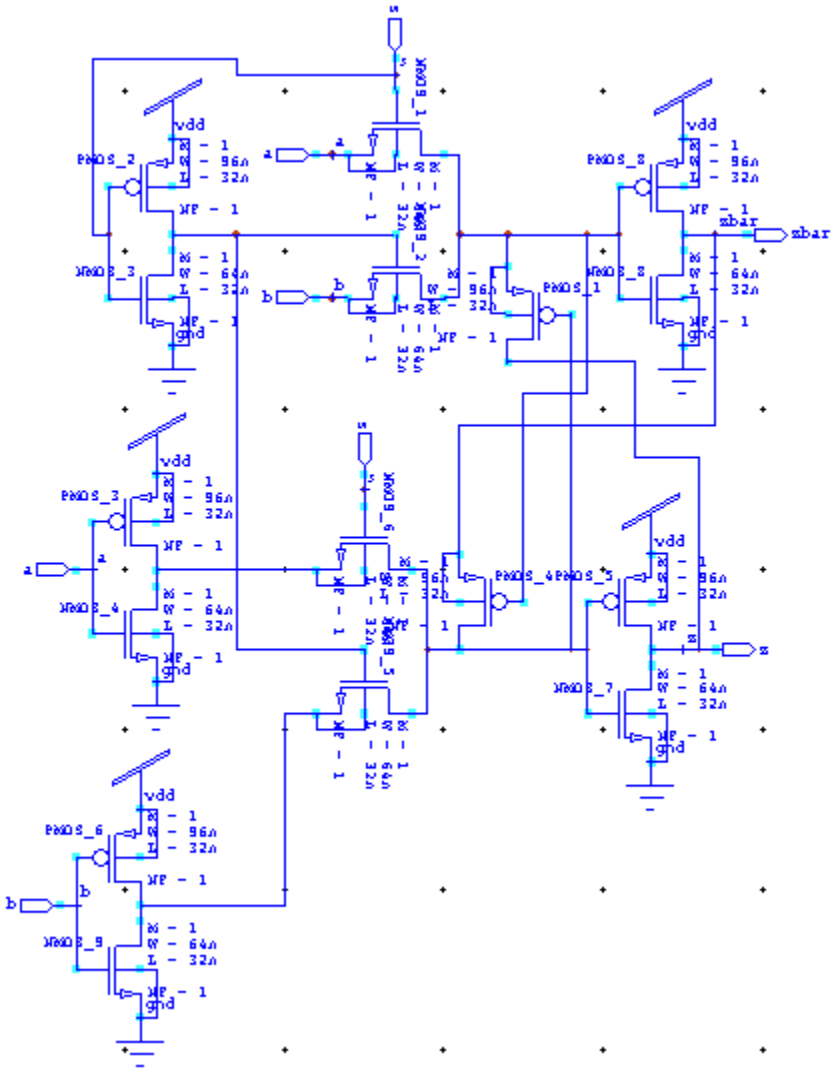

Fig.7 EEPL 2:1 multiplexer

H. ***Modified Logic structures and Proposed Multiplexer***

In CPL multiplexer, there are two PMOS transistors with cross coupled gates at the output as pull-up network which is succeeded by two inverters generating the output and its complement. Most of the arithmetic circuits use either the output or its complement and not both. In such a case, one of the inverters may be removed as in Fig.8 to reduce the transistor count, power dissipation and at the same time maintain the full swing at the output. The delay is also found to be reduced compared to the original CPL gate for the same process technology.

The EEPL multiplexer's modified version in Fig.9 has PMOS pull-up network replacing the cross coupled ones in the original. With pull-up network alone, full output swing could not be achieved. Thus the addition of an inverter at the output of

one of the terminals has decreased delay traded off with power. Then too, only a very small increase in power consumption is witnessed with the inclusion of an inverter.

The proposed multiplexer in Fig.10 is a combination of pass transistor logic and inverter based logic. The logic deciding part is the first level PMOS and NMOS transistors. The input signals are applied to their sources, selection input is applied to their gates and the output is obtained from their combined drains. The circuit does not produce full output voltage swing and at the same time it is not power efficient and faster. To overcome this two inverter stages are added at the output. This preserves the output logic and at the same time produces full output logic swing and comparatively lesser power dissipation. In order to reduce propagation delay, the inverter at the output is sized such that W_n/L_n = 5/1 and W_p/L_p=5/2. This big inverter at the output offers lower resistance and so lesser propagation delay at the little expense of power.

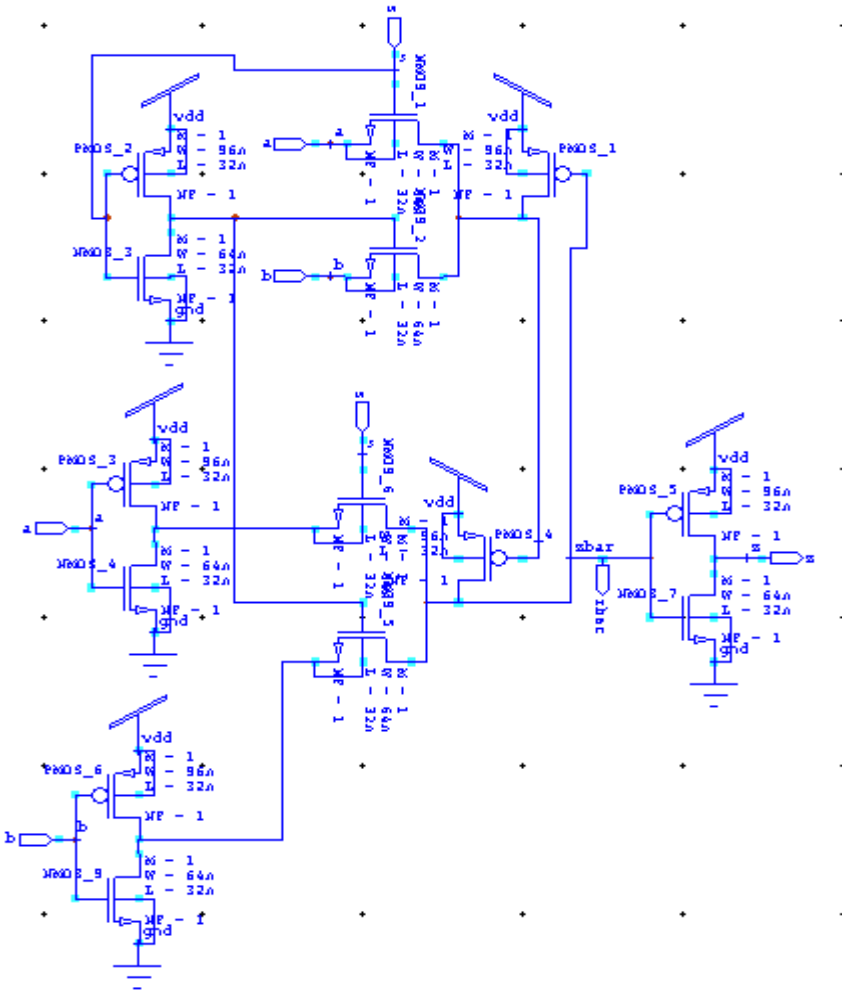

Fig.8 Modified CPL multiplexer

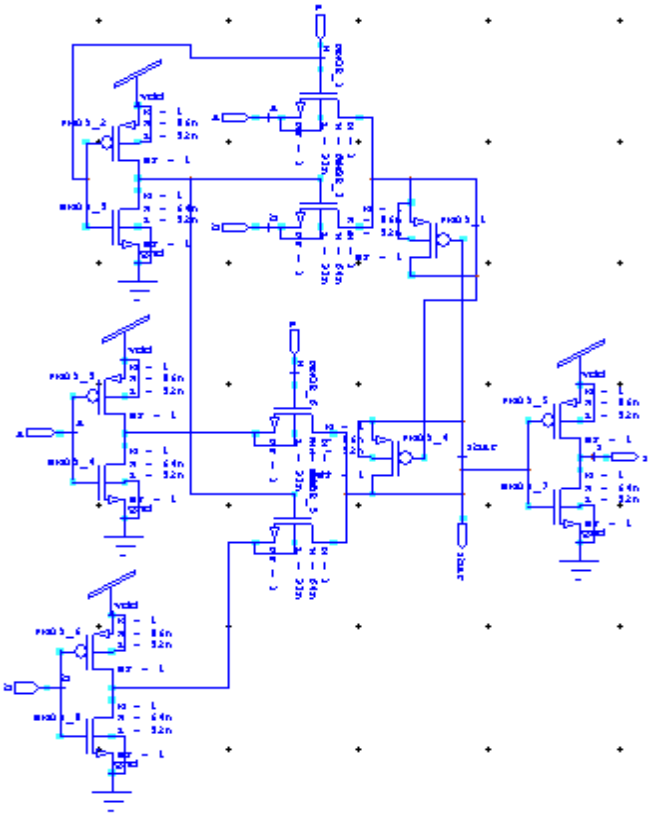

Fig.9 Modified EEPL 2:1 multiplexer

III. EXPERIMENTAL SETUP AND SIMULATION RESULTS

All the circuits mentioned in the paper are simulated and transient analysis is done employing a scaled down process technology of 32nm using TSPICE . The length of both the NMOS and PMOS transistors is chosen to be 32nm. The width of NMOS is twice that of its length and that of PMOS transistor is thrice that of its length. A constant load of one femto farad is used and all the simulation results are obtained for the same input combination with a supply voltage of 1V. The power is measured over a simulation period of 425 nano seconds. The delay is measured between the time when the input amplitude reaches 50% of its peak value and the output reaches 50% of its peak value for both fall transitions.

The power, delay and power delay product of multiplexers implemented using different logic styles are measured and compared in Table.1. The DPL, LEAP, CPL, EEPL, SRPL and PTL multiplexers are compared with their variants of CPL and EEPL. The existing circuits were previously simulated using 500 nm CMOS process and their performances were compared in [1]. For 500 nm process technology, LEAP logic style was found to possess lower power and CPL lower delay than the others. But for a much reduced CMOS process, say, 32 nm variants of CPL and EEPL are found to be power efficient and faster.

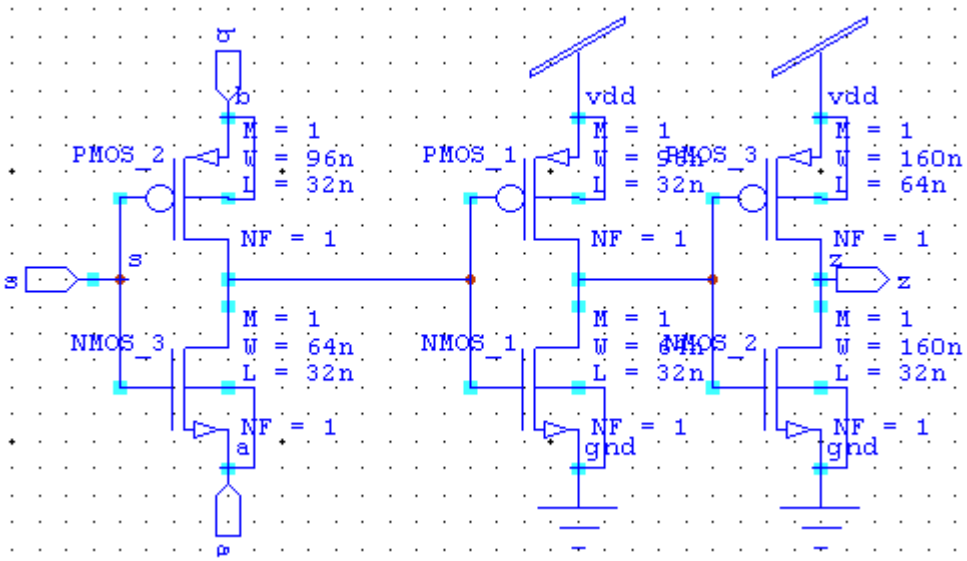

Fig.10 Proposed 2:1 Multiplexer

Table.1 Transistor count, power, delay and power delay product of differnet logic styles.

Logic Style	Number of Transistors	Average Power (W)	Delay (s)	Power Delay Product (J)
DPL	16	9.32×10^{-6}	3.12×10^{-11}	2.91×10^{-16}
LEAP	7	7.83×10^{-7}	2.26×10^{-9}	1.77×10^{-15}
CPL	16	1.2×10^{-5}	3.89×10^{-12}	4.67×10^{-17}
EEPL	16	9.77×10^{-7}	4.36×10^{-8}	4.26×10^{-14}
SRPL	16	8.43×10^{-7}	2.07×10^{-9}	1.75×10^{-15}
CMOS	12	2.24×10^{-7}	6.7×10^{-12}	1.5×10^{-18}
PTL	12	5.49×10^{-6}	2.01×10^{-7}	1.103×10^{-13}
Modified CPL	14	3.6×10^{-7}	6.25×10^{-12}	2.25×10^{-18}
Modified EEPL	14	2.14×10^{-7}	1.6×10^{-11}	6.3×10^{-18}
Proposed Mux	6	9.37×10^{-7}	1.66×10^{-12}	1.56×10^{-18}

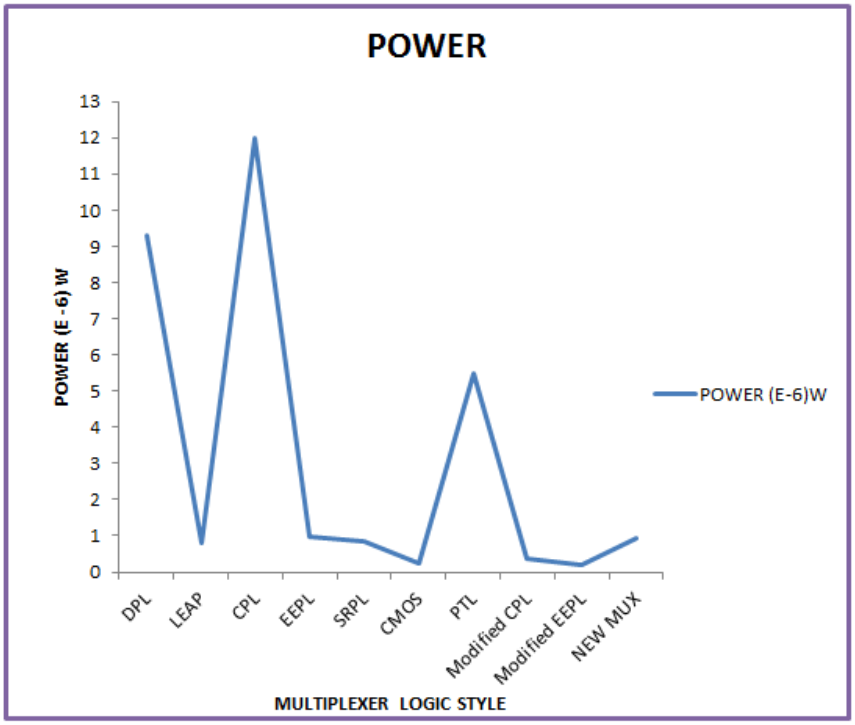

Fig.11 Comparison of powers of different logic styles

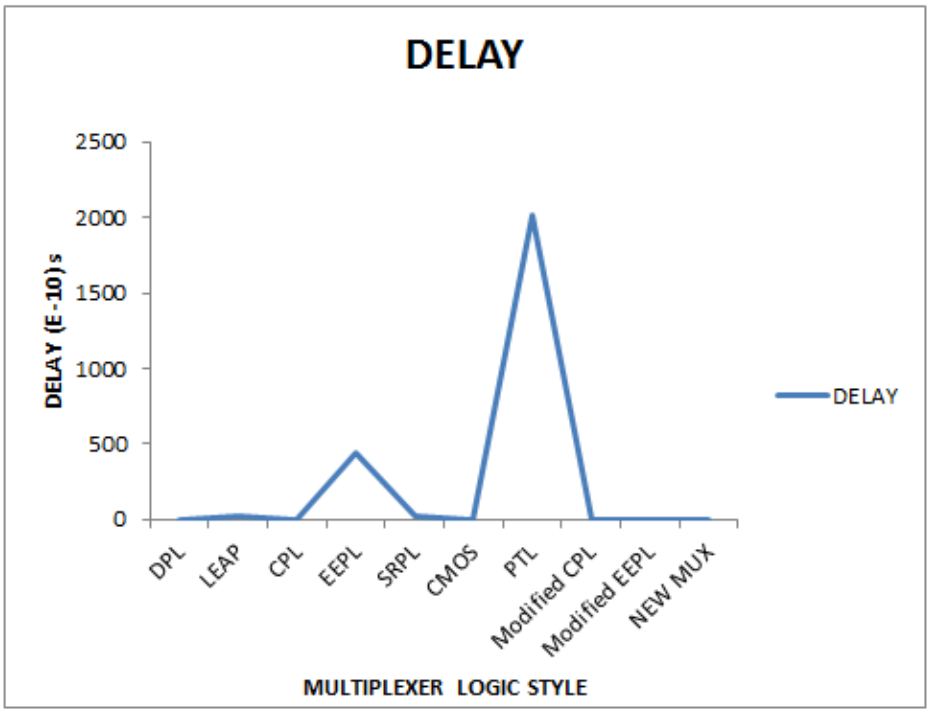

Fig.12 Comparison of delays of different logic styles

Modified EEPL is 72.67% power efficient and 11.5% faster than LEAP. CPL is found to be 37.8% faster than its modified counterpart, but when power is concerned, the latter is 97% power efficient than the former. CMOS logic style has the lowest power delay product. Modified EEPL is 4.4% power efficient then CMOS and modified CPL is 6.72% faster than CMOS. The proposed multiplexer is 73.44% faster than modified EEPL even though the latter is 77.14% power efficient. Also, the power delay product of the proposed multiplexer is comparable to that of CMOS and is superior due to the lower transistor count. A comparison of powers and delays of the different logic styles and the proposed multiplexer are made in Fig.11 and Fig.12 respectively.

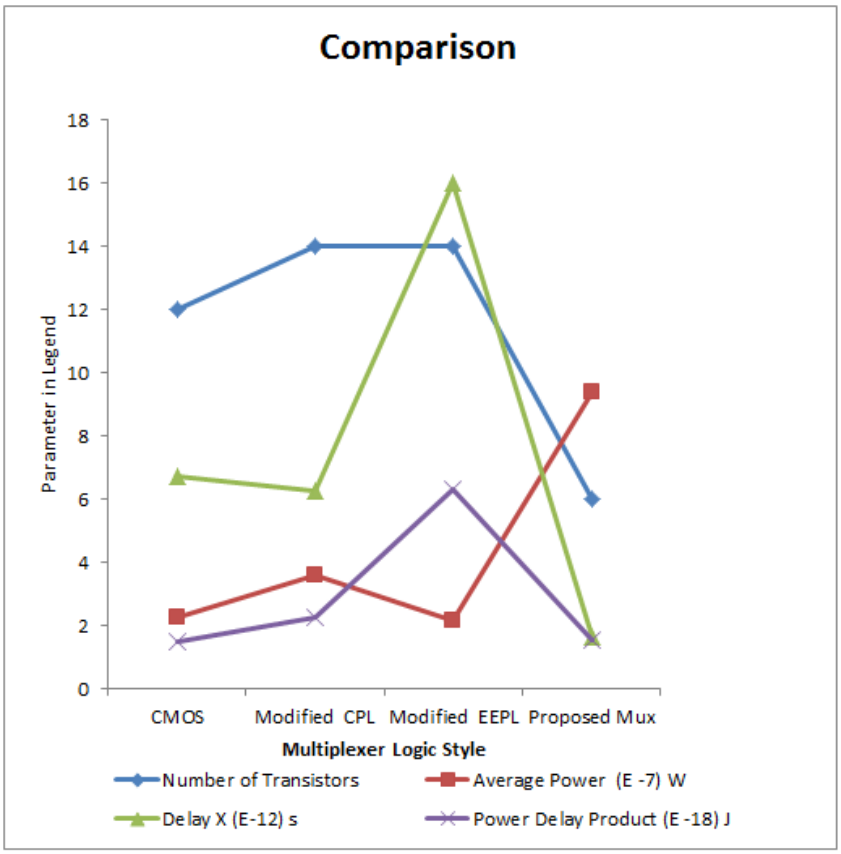

Fig.13. Comparison of CMOS, Modified CPL, Modified EEPL and Proposed Multiplexer.

IV CONCLUSION

In this paper, a study of impact of logic style in the design of combinational circuits like multiplexer was done with the aid of studies conducted earlier. The operation and performance analysis of the multiplexer circuits was done for a much reduced CMOS process technology. Though CMOS logic style is robust performs much better than the other logic styles, alternative CPL and EEPL logic styles and the proposed

multiplexer are found to be superior in the aspects of delay and power respectively Fig.13. Even for 32 nm CMOS technology, proposed multiplexer is found to be faster and modified EEPL power efficient. The study conducted in this paper, helps the designers to choose the best suited multiplexer for particular applications. For low power applications variant of EEPL and for high speed applications the proposed multiplexer can be used. This paper also puts forth the suggestion that with reduced process technology, the proposed multiplexer is best suited as far as delay, power delay product and number of transistors are concerned.

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