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Power Reduction Techniques for Clock-Gated Double Edge-Triggered Flip-Flops

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Abstract

This paper introduces new architecture of low power Double-Edge Triggered Flip-Flops. In the low-power circuit design the energy efficiency from the clock elements plays an important role. Double edge-triggered flip-flops(DETFFs) can maintain the same throughput as single edge-triggered flip-flops (SETFFs) while using only half of the clock frequency. So DETFFs are suitable for low power applications.Another well accepted technique to reduce the power is clock gating. This paper introduces an approach for reducing the power based on clock gating and the modified structure of DETFFs.

Index Terms- Clock gating, DETFF, low power.

I. Introduction

With the integration of today's VLSI circuits power dissipation is gaining much importance. Increasing the performance of mobile devices and maintaining its energy efficiency is very important in integrated circuits (ICs) [1], [2].Designers are working very hard for low power consumption, higher speed, small silicon area and reliability due to the increasing demand of portable electronics. For reducing the complexity of

circuit design, a large proportion of digital circuits are designed to be synchronous circuits.

The most popular synchronous digital circuits that we are using are edge triggered flip-flops. Power spent on the clock-tree or the timing components is a major source of all the power consumption in synchronous VLSI circuits. Flip-flops are widely used in storage elements or in the finite state machine(FSM) as a timing component in the IC. A power-efficient flip-flop provides a great advantage for ICs. Because half of the clock edges in a single edge-triggered flip-flop (SETFF) are inactive, double edge-triggered flip-flops (DETFF) emerged [3], [4] to utilize the other clock edges. With the same clock frequency, a DETFF could double the throughput while operating at half of the clock frequency of the SETFF.

DETFFs have been applied to low-power application-specific integrated circuit (ASIC) designs [5] and also have been employed in high-level synthesis as the primary storage element [6]. The average power in a digital CMOS circuit is given by the following equation:

$$Pavg=pt(CL*Vdd*fclk) + Isc*Vdd + Ileakage*Vdd \quad (1)$$

The above equation represents the three major sources of power dissipation in CMOS VLSI circuits. The first term represents the dynamic or switching power dissipation. The second term indicates the direct path short circuit power dissipation. The third term indicates the leakage power. All these three types of powers are dependent on supply voltage..

To save the power dissipated on the clock tree power-reducing techniques have been added to DETFFs [7]-[8].One of the major techniques is clock gating [9]. Clock-gating technique is used to reduce the power consumed on idle circuitry in the design [10].It can be applied at both circuit-level [11], [12] and behavior-level [13]-[14].This paper discusses the analysis of recent attempts to include clock-gating technique with synchronous double edge-triggered mechanisms. The internal clock controls the gated circuits for a clock–gated system. And it is separated from the global clock during the gated periods. If the internal clock is out of phase with the global clock when the gating signal is de-asserted, then the internal clock signal switches immediately to match the global clock. The internal clock switch is not synchronized with the external clock, which creates an asynchronous data sampling. As a result the output will be changed between clock edges. Each clock-gating transition can create the asynchronous sampling issue.

In this paper four novel low power flip-flops will be presented. The double edge-triggered flip-flop structure is modified to reduce the power consumption. Proposed flip-flops use gating techniques to gain low power operation and show no limitation on clock duty cycle. The analysis in this paper examines the specific conditions that create the asynchronous data sampling.

This paper is organized as follows.Section II describes the basic mechanisms that lead to the asynchronous data sampling with clock-gated DETFF. Then, Section III explains the proposed clock-gated double-edge triggered flip-flop. Section IV contains performance results for the proposed design. Section V ends with conclusion.

II. Asynchronous Data Transitions In Detffs With Clock Gating

This paper uses the following terminology: CLOCK, global clock signal; C_IN, the gated clock signal; CG ,clock-gating control signal; D, input data; and Q, output data. The asynchronous data sampling may cause data miscommunication errors.Clock gating is applied when D = Q. Transitions of D are used to assert the CG signal. C_IN triggers the flip-flop. C_IN maintains its value for the gating mode. C_IN changes after the transition on CLOCK for the non-gating mode. If D changes while C_IN and CLOCK are not equal,then an asynchronous data transition may occur.

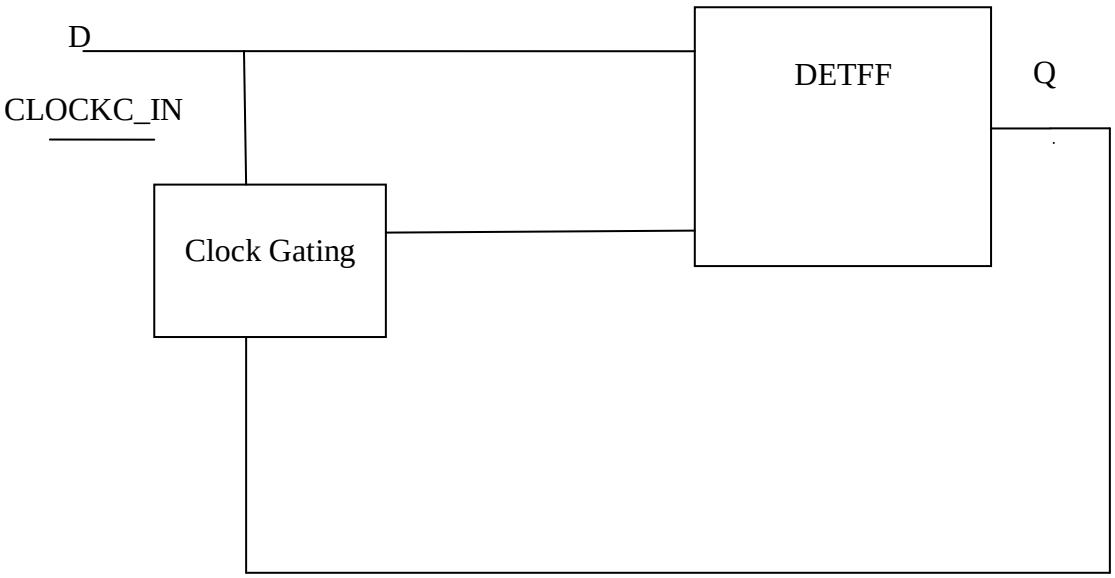


Fig. 1. (a) Block diagram of clock gated DETFF.

Fig. 1 shows an example of data miscommunication error. In this example, when D changes from 0 to 1, CG changes to 0 to allow the flip-flop to operate normally. The input D had a pulse between two clock edges. This should not be observed at the output. For asynchronous data sampling associated with clock-gated DETFFs, this pulse will be passed to the output.

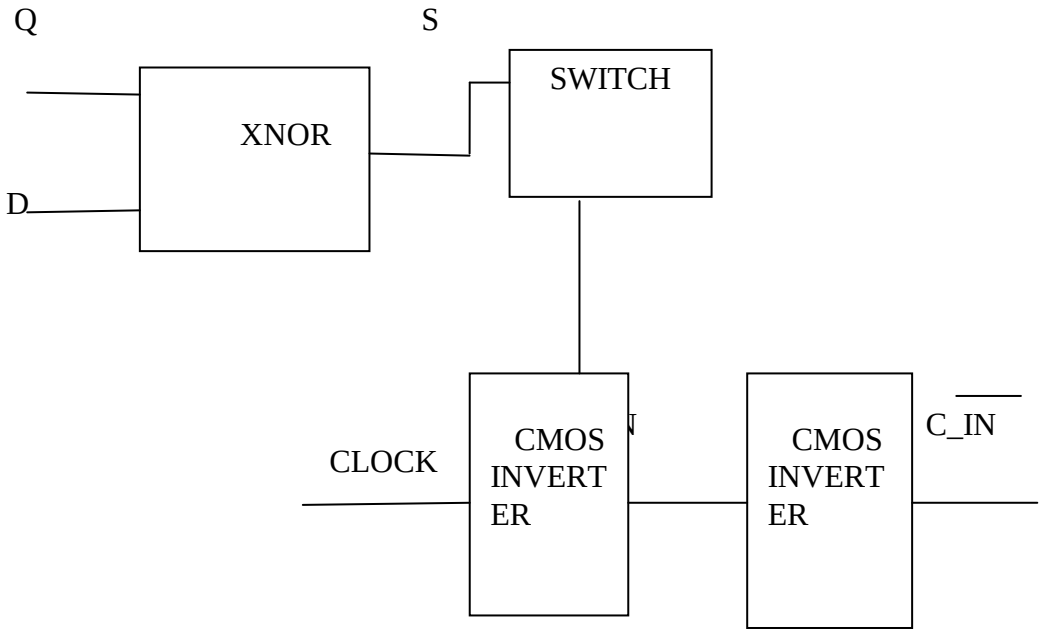
In this paper, we focus on the four cases that enable a data transition.

- Before rising edges: a) Q=0, D = 1, b) Q=1, D=0.
- Before falling edges: c) Q = 0, D = 1, d) Q =1, D = 0.

There will be 50% possibility to have an asynchronous data transition when the clock gating is turned off. When the clock gating is discontinued and if the internal clock differs from the global clock, then the internal clock event is transmitted immediately.

III. Proposed Clock-Gated Double Edge-Triggered Flip-Flop

The clock-gating signal named S in Fig.2 is generated by comparing the value of input D and output Q. PMOS is used as the switch that controls the signal path of the global CLOCK to the internal gated clock. The internal clock signals generated from the CMOS inverter chain are C_IN and inverted C_IN



D	Q	S	Switch	Inverter Chain
0	0	1	OFF	Disabled
0	1	0	ON	Enabled
1	0	0	ON	Enabled
1	1	1	OFF	Enabled

Fig. 2. Clock-gating and internal clock generating block diagram.

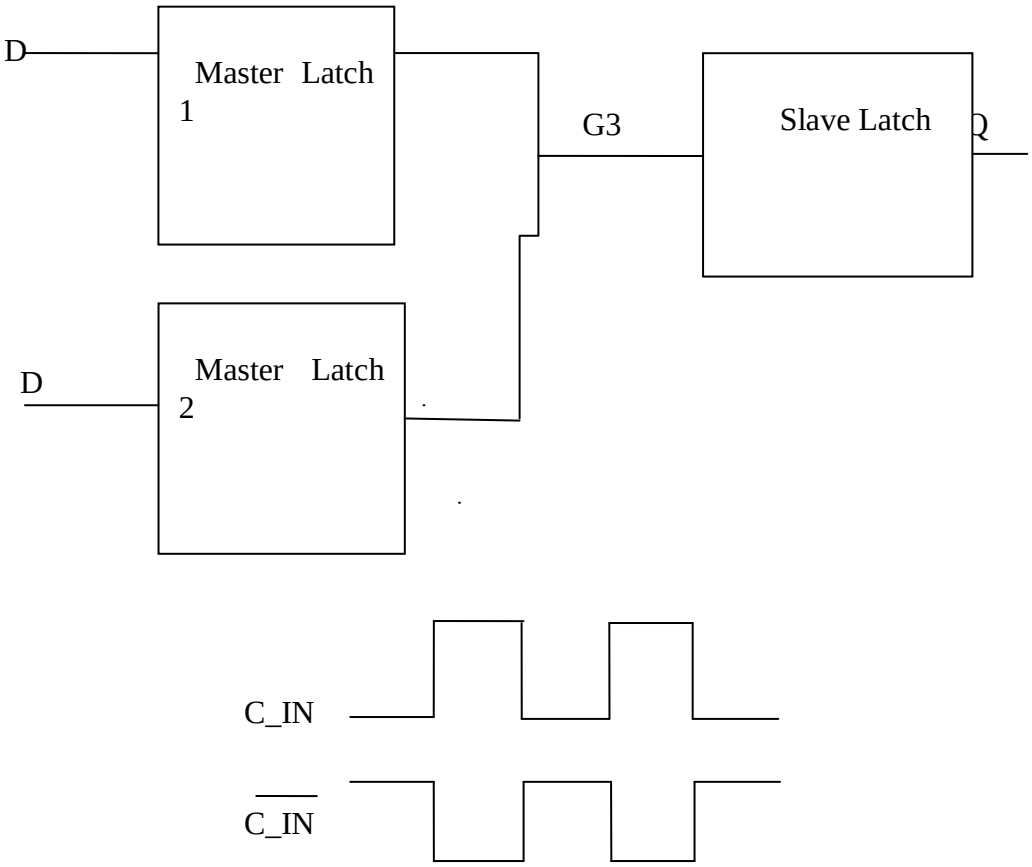
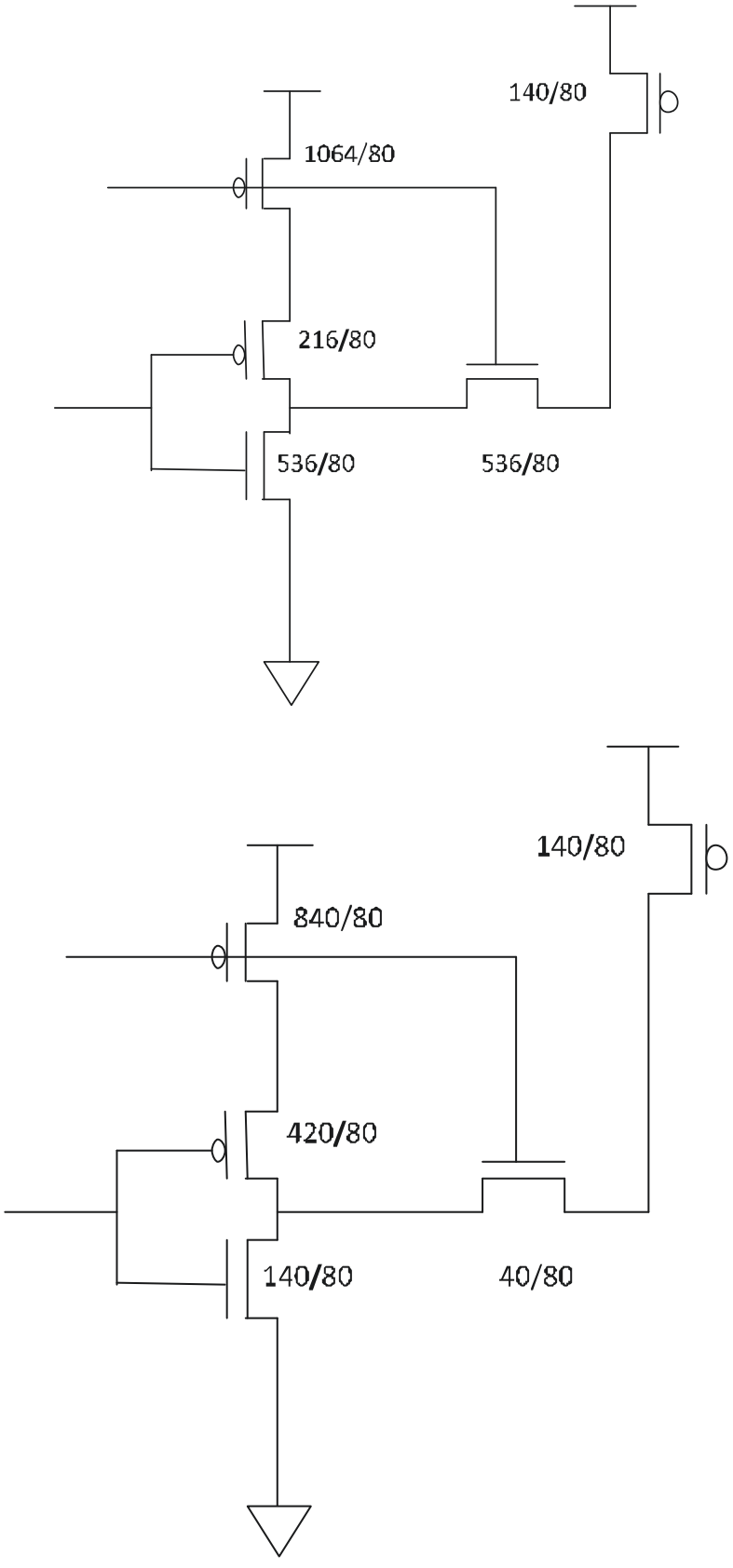


Fig. 3. Flip-flop block diagram. Master Latch 1 is referred to as the first path, and Master Latch 2 is referred to as the second path.

In Fig. 3. Master Latch 1 is referred to as the first path and Master Latch 2 is referred to as the second path. The first path transmits data on the falling edge of C_IN and the second path transmits data on the rising edge of C_IN. The gated clock signal S stays 0 when inactive. So if the input data D changed when CLOCK = 0, then the value of C_IN will change to 1 suddenly. Asynchronous data sampling occurs due to the triggering of the flip-flop by the clock edge of C_IN. The gated signal C_IN goes back to 0 and stays low until the next data transition. Master Latch 1 is always ON when the flip-flop is in standby mode. Whenever a digital signal is changed, Master Latch 2 will always be triggered first.

By adjusting the transistor sizes around node G2 of Master Latch 2, there are multiple sets of transistor sizing that can cause the asynchronous data sampling to fully appear, partially appear or be hidden. The condition that makes the asynchronous transition appear depends upon whether the voltage of node G3 reaches the critical value to flip the output.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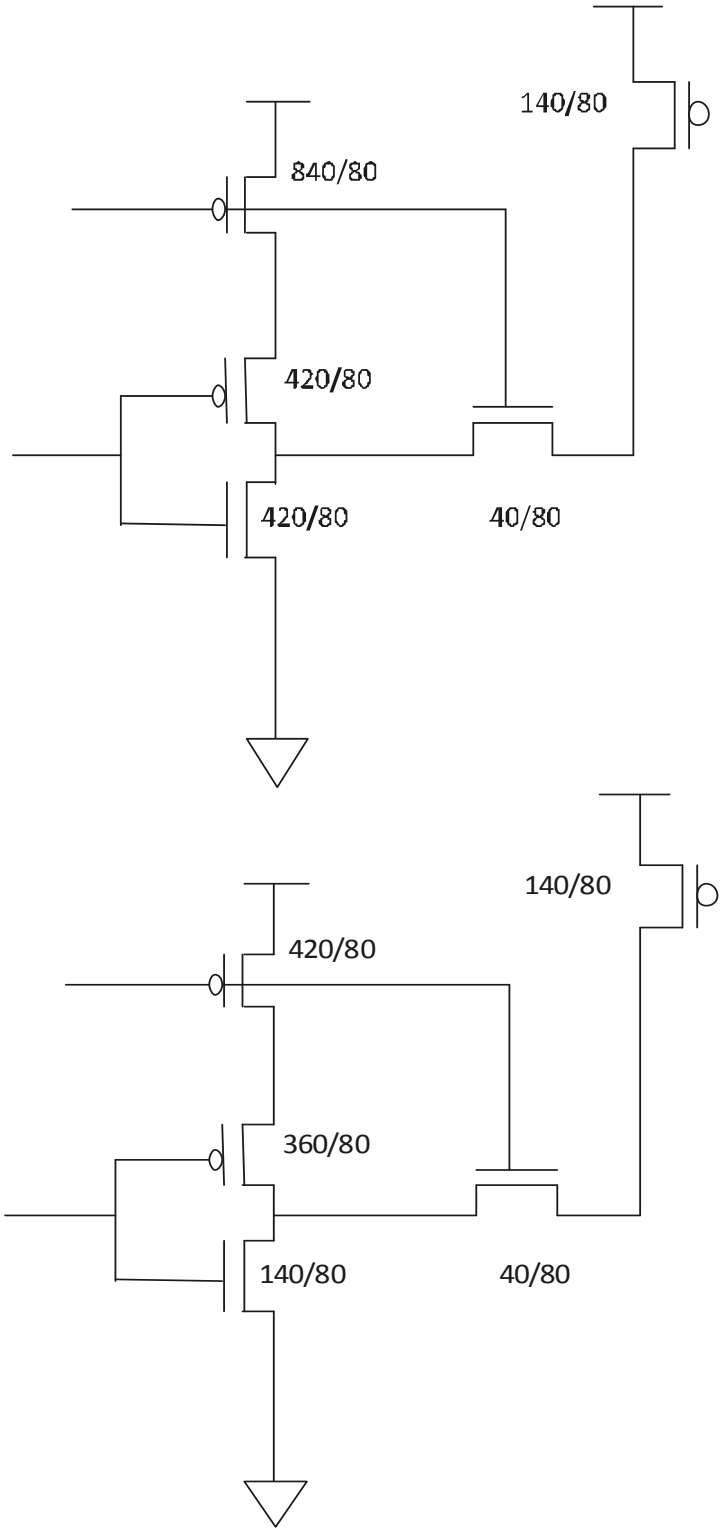

Fig. 4. Actual sizes of Master Latch 2 (a)Tam's size (b)Balanced size
(c) Modified I (d) Modified II

The actual transistor sizes used in simulation are shown in Fig. 4. The simulations are performed with the 180-nm CMOS technology.C_IN is the Internal Clock; CLOCK is the Global Clock; D and Q are Input and Output, respectively; X2 and X3 are nodes marked as in Fig. 7(B).

IV. Performance Results For The Proposed Design

The performance of the proposed DETFF is calculated by comparing the average power, delay and power delay product (PDP) of the modified structures of DETFF. TABLE 1 shows the comparison of modified DETFF structures.

Table 1: Performance Comparison Of Modified Detff Structures

Flip flop	Average Power	Delay	PDP
Tam's size DETFF	9.504	5.2	49.42
Balanced size DETFF	8.32	4.8	39.93
Modified I DETFF	9.1	5.1	46.41
Modified II DETFF	3.72	2.1	7.812

V. Conclusion

The flip-flops are the targets for optimization and improvement, as they are the basic elements of a computing system. A variety of power reduction techniques emerged because of the high demand of mobile devices on power efficiency. Clock gating and DETFF are two methods to reduce dynamic power consumption. Both of them are successful when used separately.In this paper, a low power clock gated DETFF has been proposed. Modified structures of DETFFs have also been discussed here. The simulation results show that proposed DETFF offers improvement in power dissipation. Therefore the proposed DETFF have been applied to low-power application specific integrated (ASIC) designs and also have been employed in high-level synthesis as the primary storage element.

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