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Research of horizontal structure of Split-Drain Magnetic-Field Sensitive Field-Effect Transistor

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Abstract-
This article presents the results of numerical modeling the horizontal structure of Split-Drain Magnetic-Field Sensitive Field-Effect Transistor (HSDMAGFET). Separation of drain areas were implemented by using p-region build-in deep into the drain area. In article received the dependencies of the sensitivity of the transistor from the length of the channel and from the thickness of the separating drain region.

Keywords: Hall sensor, MAGFET, HSDMAGFET.

Introduction

Integrated sensitive Hall elements are widely used in the creation of modern magnetically sensitive circuits, since relatively easily integrated into a CMOS technological process. There are several different designs of integrated Hall element. Usually, Hall elements are created in the form of a Wheatstone bridge [1, 8], technologically implemented in the layer n-well, often pinched from above the p-region [2, 10].The further development of this design is to add a gate above the active region [3, 7], which provides additional control of the Hall element by changing the parameters of the conducting region the voltage across the gate. Further study of the Hall elements has led to structures in the form of a MOS transistor with a separated drain, MAGFET [4, 13], the ratio of drains currents is proportional to the magnetic field. This design allows integration of the Hall elements directly in the converter circuit path. Further development of the constructs of Hall elements in the form MOS structures is embodied in a Horizontally-Split-Drain Magnetic-Field Sensitive Field-Effect Transistor, HSDMAGFET [5, 11], differed by MAGFET that drain region separated in a vertical plane. The article [6, 9, 14] presents a model of horizontal magnetic-field sensitive transistor with separate drain area.
The dielectric thickness of 20 nm split up the drain region. However, such device is very difficult to fabricate, due to the thin oxide layer in the silicon substrate. Inculcation boron doping area instead of a thin dielectric is more technological. This article presents the results of a two-dimensional simulation of transistor with drain separating the p+region.

Formulation of the task

The goal of this work was to study the influence of the design parameters on the sensitivity of the structure of the MAGFET in which the drain region separated in a vertical plane.

The modeling technique

To solve this problem the HSDMAGFET model has been created using Sentaurus TCAD simulator.
The structure is a standard n-MOSFET with the p+-region inserted into the n+-drain region, which performs the same function as the dielectric of [6, 12]. Fig. 1 shows the resulting doping distribution on the horizontal cross-sections of the structure, the cross section C1 is located near the surface, and C2-in the middle of the p-doping region.
The distribution of resulting doping in the in the source-drain areas approximated by a Gaussian function. The drain region was created using complex analytical profile, which is shown in Fig. 2.
It has three local maxima, the central-a p-type doping, and the side correspond to the n-type doping.
For simulation, different structures with various thickness of a p-type region and with different channel length were created.

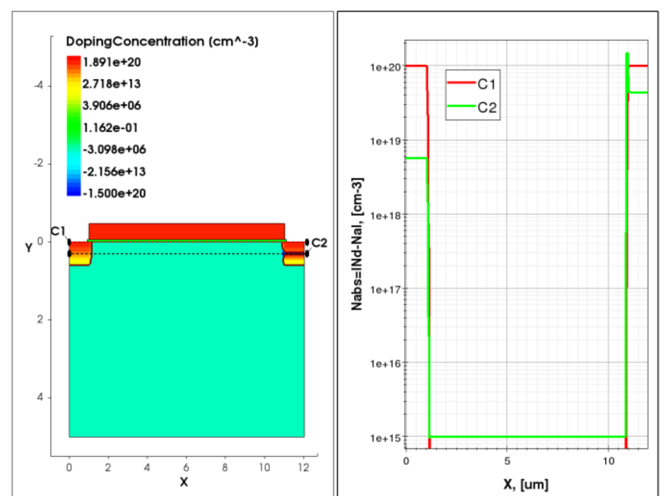

Fig. 1. Two-dimensional structure and distribution of the resulting doping of two horizontal cross-sections

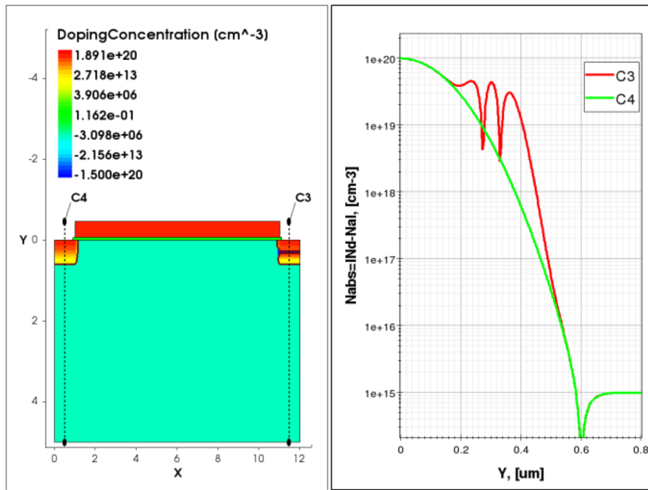

Fig. 2. The distribution of resulting doping in the source-drain areas

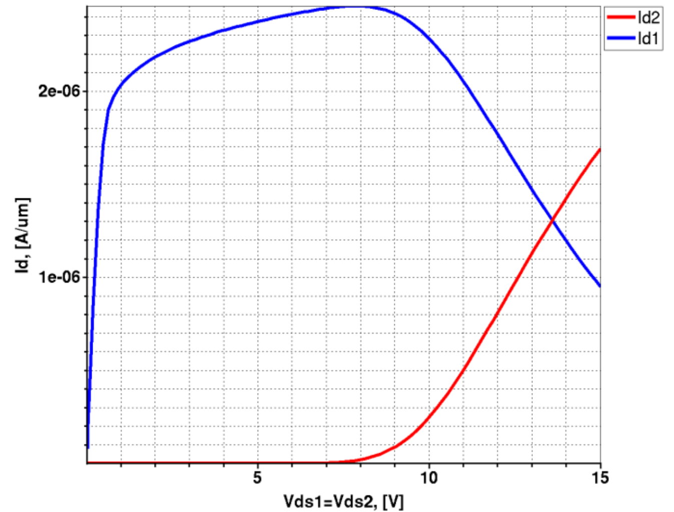

Fig. 3. Simulated output characteristics for the HSDMAGFET of Fig. 2; the channel length L=10 μm, $V_{DS1} = V_{DS2}, V_{GS} = 1V, B_Z = 0\,T$.

Results

For the simulation the following parameters were utilized structures: $T = 300°K$, $N_{bulk} = 10^{15}cm^{-3}, t_{ox} = 60\,nm$, $X_{j,sd} = 0.6\,um$, $L = 10\,um, V_{GS} = 1V$. To calculate the electrical characteristics the drift-diffusion model with the Shockley-Read-Hall recombination and the velocity saturation models were used. The output characteristic of the transistor is shown in Fig. 3. In Fig. 4 you can see the distribution of the electron current density in the vicinity of the drain $V_{DS1} = V_{DS2}$ =15V and $V_{GS} = 1V$.

Fig. 3 shows that for voltage $V_{DS1} = V_{DS2}$ = 13,6V, currents on both drains are equal, i.e. $I_{D1} - I_{D2} = 0$. If the transistor is put in an external magnetic field, the magnetic induction which is perpendicular to the cross section of the structure, at the same voltage value, $I_{D1} - I_{D2} \neq 0$. This phenomenon can be explained by the Lorentz force, which will reject the charge carriers to one of the two drains. The relative magnetic sensitivity of the transistor can be found from the formula (1):

$$S = \left|\frac{I_{D1} - I_{D2}}{(I_{D1} + I_{D2})B_Z}\right| \quad (1)$$

The length of the channel of the transistor has the most significant effect on sensitivity. This dependence, for different thickness of the separating p-region, is shown in Fig. 6.

The Fig. 6 shows that the maximum sensitivity of the transistor 14,8%/T is reached at L=40um, Vgs=1V and thickness of separation drain p-region 60nm.

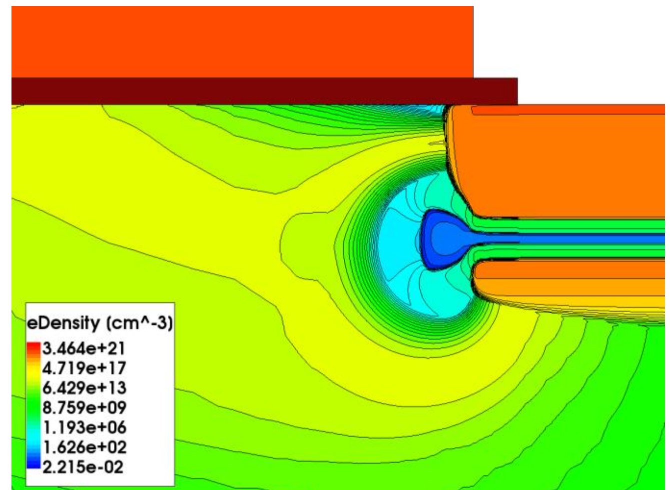

Fig. 4. Simulated electron current density near the drain region, $V_{DS1} = V_{DS2}$ **=15V и** $V_{GS} = 1V, B_Z = 0\,T$.

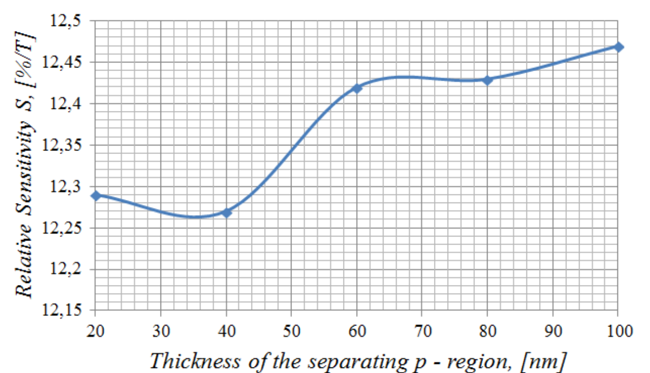

Fig. 5. Simulated relative sensitivity as a function of the thickness of the separating p-region at $B_Z = 30\,mT, L = 10\,\mu m$

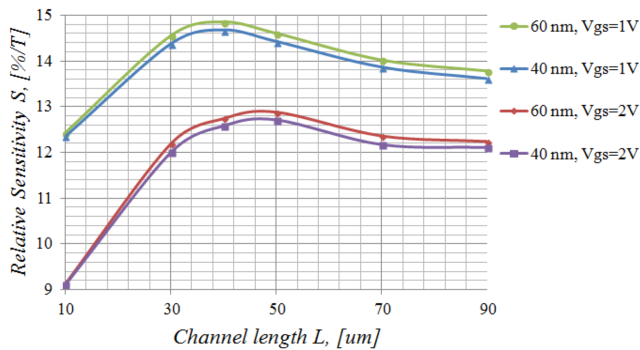

Fig. 6. Simulated relative sensitivity as a function of the of the channel length at $B_Z = 30\ \mathrm{mT}$

Conclusion

A study was conducted of the characteristics of the Horizontally-Split-Drain Magnetic-Field Sensitive Field-Effect Transistor splitted vertically by p-region. Studies have shown that the structure HSDMAGFET transistor has a sufficiently high sensitivity in low magnetic fields. The results obtained in this paper can be used to develop a device based on this structure. Identified the optimal parameters of the structure, allowing to achieve maximum sensitivity. Already when the channel length 40 um, simulated relative sensitivity in 5 times more than the experimental value 2.64%/T obtained for the standard SDMAGFET [4, 11, 14].

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