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Modeling the Effect of Local Thermal Effect on the Stress-strain state of the Conductive Layer Printed Circuit Board

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Abstract
In this article the questions of calculation of the intense-deformed condition of printed circuit boards (PCB) based on local thermal effects. The proposed model of the single-layer PCB as a system consisting of two plates rigidly fixed in a plane of contact. Heat sources are electroradioelements surface-mounted PCB. Considered various options of conditions fixing PCB-hard sealing, swivel bearing, the free edge. Mathematical model of calculation of stresses in conductive and dielectric layers of PCB, which considers linear deformation in the plane of the plates, as well as local bending moments in a dielectric plate from an unbalanced distribution of heat across the width of entire paragraphs. The equations lie in the basis of construction of computational models of PCB and estimate the degree of influence of local thermal effects on the technical condition of the printed conductors and reliability of software in general.

Keywords: Mathematical Model, PCB, Stress-strain State, Local Heat.

Introduction

High rates of development and implementation in all areas of the complex electronic systems, the rapid growth of their structural complexity and dimensions, specific conditions of use of on-board equipment and the reliability requirements of the functions determine the urgency of the problem of reliability, quality and safety operating avionics (BRES).

Ensuring the reliability, quality and safety of the BRES is connected with uncertainty and a variety of unpredictable action mechanisms of interaction of loading, aging and destruction in conditions of high dynamism of irregular power, temperature, radiation and other impacts on the structural components RES. So complex interactions require the creation of tools for modeling the dynamics of changes in the parameters of complex systems.

The problem of increasing the reliability of BRES and their components is based on the creation of diagnostic models is becoming increasingly important. This is connected, on the one hand, with increasing of the mechanical loads on BRES and, on the other hand, increasing demands to the functionality of the apparatus (increase in the degree of integration of elements, a decrease in weight and size, etc.), which leads to an increase in hardware complexity.

In practice, we face with the problem of diagnosing complex BRES with lots of possible defects that require rapid containment to prevent emergency conditions. These tasks require the development of mathematical models, methods and algorithms for the effective detection of defects, the use of which will locate a wide class of both overt and latent (hidden) defects.

Leading scientists of our country, such as PP Parkhomenko, AV Mozgalevskaya, VA Gulyaev and other., created the theoretical foundations of discrete and continuous diagnostics of technical systems.

The works of N. Kofanova presented the theory of parametric sensitivity of electronic circuits and structures to determine

how changes in their management in order to meet the requirements of the output characteristics of the RES. This theory allows us to formulate ways to ensure high levels of reliability of radio electronic equipment.

The first digital models of mechanical and thermal processes in the design of devices and systems have been developed by EN Makvetsovym and AM Tartakovsky. The works of AS Shalumova are dedicated to the development of scientific bases of creation and introduction of the automated systems of complex mathematical modeling of physical processes in the Zone, as well as to simulation techniques based on modern software tools. The works of A. Fadeyev are dedicated to the development of methodology of interactive synthesis of design solutions RECs in accordance with the principles of CALS-technologies. The list can go on and on.

At the same time there is a problem of characterizing the degree of local thermal impact on printed circuit board that is a main commutation element of the aiborne radio-electronic equipment (AREE) with the function of being a carcass for radiocomponents. It is necessary to carry on analyses of thermomechanical stresses, occurring in anisotropic layers of the printed circuit board, which leads to its creasing, deformation of printed wires and results in development of dormant defects and their further transformation into real defects that consequently causes failures in operation of AREE [1, 2]. Thus, it becomes actual to develop new effective models for solving the problems of AREE diagnostics, consisting of several thousands of units, as well as to construct strategies of diagnostics of AREE technical condition and forecasting behavior of modern AREE. It is fully applicable to the analyses of thermal impact on printed circuit boards, containing thousands of commutation elements. The modeling of thermal effects on printed wires allows to measure their operational performance in conditions of prolonged exposure to external unfavourable factors.

During the analyses of complex AREE with the use of mathematical model method there are some problems connected with the high dimension and necessity to consider many factors incident to the system and influencing the problem solving degree.

Analyses Of Stress-Strained Printed Circuit Board With Allowance For Thermal Effects

Let's take single-layer circuit board that has the following grip conditions: anchorage, hinge support, free edge [3, 4]. The single-layer circuit board consists of two slats attached to each other in the *xOy* (pic 1). One of them is dielectric and the other is metal. In order to make calculations we divide this system into separate slats. For each slat we determine magnitudes of direct and tangential stresses appearing in condition of thermal effects. The largest number of defects occurs when there is a break of conductive wires (pic 1).

Let's consider the cooper conductive layer of the circuit board as a separate slat. If it is free of any fixing, its heating on amount ΔT leads to an increase in the linear dimensions in three coordinate positions. In such case relative amount of linear thermal deformation is αT, where α is a coefficient of temperature expansion. Such free thermal deformation doesn't cause any additional stresses in the slat.

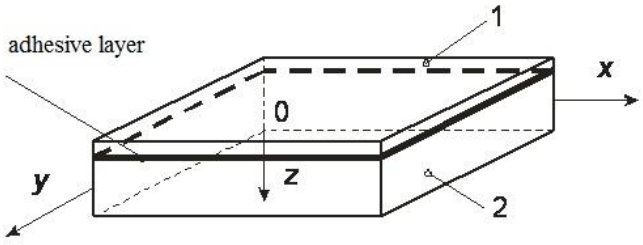

Fig. 1. General view of the printed circuit board: 1-cooper conductive layer; 2-woven-glass reinforced dielectric layer

If the temperature changes irregularly or the slat has some fixing elements (cooper layer is attached to dielectric slat), thermal expansion of some units of the slat will be restrained by the contact with the other units. Thus, there are some additional temperature stresses in the slat.

In the elasticity theory the problem of finding these stresses (temperature problem) can be handled as an ordinary elasticity problem with the modified recording of Hooke's law [5]:

$$\sigma_x = \frac{E}{1-\mu^2}(\varepsilon_x + \mu\varepsilon_y) - \frac{E\alpha T}{1-\mu};$$
$$\sigma_y = \frac{E}{1-\mu^2}(\varepsilon_y + \mu\varepsilon_x) - \frac{E\alpha T}{1-\mu}; \quad (1)$$
$$\tau_{xy} = G\gamma_{xy};$$

Where temperature $T > 0$; σ_x -direct stress along *Ox*; σ_y -direct stress along *Oy*; E -Young's modulus; ε_x - relative strain along *Ox*; ε_y -relative strain along *Oy*; μ - Poisson's ratio; G -modulus of transverse elasticity; τ_{xy} - tangential stress in the *xOy*; γ_{xy} -shear strain in the *xOy*.

If we make magnitudes $\varepsilon_x = \varepsilon_y = \gamma_{xy} = 0$ equal, we'll find stresses, appearing in the slat in free condition:

$$\sigma'_x = \sigma'_y = -\frac{E\alpha T}{1-\mu}; \quad \tau'_{xy} = 0. \quad (2)$$

If changes of the temperature in the cooper slat having gage of 30-50 mym are symmetrical for *xOy* ($T = T(z)$), each volume $\partial x \cdot \partial y \cdot h$ (pic. 2) separated from the slat is in identical conditions and its deformation ε_z can be free.

Stress state in the absence of fixing will have the form (3)

$$\sigma'_x = \sigma'_y = -\frac{E\alpha T(z)}{1-\mu}; \quad \tau'_{xy} = 0. \quad (3)$$

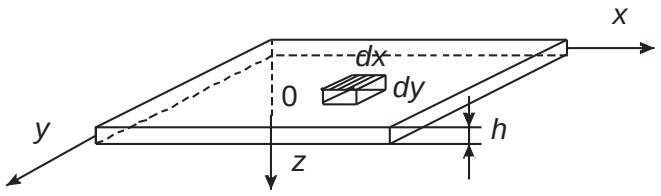

Fig. 2. Free of fixing conductive plate (copper layer)

similar voltage must occur while the free thermal expansion of the dielectric plate but koffitsient thermal copper's linear expansion($\alpha_м$) (AST) approximately is about three times greater than fiberglass($\alpha_{ст}$), of which a theoretical circuit substrate board is making, so and the deformation of the copper layer will be proportionally greater. Taking in consideration the modulus magnitude elasticity of copper $E_м$=1,3·10^{11} Н/м^2, and fiberglass $E_{ст}$ = 3 ·10^{10} Н\м^2 it turns out that the linear tensile stresses $\sigma_x = E\varepsilon_x \quad \sigma_y = E\varepsilon_y$ should also be greater than in the dielectric layer

Then, if the any sides plates1 (see picture 1) are fixed (copper layer fixedly "glued" to the dielectric layer), so it occurs that during the heating of plate the volumetric load stresses appears which applied to the face plate X=0, X=a Y=0, Y=b, These loads produce resultant forces on corresponding coordinates per unit of faces length N'_x and N'_y:

$$N'_x = N'_y = \int_{-h/2}^{h/2} \sigma'_x dz = -\frac{E\alpha}{1-\mu} \int_{-h/2}^{h/2} T(z)dz. \quad (4)$$

if the T(z)□ 0(flat is heated by) the stresses and strains will be compressed.

If the plane cools so the loads will be stretched $N_x = -N'_x; \quad N_y = -N'_y$ (pic.3) Stresses occur because of such uniform central tension (second condition)

$$\sigma''_x = \sigma''_y = \frac{N_x}{h \cdot 1} = -\frac{E\alpha}{(1-\mu)h} \int_{-h/2}^{h/2} T(z)dz. \quad (5)$$

The value should be considered only for conducting (copper flat) layer.

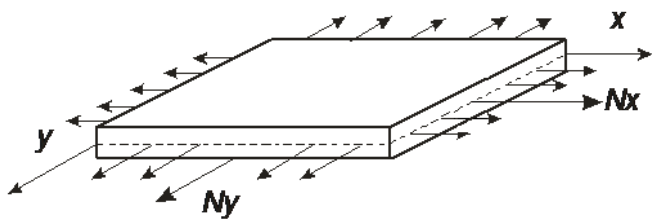

Fig. 3.

$$\sigma_x = \sigma'_x + \sigma''_x, \ \sigma_y = \sigma'_y + \sigma''_y, \ \tau_{xy} = \tau''_{xy} \quad (6)$$

Thus

$$\sigma_x = \sigma_y = \frac{E\alpha}{1-\mu}\left[T_{cp} - T(z)\right], \quad (7)$$

Where $T_{\text{ср}} = \frac{1}{h}\int_{-h/2}^{h/2} T(z)dz$ significantly average temperature along the plate thickness. Temperature distribution *T*(*z*) can be not symmetric towards to the thickness of the dielectric slab

If the heat source is a specific-(chip, transistor or other element then comes local heating systems) and then the temperature gradient be should determined through the thickness of the axis(Z) while passing the heat flux through the wall plate F (slab). Assume that the area of the base of the transistor is warming up is *S* = 100 mm^2. Suppose that this is going to cost the flow of heat F = 1.The thickness of the board is h= 1,2 Then the temperature gradient between the upper and the lower plane is: $t_1 - t_2 = \Phi R_n = \Phi \frac{h}{\lambda S}$,

where λ coefficient thermal conductivity material for fiberglass is:

λ = 0,23 ÷ 0,34 Вт/м^2 °С.

we shall use the average value of the thermal conductivity λ = 0,3

$$t_1 - t_2 = 1\frac{1,2 \cdot 10^{-3}}{0,3 \cdot 100 \cdot 10^{-6}} = 40°C.$$

If the t_2 = 40°C accordingly t_1 = 60°C, the deformation strain and tension of the top layer will be greater than the lower. Therefore in that_temperature *T*(*z*) not symmetrical relatively to the thickness of the plate and fiberglass in the heated zone must appear bending moments M_x и M_y.

The peculiarity of Pp is a feature of the conductive layer is a micron-thick membrane which is glued to the dialetric base.

It is known that the membrane doesn't resist a bend [5], and it doesn't make to consider any special sense in it.

Using a magnitude $z = h/2$, we can find the bending moment in the section of a dielectric plate in a heated state:

$$M_x = M_y = N_x \cdot z = \frac{E_{\text{ст}}\alpha_{\text{ст}}}{1-\mu} \int_{-h/2}^{h/2} zT(z)dz; \quad (8)$$

where $E_{\text{ст}}$ -is the module of fiberglass resiliency, $\alpha_{\text{ст}}$ - LETC of fiberglass.

Thus we will find tension in the top stretched layer of a plate (fig. 4):

$$\sigma_x = E_{cm} \cdot \varepsilon = E\frac{z}{\rho_\kappa}, \quad (9)$$

where ρ_κ -is the curvature radius in a point.

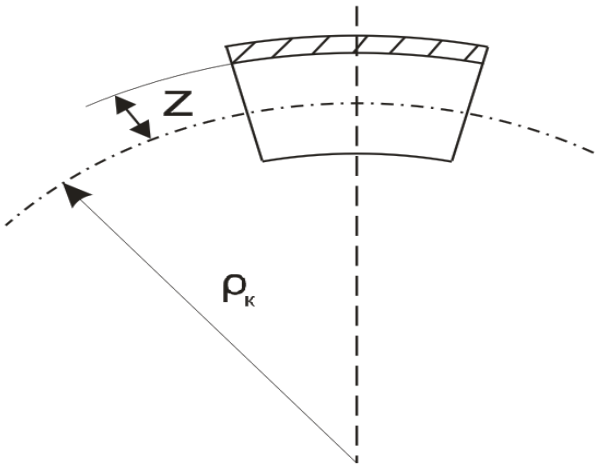

Fig. 4. Flexural tensions determination

Using the resilient line equation in a beam, we receive:

$$\frac{1}{\rho_к} = \frac{M}{EJ_y}.$$

Having increased both parts on *z*, we transform it to

$$\frac{E \cdot z}{\rho_к} = \frac{M \cdot z}{J_y}, \quad m.e. \quad \sigma_x = \frac{M_x \cdot z}{J_y}, \qquad (10)$$

where J_y -is the moment of section inertia.

As the conductor layer is rigidly related to the dielectric basis, we consider that the top layer tension σ_x will affect a conductor layer as tangent tension.

Then the full conductor layer thermal stress is:

$$\sigma_x = \sigma_y = \frac{N_{x(м)}}{h_м} + \frac{M_{x(ст)} \cdot z}{J_{y(ст)}} - \frac{E_м \alpha_м}{1-\mu} T(z) = \qquad (11)$$

$$= \frac{E_м \alpha_м}{1-\mu} \int_{-h/2}^{h/2} T(z)dz + \frac{E_{ст} \alpha_{ст}}{\frac{(1-\mu) \cdot h_{ст}^3}{12}} \cdot z \int_{-h/2}^{h/2} zT(z)dz - \frac{E_м \alpha_м}{1-\mu} T(z).$$

where the *"m"* index means that the corresponding magnitude belongs to a copper layer.

Having taken the integral, we receive:

$$\sigma_x = \sigma_y = \frac{E_м \alpha_м}{1-\mu} \cdot z_м \cdot T(z) + \frac{12 E_{ст} \alpha_{ст}}{(1-\mu) h_{ст}^3} \cdot \frac{z_{ст}^3}{2} \cdot T(z) - \frac{E_м \alpha_м}{1-\mu} \cdot T(z). \qquad (12)$$

The received mathematical model (12) allows to determine thermal stresses magnitudes on the axes set coordinates with an account of local sources thermal influences.

Further it is necessary to determine a temperature field of software fiberglass basis from local sources heating by heat experimentally or by modeling. It is possible to determine the directions by axes *Ox* or *Oy*. According to it temperature overfalls will be maximum. Having entered these values into the copper layer temperature model (12) (as external influences) we receive the maximum values of thermal stresses in this layer in the chosen directions.

These calculations will allow to estimate the overstrain conditions in a conductor layer leading to conductors rupture of printed circuit wiring.

If there are no conductor software layer defects (sinks, cracks, etc.), the breaking point will be equal to temporary resistance $\sigma_в$ (strength) of layer material [6]. Comparison of set tension with the possible will allow to estimate probability of the printing conductor rupture and the software refusal emergence.

So, for example, if there is a printing conductor defect (a round opening) at monoaxial stretching of the thermal stresses conductor can lead to the increase of value tension to 3 [4]. If magnitudes of this tension come nearer to $[\sigma_в]$, even at $\sigma_x < [\sigma_в]$, the material destruction can begin. It can lead to a rupture of the printing conductor and software refusal.

Besides, cyclic repetitions of heat-prostrations, even at available lacks of tension, with a high probability can lead to emergence refusals. It that can be also predicted on the basis of the removed ratios.

Conclusions

The received equation forms a basis for the analysis of the intense deformed condition of a conductor software layer with an account of heterogeneity caused by the local heat sources (chips, transistors, etc.) located at the fiberglass basis.

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References

[1] A. V. Zatyilkin, V. B. Almametov, A. V. Avdeev, G. V. Tankov, N. K. Yurkov, V. Ya. Bannov, "Modelirovanie nestatsionarnyih teplovyih poley elektroradioelementov", Trudyi mezhdunarodnogo simpoziuma Nadezhnost i kachestvo.-2010.-T. 2.-S. 446-449.

[2] A.V. Grigor'ev, N.V. Goryachev, N.K. Yurkov, "Way of measurement of parameters of vibrations of mirror antennas. 2015 International Siberian Conference on Control and Communications (SIBCON). Proceedings", Omsk: Omsk State Technical University. Russia, Omsk, May 21−23, 2015. IEEE Catalog Number: CFP15794-CDR. ISBN: 978-1-4799-7102-2. DOI:10.1109/SIBCON.2015.7147031

[3] N. K. Yurkov, "Tehnologiya proizvodstva elektronnyih sredstv", M: Lan, 2014.-468 s.

[4] K. I. Bilibin, A. I. Vlasov, L. V. Zhuravleva, "Konstruktorsko-tehnologicheskoe proektirovanie elektronnoy apparaturyi: ucheb. dlya vuzov", pod obsch. red. V. A. Shahnova.-2-e izd., pererab. i dop.-M.: Izd-vo MGTU im. N.E.Baumana, 2005.-563 s.

[5] A. V. Aleksandrov, V. D. Potapov, "Osnovyi teorii uprugosti i plastichnosti", M.: Vyissh. shk., 1990.-400 s.

[6] M.V. Kashin, "Kurs fiziki", M.: Vyissh. shk., 1962.-T. 2.-643 s.

[7] E. M. Morozov, A. Yu. Muyzemnek, A. S. Shadskiy, "ANSYS v rukah inzhenera: mehanika razrusheniya", M.: LENAND, 2010.-456 s.