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Analysis of the Effect of Inverter of Different sizes on the XOR/XNOR Gates at Reduced CMOS Process Technology

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Abstract

Scaling down in process technology has led to reduced MOS transistor feature sizes thereby increased circuit complexity and the number of transistors in a given area. This causes more power dissipation and reduced propagation delay. Different logic structures to represent the logic function were explored aimed at reducing power and propagation delay. Sometimes, full output voltage swing is not attained. This limits the output drive capability of the logic function or the gate. A CMOS inverter is one basic circuit that comprises of a balanced pull-up PMOS and pull-down NMOS network. Inverters do produce full output voltage swing and proper transistor sizing reduce the propagation delay. In this paper, detailed analysis of two inverters, one with Wn/Ln = 2/1, Wp/Lp = 3/1 and the other with Wn/Ln = 5/1, Wp/Lp = 5/2 was done. It was found that former was 18. 3% power efficient but 59. 08% slower than the latter. The effect of these two inverters were analysed by inserting each of them separately, at the outputs of the XOR/XNOR gates. All the circuits were simulated using 32nm process technology.

Keywords: low power; logic style; sizing;

Introduction

The world is witnessing an ever growing demand for hand held, portable electronic devices. The scaling down in process technology has reduced the size of the transistors and so one might expect a fall in the power dissipated. But on the contrary more number of transistors can be packed in a smaller area, the devices go smaller, more compact and the power dissipated tends to increase. This also puts strain on the designer in the form of circuit complexity. The total power dissipated can be considered as the sum of static power and dynamic power. Static power dissipation is due to gate leakage and sub threshold leakage and dynamic power dissipation due to the switching activities at the nodes of the circuit. [3]

In the design hierarchy, logic gates form one of the lowest abstraction levels. The logic gates or functions form the basic building blocks of any complex logic design. An inverter is the most basic circuit at transistor level. These CMOS logic gates or functions can be implemented using a pull-up and pull-down network connected in series. These complementary CMOS circuits produce full output voltage swing most of the time, but the major drawback being increased number of transistors, area and power dissipation.

To overcome this, several logic structures were used in constructing these gates. Each of the logic structures like, pass transistor logic, double pass transistor logic, transmission gate, high performance transmission logic, inverter based logic, etc., have their own advantages and drawbacks. Power dissipation is not the only pre dominant factor to be considered during a digital logic design, propagation delay, the one that marks the speed of the circuit too must be taken into consideration.

In this paper, performance of two complementary CMOS inverters, one with NMOS and PMOS transistor sizes as Wn/Ln = 2/1, Wp/Lp = 3/1 and the other with Wn/Ln = 5/1, Wp/Lp = 5/2 is analysed in section II. The operation, advantages and disadvantages of existing XOR/XNOR gates is discussed in section III. Section IV puts forth experimental setup and simulation results for the two inverters as well as the XOR/XNOR gates without inverter and with the inverters at their outputs. Conclusions are drawn in section V.

Conventional Inverter

Complementary CMOS inverter Fig. 1a [4] uses a pair of complementary switches – a pull up PMOS connected to output node and supply and, a pull down network connected to output node and ground. When Vin is low, pull-up transistor gets closed and pull-down gets opened. The supply is connected and current flows and so power is dissipated. When Vin is high, pull-up transistor gets opened and pull-down gets closed. The ground is connected to output. Here again no current flows and no power is dissipated. Static power dissipation is present due to reverse biased parasitic diodes that constitute leakage current. The leakage current is given as,

$$I_{leakage} = i_s (e^{qV/kT} - 1) \quad (1)$$

The static power dissipation can be calculated from the leakage current and power supply voltage as,

$$P_{static} = I_{leakage} \times \text{Supply voltage} = I_{leakage} \times V_{dd} \quad (2)$$

If the inverter is switched from one state to another, current flows to charge and discharge the load capacitance. This power dissipation is called dynamic power dissipation. A low resistance path exists between the output and ground in low output state or supply in high output state. This ensures that inverter is less sensitive to noise and other disturbances.

$$P_{total} = P_{static} + P_{dynamic} \quad (3)$$

High driving capability is due to the active pull-up and pull-down devices. The input resistance of the inverter is infinite as IG=0. Thus the inverter can drive a large number of parallel inverters with no loss in signal level but, each additional inverter increases load capacitance.

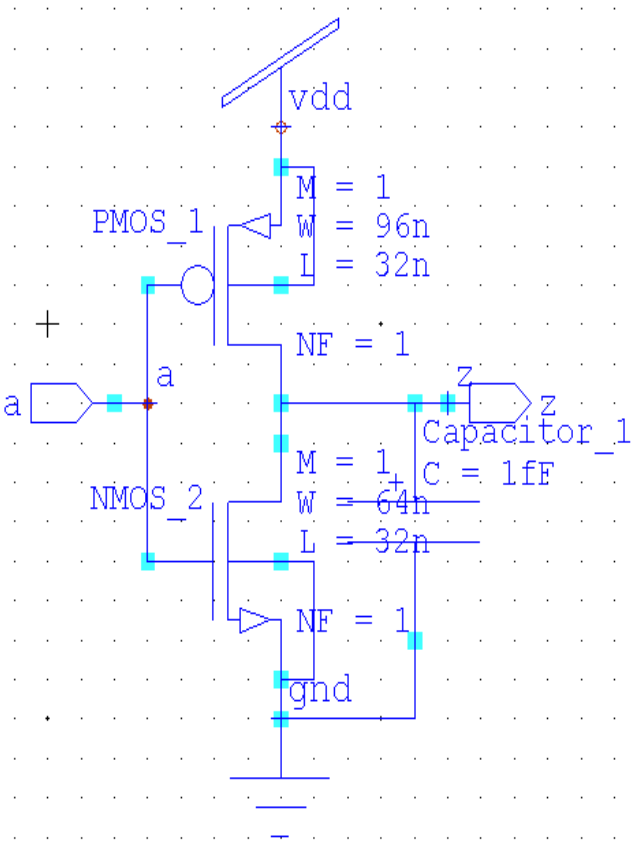

Fig. 1 CMOS Inverter.

CMOS Logic Styles

There are many logic structures [2] or styles to implement any logic gate or function. Some logic styles exhibit significant improvement in performance, some can be faster, some may consume less power while, some behave more sensitive to noise. With these metrics in mind, different CMOS logic structures for XOR/XNOR gates that are scaled down to 32nm process technology are discussed.

A. Static CMOS gates

Static CMOS circuits Fig. 2 employ pull-up and pull down networks to implement any logic function. They are robust against scaling of transistor size and supply voltage. Though, these circuits provide reliable operation with full output voltage swing, they need more number of transistors. This leads to increased power dissipation as well as delay.

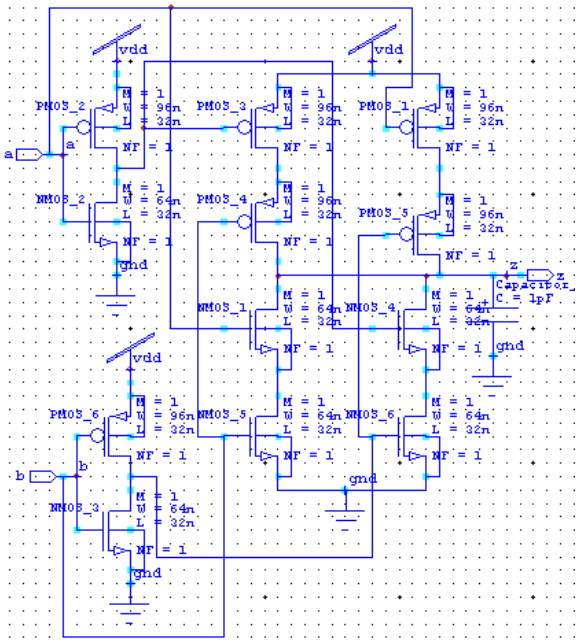

Fig. 2 Static CMOS XOR gate

B. Pass Transistor Logic (PTL) gates

In pass transistor logic circuits, n transistors are used to implement the logic function. A set of control signals are applied to the n transistor gates and another set of pass signals are applied to their sources. The number of transistors required is less compared to static CMOS.

The output voltage swing is reduced and leads to delayed switching in cascaded circuits. At reduced transistor size and supply voltage, degraded performance can be observed. The PTL XOR gate[6] in Fig. 3a produces a bad 1 for 10 input. The logic 1 output for input 10 is less than the logic 0 output voltage for the pass transistor circuit in Fig. 3b. Thus the noise margin for these circuits is poor.

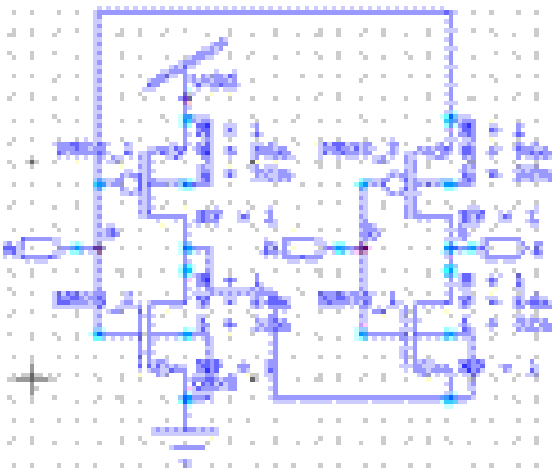

Fig. 3a PTL1

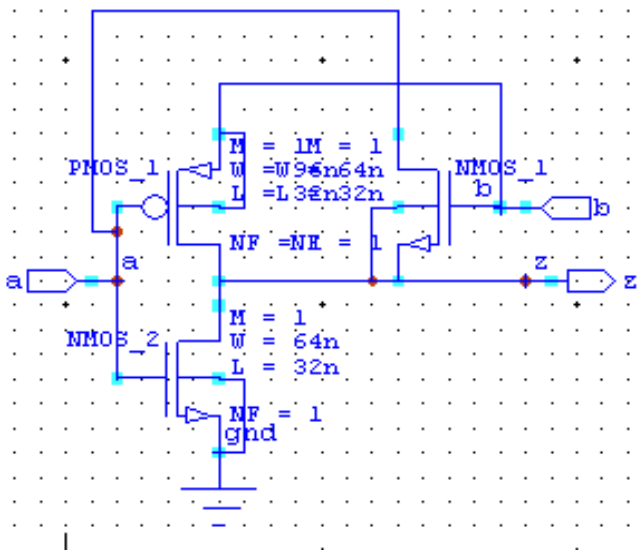

Fig. 3b PTL2

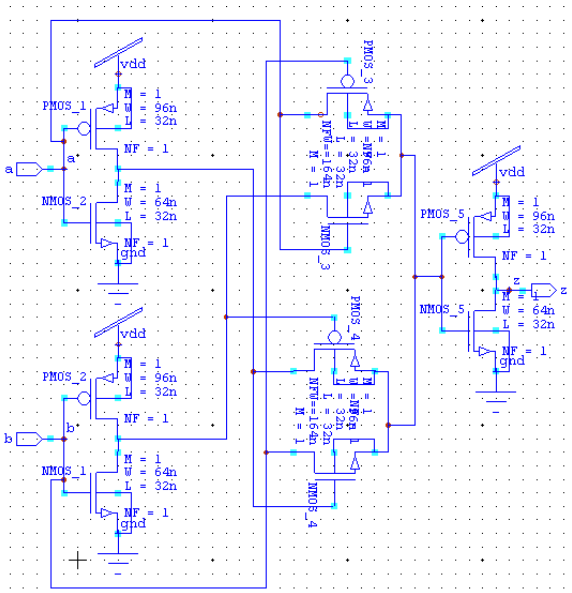

Fig. 4b XNOR DPL

C. Double Pass Transistor Logic (DPL)

Both nMOS and pMOS pass transistors are used in DPL circuits. These circuits enhance full swing operation and so there is no need for restoration circuitry. The use of complementary circuits reduce the power consumption. Presence of pMOS transistors and the requirement of complementary inputs increase the area of the logic circuit. The XOR and XNOR DPL circuits in Fig(4a and 4b) produce full voltage swing at a scaled down process technology.

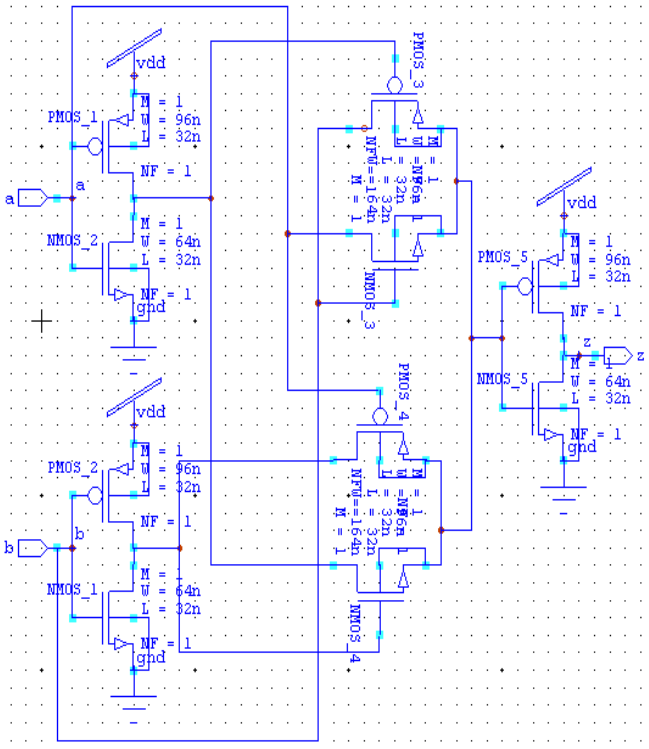

Fig. 4a XOR DPL

D. Inverter based Gates

The logic circuits of interest are designed by cascading inverters. Their operation was previously believed to be reliable only at high supply voltage but, even for scaled down transistor sizes and supply voltage the operation is reliable. The XOR and XNOR gates constructed using inverter based logic in Fig. 5a and 5b exhibit full output voltage swing.

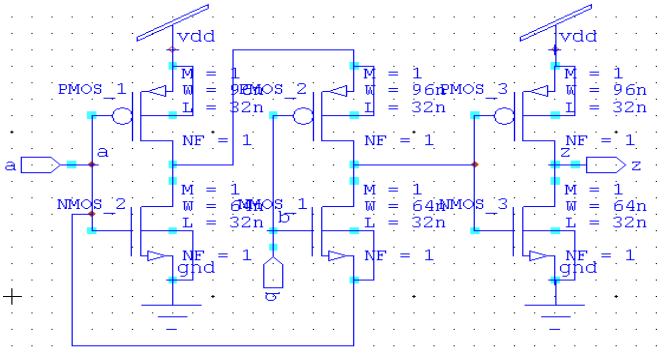

Fig. 5a Inverter based XOR

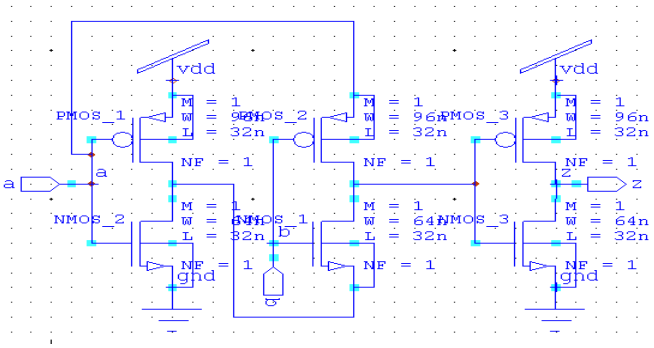

Fig. 5b Inverter based XNOR

E. Transmission Gate Circuits

A transmission gate consists of an nMOS and PMOS with separate gate connections and common source and drain connections. This logic is used to implement complex logic circuits using lesser number of complementary transistors as in Fig. 6a and 6b.

A high performance transmission gate version of XOR and XNOR gates Fig. 7a and 7b are constructed with output restoration. Both the transmission gate and the high performance XOR and XNOR gates in Fig(5. a, 6. a and 6. b) produce full output voltage swing but, the transmission XNOR gate in Fig(5. b) has incorrect output for logic 0 with reduced transistor size and supply voltage.

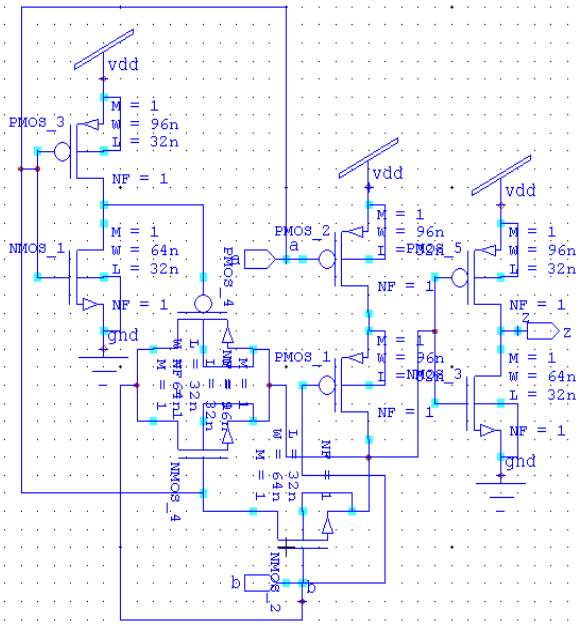

Fig. 6a Transmission gate XOR

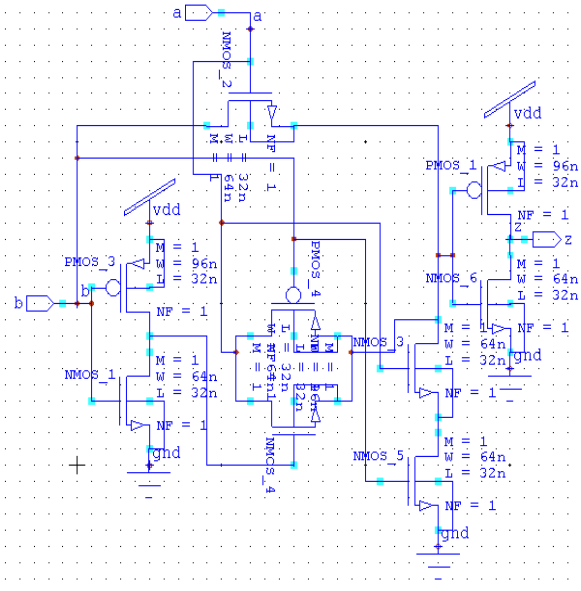

Fig. 6b Transmission gate XNOR

F. Feedback Circuits

In order to improve output voltage swing cross coupled pMOS and nMOS transistors are connected between XOR and XNOR outputs in feedback Fig. 8. These feedback circuits are also used to overcome the problem of skewed outputs for 180nm technology process as in []. But for 32nm process technology, the outputs are poor. For input combinations 10 and 11 the XOR output logic 1 and logic 0 respectively for circuit in Fig. 8 is 0. 3V, which is incorrect.

The complementary feedback circuit in Fig. 9 is based on complementary inputs. The number of transistors increase and here the performance has not improved comparatively. Even in the presence of two pull up and two pull down transistors there is no full output voltage swing. The output of the XOR gate for input combination 10 is a bad 1 even in the presence of feedback loop.

This complementary feedback circuit is hence modified as in Fig. 10 by including feed forward loop to improve the output logic level. Though this circuit has improved the output logic level, for reduced transistor size and supply voltage, incorrect outputs are produced for input combinations 10 and 00. The power dissipation is also fairly higher than any of the logic designs discussed here.

In the modified feedback XOR/XNOR circuit in Fig. 11 one pMOS and one nMOS transistor is added to attain full output voltage swing. The pMOS is to pull up the output to supply VDD and nMOS to pull down the output to ground in the case of logic 1 and logic 0 outputs respectively. Thus the driving capability of the gate is improved. The power dissipated is of the order of micro watts and the logic1 output voltage for 1V supply voltage is 0. 8V

The yet another modified complementary feedback circuit in Fig. 12 is supposed to have improved delay and attain full voltage swing. This could be achieved for 180nm but in the case of 32nm the output voltage for logic 1 and logic 0 are 0. 7V and 0V respectively. A small drop in the output voltage and no significant change in delay compared to the Fig. 11 is observed

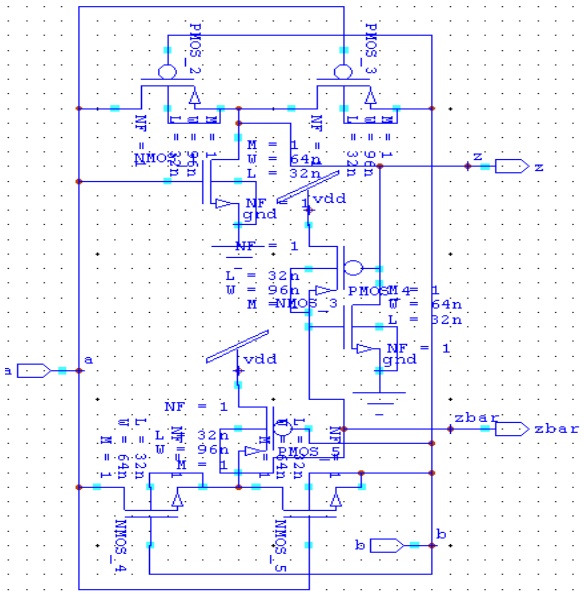

Fig. 8 Feedback XOR/XNOR gate

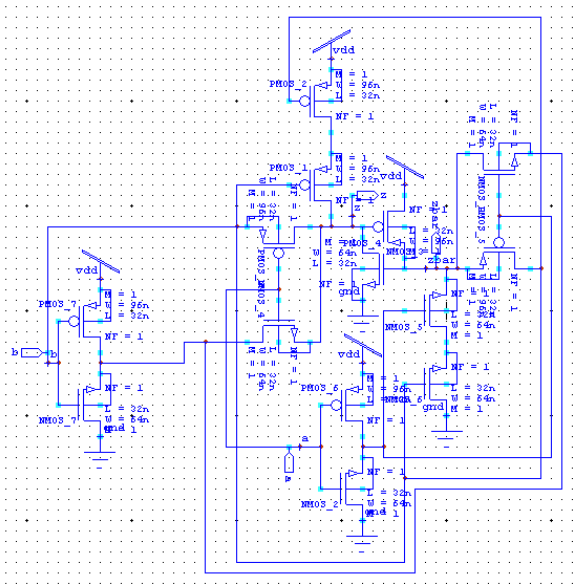

Fig. 9 Complementary feedback XOR/XNOR gate

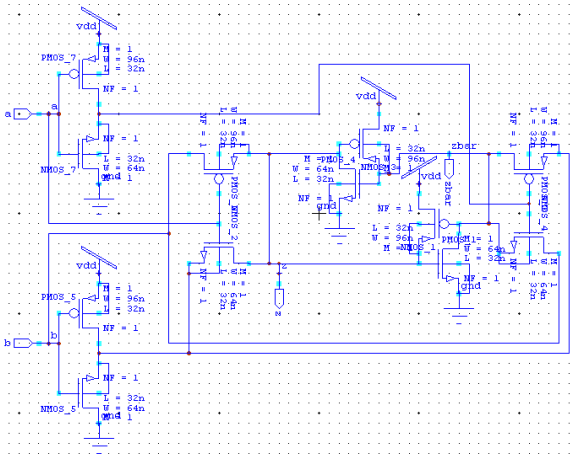

Fig. 10 Complementary feedback with feed forward loop

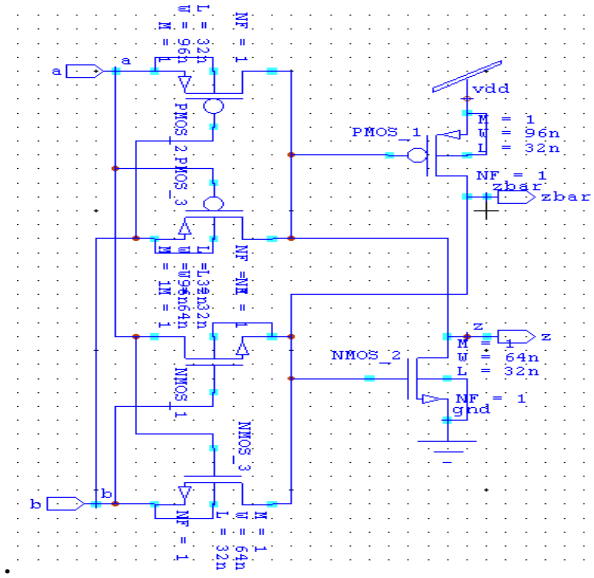

Fig. 11 Complementary feedback with restoration

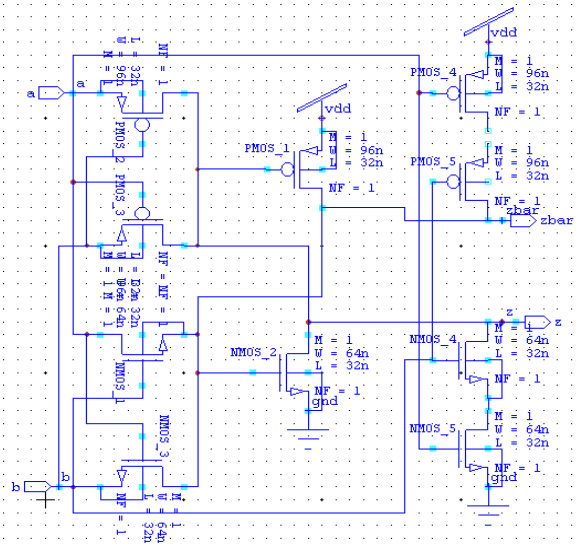

Fig. 12 Modified complementary feedback circuit

Experimental Setup and Simulation Results

The complementary CMOS inverter in Fig. 1 was simulated for two different transistor sizing namely, Wn/Ln = 2/1, Wp/Lp = 3/1 (inverter 1) and the other with Wn/Ln = 5/1, Wp/Lp = 5/2 (inverter 2)at 32nm CMOS process technology with a supply voltage of 1V. The static power and leakage current were obtained in the absence of switching activity by fixing the input at logic 1 and logic 0 level individually as in Table. 1. The average static power is then computed using equation (2). The total average power was obtained for five different inputs of eight bits each with different switching patterns. From this and the static power dissipation, the dynamic power dissipated can be computed using equation (3).

The power dissipated was found to be lower for both the inverters for the input pattern 00001111. Inverter 1 exhibited minimum delay for the input pattern 00001111 and inverter 2 exhibited an almost constant delay for all the input combinations**.**

To analyse the effect of inverters 1 and 2 on XOR/XNOR gates, the inverters were inserted one at a time at the output of these gates and simulated. The XOR gate exhibited XNOR operation due to the inverter at the output and vice versa. The average power dissipated and the propagation delay was noted from the simulation results. Comparison was made among gates without inverter, with inverter1 and then with inverter 2 as in Table 3.

Table. 1 Static power dissipation and leakage current

Circuit	Vdd = 1V					
	Static Power (P_{static}) x 10^{-8}W			Leakage Current (I_{leak})x nA		
	V_{in} = 0V	V_{in} = 1V	Average	V_{in} = 0V	V_{in} = 1V	Average
Inverter 1 W_n/L_n = 2/1, W_p/L_p = 3/1	3.545	3.227	3.386	35	35.5	35.25
Inverter 2 W_n/L_n = 5/1, W_p/L_p = 5/2	8.81	0.0075	4.408	88	0.0075	44.004

Table. 2 Power dissipated for different input combinations

Circuit	Input bit pattern (V_{in}) Logic 1 = 1V; Logic 0 = 0V					
	Parameter	00001111	00110011	11001100	01010101	10101010
Inverter 1 W_n/L_n = 2/1, W_p/L_p = 3/1	P_{total} x 10^{-8}W	4.51	5.853	5.851	8.653	9.02
	$P_{dynamic}$ x 10^{-8}W	1.124	2.467	2.465	5.261	5.734
	Delay x 10^{-12}sec	6.012	9.005	9.01	9.01	8.66
	P_{static} x 10^{-8}W	Average = 3.386 x 10^{-8}W				
Inverter 2 W_n/L_n = 5/1, W_p/L_p = 5/2	P_{total} x 10^{-8}W	5.557	6.725	7.19	9.39	10.63
	$P_{dynamic}$ x 10^{-8}W	1.149	2.317	2.782	4.982	6.222
	Delay x 10^{-12}sec	2.46	2.46	2.46	2.40	2.40
	P_{static} x 10^{-8}W	Average = 4.408 x 10^{-8}W				

Table 3. Comparison of Power without inverter and with inverters 1 and 2.

Gate	Without Inverter			With Inverter 1			With Inverter 2		
	$P_{average}$ x10^{-8} W	Delay x 10^{-12} s	PDP x 10^{-18} J	$P_{average}$ x10^{-8} W	Delay x 10^{-12} s	PDP x 10^{-18} J	$P_{average}$ x10^{-8} W	Delay x 10^{-12} s	PDP x 10^{-18} J
Static XOR	0.2032	24.6	4.998	0.266	9.61	2.556	0.318	5.98	1.9
PTL 1	2.28	8.92	20.34	3.82	1.82	69.52	3.96	5.73	22.69
PTL 2	2.27	8.92	20.35	3.82	18.2	69.52	3.96	8.6	34.05
XOR DPL	14.8	10.12	149.77	11.5	9.3	106.95	1.16	5.82	6.75
XNOR DPL	11.7	8.52	99.68	12	9.23	110.76	11.8	5.77	68.08
Inverter based XOR	1.67	17.1	28.55	1.7	9.11	15.48	1.79	5.73	10.26
Inverter based XNOR	3.86	78.2	301.85	3.88	9.45	36.66	3.93	5.88	23.11
Transmission gate XOR	6.297	9.16	57.68	6.36	170	1081.2	6.41	158.6	1016.6
High Performance TG XOR	6.41	12.6	80.76	6.47	178	1151.6	6.52	172	1121.4
High Performance TG XNOR	7.93	11.3	89.61	7.99	9.28	74.14	8.91	5.79	47.49
Complementary Feedback XOR/XNOR	63.7	194	12357.8	64.7	140.5	9090.35	65.4	30.6	2001.24
Complementary Feedback with restoration	9.66	51.99	502.2	10.8	75	810	11.5	33.9	389.85
Modified Comple-mentary Feedback	9.67	52.7	509.6	15.3	7.8	119.34	15.85	4.198	66.53

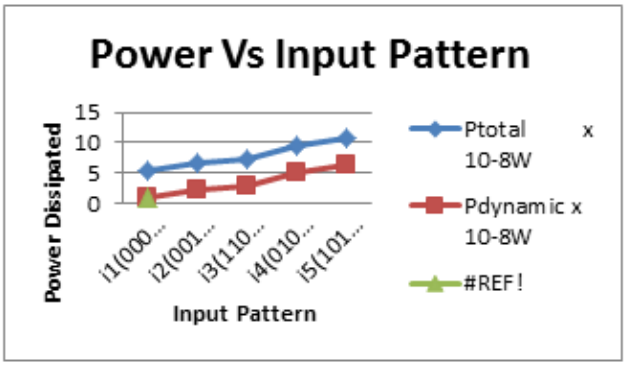

Fig. 13 Power versus Input Pattern of Inverter 1

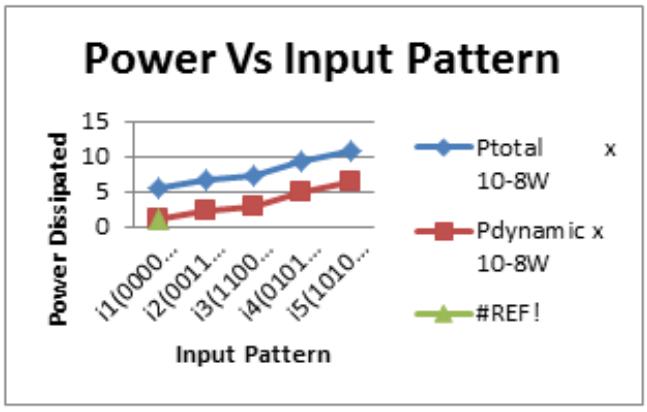

Fig. 13 Power versus Input Pattern of Inverter 2

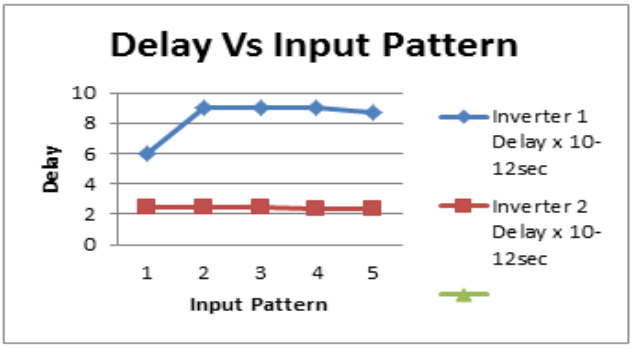

Fig. 15 Delay versus Input Pattern for Inverters 1 and 2.

Conclusion

In this paper, a detailed analysis on the performance of a basic complementary CMOS inverter subject to two different transistor sizing, one W_n/L_n = 2/1, W_p/L_p = 3/1 and the other with W_n/L_n = 5/1, W_p/L_p = 5/2 was performed. The static, dynamic power and leakage current were obtained and compared. Though the former was 18. 3% power efficient, it was found to be 59. 08% slower than the latter. The analyses were extended to verify the impact of introducing inverter at the output of other logic circuits like XOR/XNOR gates. The presence of inverter aided in acquiring full output voltage swing thereby improving the output drive capability. Also, the propagation delay was reduced considerably at the expense of minimum trade-off with power dissipation in a majority of the XOR/XNOR gates. Transistor sizing to reduce propagation delay was done only on the inverter circuit that was inserted at the output and not on any other transistor in the logic gates. Further analyses can be carried out by employing progressive transistor sizing in these logic circuits to reduce propagation delays and power dissipation

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