International Journal of Applied Engineering Research ISSN 0973-4562 Volume 10, Number 23 (2015) pp 43549-43554

Design of low leakage power SRAM using Multithreshold technique

D. Sudha[(1)]

Dept. of ECE GRIET Hyderabad, India Sudha.dsce2007@gmail.com

Dr.CH. Santhirani[(2)]

Dept. of ECE DMSSSVH College of Engineering Machilipatnam, India Santhirani.ece@gmail.com

Abstract
CMOS scaling technology has leads to sub-threshold leakage, effects of short channel, leakage of gate dielectric and device to device variations increase leakage additionally. In SoC (System on Chip), SRAM cell is occupied in the area of about 90%. It has been implementing by using FinFET, though leakage becomes the considerable main factor in SRAM. In addition, for deep submicron technologies the double gate FinFET devices are became a best option in technology where implemented in deep submicron. By this consideration, we proposed to implement 6T SRAM cell using double gate FinFET (DG FinFET) with independent gate which controlled independently with gates opposite sides that maintains excelling scalability for SRAM. The proposed device is applied using different techniques for leakage reduction namely gated V_{dd} and multithreshold voltage techniques to reduce leakage. Therefore, leakage power in the SRAM cell is decreased and provides better performance. The proposed leakage reduction techniques have been simulated using Cadence in 45 nm technology for FinFET SRAM with independent gate.

Key words-CMOS; FinFET; Double gate; DG FinFET; Multithreshold; SRAM

I. INTRODUCTION

CMOS scaling technology has leads to sub-threshold leakage, effects of short channel, leakage of gate dielectric and device to device variations increase leakage additionally. Nanometer scaling system develops a considerable effect of short channel that produces a number of effects where depletion layer is equal to channel length. Short channel effect (SCE) produced a main effect by its electric fields considerably very high i.e., DIBL. Gate is only controlled this effect. Ultrathin t_{ox} with current drive and very low threshold voltage V_{th} required for maintaining the speed of the device and variations of threshold voltage V_{th} in control while dealing SCE [3]. This effect reduces the slope of the sub threshold which causes variations in V_{th}. Subthreshold leakage and gate leakage currents mainly considered which are generated by SCE where subthreshold leakage generates while $V_{th} > V_{gs}$ and gate leakage occurs when current passes gate to substrate via oxide layer. To avoid this effects, conventional MOSFET less than 65nm is no more options. Hence, we proposed FinFETs i.e., FET with double gate where opposite of the first gate is connected to second gate so as to reduce the effects of SCE, especially for CMOS low power designs. There are two types of FinFET have been designed such as FinFET with independent gate and tied gate. In FinFET with independent gate, one of the gate acts as switch (on/off) and other gate for adjusting the V_{th} for efficient V_{th} control. It decreases the leakage and therefore decreases the power consumption and enhances the efficiency. To overcome the SCE problem, tied gate FinFET can be used where opposite of the gates are tied with each other. In Microprocessor memory occupied large area in a chip, while leakage current has a significant role thus decreases a small amount of leakage current tends to reduction of large amount in total power. Since SRAM occupied minimum area in a chip with small processing variations and stability by applying low voltages and V_{th} respectively [1, 9]. Therefore, the proposed FinFET approach is desirable for SRAM to extract additional stability and leakage power reduction [2] and also it is most preferable in nano systems with low SCE.

Many techniques has presented for reduction of leakage power. In this research work, we proposed two different techniques in circuit level named as multithreshold leakage and gated V_{dd} [4, 6]. In standby mode NMOS and PMOS functioning as switch to cutoff the supply power thus to reduce the leakage is designed in a leakage reduction technique proposed as multithreshold leakage. It drives high operating speed with small threshold MOSFET, reduction of leakage with high V_{th}. It is observed that by adapting of this technique increases the area for circuit while adding delay and parasitic capacitance at fabrication level. Therefore, we introduced a gated V_{dd} technique where SRAM cell is connected to NMOS transistor. It regulates low threshold and supply voltages by reduction of leakage and minimize the leakage power. When gated V_{dd} is in off additional transistor by combining with SRAM transistors produces a stacking effect. The gated V_{dd} technique is also used in FinFET with independent gate based on 6T SRAM.

II. CONVENTIONAL 6T SRAM CELL

It is composed by latch (cross coupled inverters) and NMOS transistors (two access) acts like pass transistors. However, latch acting as storing element and word line by access transistors. Latch inputs are connected access transistors drain terminals while source terminals to BLB (bit line bar) and BL (bit line). Disabled of the access transistors while at low, word line that is in hold state and only permitted to operations of write or read. Since the voltages maintain at gnd and V_{dd} the bit can be hold by latch. At high, enabled the access

transistors by permitting the operations of write and read. In Figure 1, shows the basic cell of 6T SRAM. The SRAM cell operation modes as follows;

A. Hold Operation

1. The data is retained while it is connected to power.
2. NM3 and NM4 (access transistors) off while WL=0 and latch disconnected with BL and BLB
3. Reinforce continuously while connecting to V_{dd} and thus flow of current is a leakage current

B. Write Operation.

1. Stored (original) bits are replaced by different bits with value which could be written by SRAM cell.
2. NM3 and NM4 (access transistors) enabled while WL=1 at write operation
3. The essential data will be written is processed to BL and compliment to BLB. For example, the value 1 to be written in SRAM by providing 1 to BL and 0 to BLB.
4. The data is written In SRAM cell while WL=0 i.e., WL is deactivated by changing latch status

C. Read Operation

- SRAM is able to communicate data which is stored.
- NM3 and NM4 (access transistors) activated while WL=1
- Read operation will be performed while both bit lines value precharged to1 and one is precharged and other is discharged to gnd. Therefore, if BL charged, BLB discharged with vice versa.

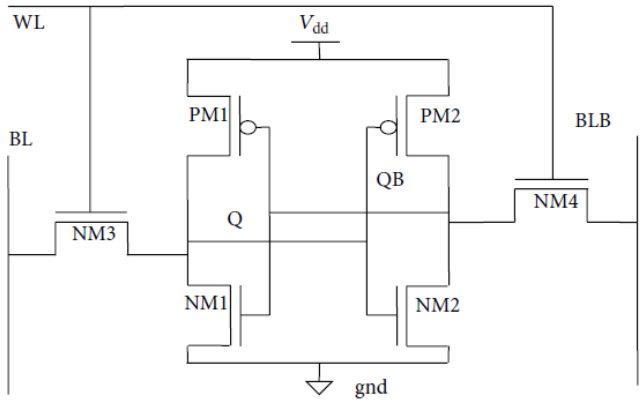


Figure 1: Basic Cell 6T SRAM cell.

III. FINFET WITH DOUBLE GATE BASED SRAM CELL

The proposed FinFET with double gate based SRAM is suitable to enhance better performance due to its fabrication and low power consumption, larger noise margins and better control of SCE without increasing the doping density and decreasing thickness of gate oxide. Increasing the height of the FinFET tends to V_{dd} reduction that leads to robust stability in SRAM with considerations of variations.

The proposed FinFET with double gate based SRAM operates in different modes as follows;

i. Tied Gate
ii. Independent Gate
iii. Low power
iv. Independent Gate

A. Tied Gate Mode

In this mode FinFET NMOS have access by enabling WL and back to back connections in both inverters. It reduces SCE as well as leakage but increases some extent in e delay while write and read operations. Hence, it is required the SRAM with reduction in size by reducing the transistors size but it tends to higher leakage and area of the cell.

B. Independent Gate Mode

In this mode gate opposite sides in pullup transistors are kept independent and controlled by biasing with multithreshold voltages hence to reducing the transistors. The opposite gates tied each other in pulldown transistors. To overcome the difficulty from the mechanism of direct accessing of data in read operation, presented a latch with reduced size of the transistor. However, it raises robust stability for SRAM. WL=0 tends to SRAM in standby and latch is maintained for stored bit. WL=1 while BLB and BL connected to V_{ss} and V_{dd} in read operation. NM1 and NM3 make the BL to discharge while 0 stored in Q node. Simultaneously, NM2 and NM4 make the BLB to discharge while 0 stored in QB node.

Therefore, NM4 and NM3 acts like high value V_{th} devices where it draws lower current consumption ability hence production of current by them is reduced comparison with Tied Gate mode. WL=1 on write operation have performed. Charging of BLB and discharging of BL makes the NM3 to conduct and passed 0 to SRAM at Q node. Simultaneously, Charging of BL and discharging of BLB makes the NM4 to conduct and passed 0 to SRAM at QB node, presented in figure 2.

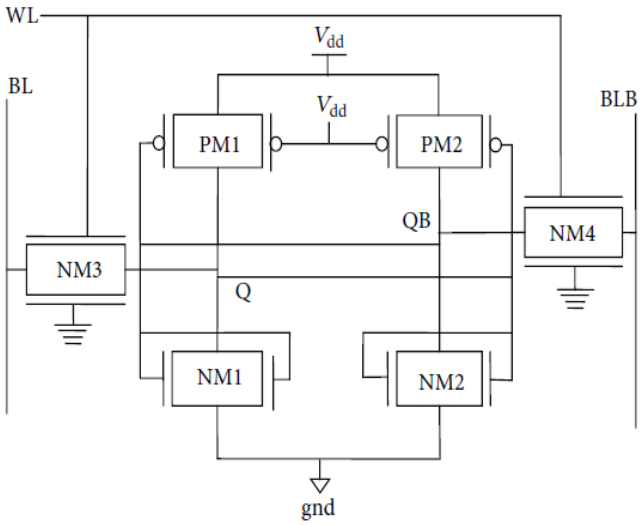


Figure 2: FinFET with independent gate SRAM cell

IV. LEAKAGE CURRENT COMPONENTS

There are three major considerable components for leakage.

A. Subthreshold leakage

B. Gate leakage
C. Junction Tunneling leakage

A. Subthreshold Leakage

Subthreshold leakage currents mainly considered which are generated by SCE where subthreshold leakage generates while $V_{th} > V_{gs}$ [7].
In the subthreshold system, drain current is given by

$$I_d \propto \exp\left(\frac{V_{gs}}{nV_T}\right), \quad (1)$$

And

$$V_T = \frac{kT}{q}. \quad (2)$$

Where
VT=Temperature voltage,
k = Boltzmann constant
T=Absolute temperature
q=Electron charge

B. Gate Leakage

Gate leakage currents mainly considered which are generated by SCE which occurs when current passes gate to substrate via oxide layer and it is having three components;

- Gate to Source current (drain overlap): The leakage occurs while the state of the transistor is off and its leakage is less compared to gate to channel
- Gate to Channel current: The leakage occurs while the state of the transistor is on
- Gate to Substrate current: Comparatively with other leakages, is small

In off state gate leakage draws less leakage than on state.

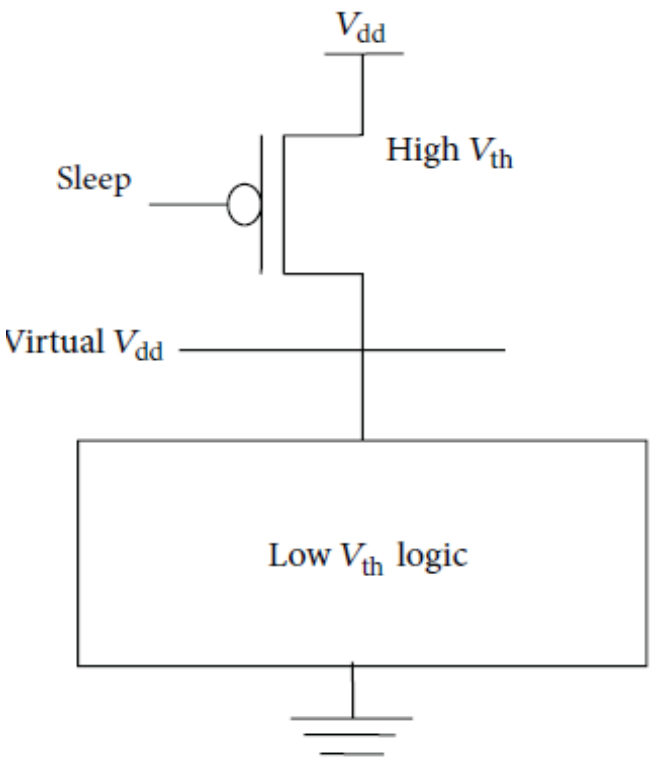
C. Junction Tunneling Leakage

It occurs while PN junction is in reverse bias with two different components and it is comparatively very small leakage.
1. Minority carriers diffusion at depletion edge
2. Pair of hole and electron generation in depletion

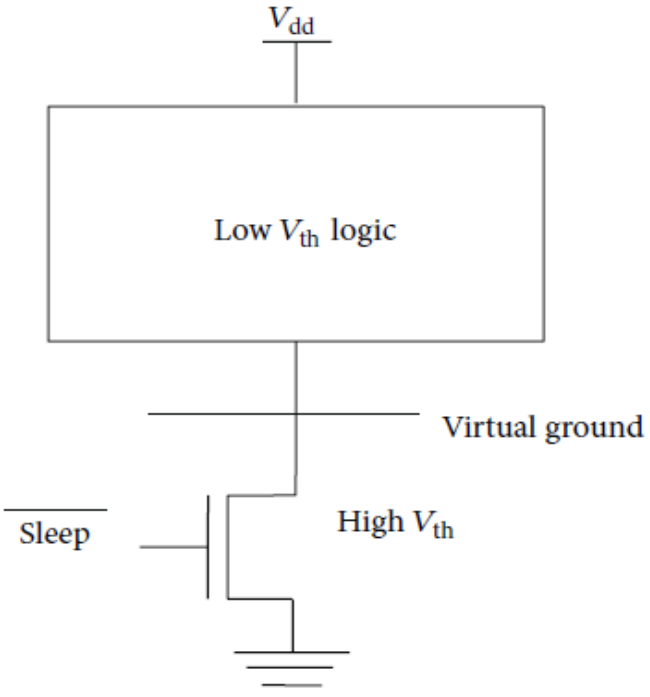
IV.PROPOSED REDUCTION TECHNIQUES

A. Multithreshold Voltage

In Figure 3, shows the multithreshold voltage technique where sleep control of low V_{th} connected with high V_{th} circuit. SRAM cell obtain standard functionality while sleep transistor is on and in off state it gives enhanced leakage control. Hence, in this technique high V_{th} would be used to attain low leakage. Therefore, high V_{th} in sleepy transistor and low V_{th} in FinFET transistors for better performance are considerable. In figure 3 illustrated the techniques with high V_{th} and low by varying the channel length.



3(a): High V_{th} PMOS



3(b): High V_{th} NMOS

Figure 3: Multithreshold technique

B. Gated V_{dd}

This technique is used to reduce leakage by adding additional NMOS transistor that generates stacking effect which develops the significant impact on leakage by presence of transistors between bit lines and ground.. It occurs while on/off of the gated transistor on used and unused portion

respectively in SRAM. In this technique source and ground connected in between NMOS transistors. Alternately, source and V_{dd} connected between PMOS transistors. In active mode the gated V_{dd} is on and off in standby mode. During read operation should maintain the adequate transistor width to give isolation from leakage. In this technique provide better control on leakage for NMOS than PMOS due to reduction of width of the transistor on read operation presented in figure 4.

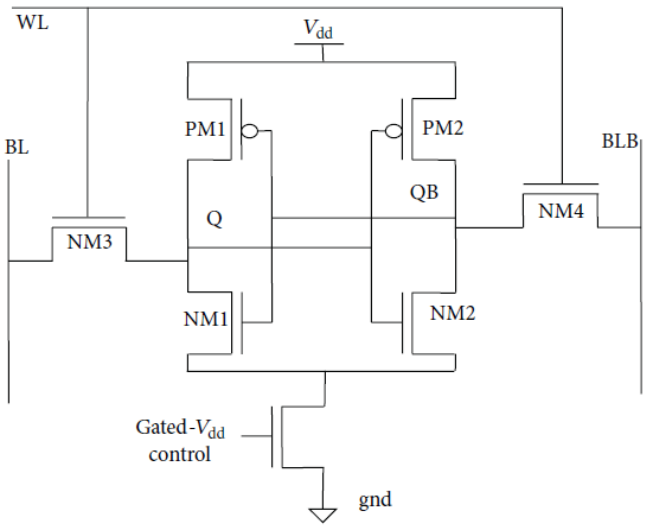
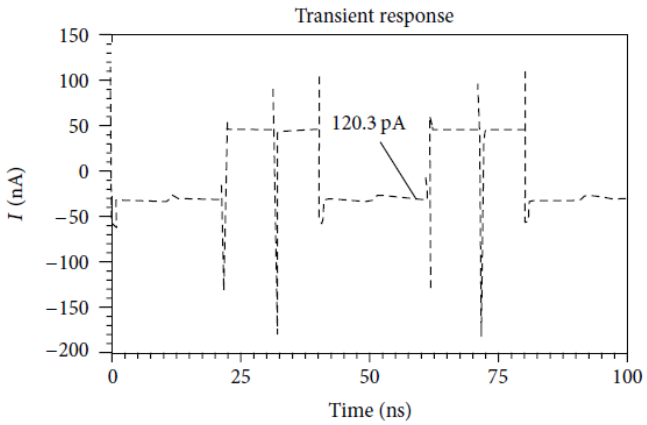


Figure 4: Gated V_{dd}

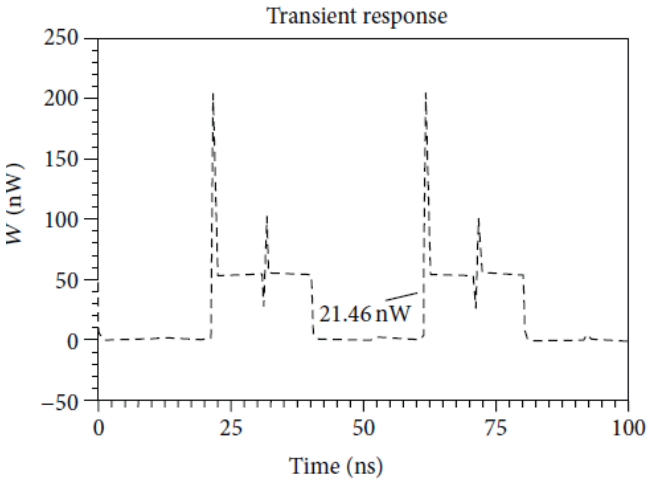
V. SIMULATION RESULTS

The simulation is carried out using by Cadence virtuoso in 45nm at 27º C. The Q output of SRAM cell depends on BL and QB on BLB while WL=1. In figure 5(a), shows the leakage current and figure 5(b) for leakage power in proposed FinFET with independent gate SRAM cell. Leakage current has been computed as 120.32 pA in 0 to 100 ns transitions and leakage power to 21.46 nW and observed reduction in leakage using multithreshold technique.

Standby mode simulation results are shown in figure 6(a, b) using high V_{th} PMOS technique and leakage has been drawn as 8.1 nW and 51.48 pA for leakage power and leakage current respectively.



5(a): Leakage current

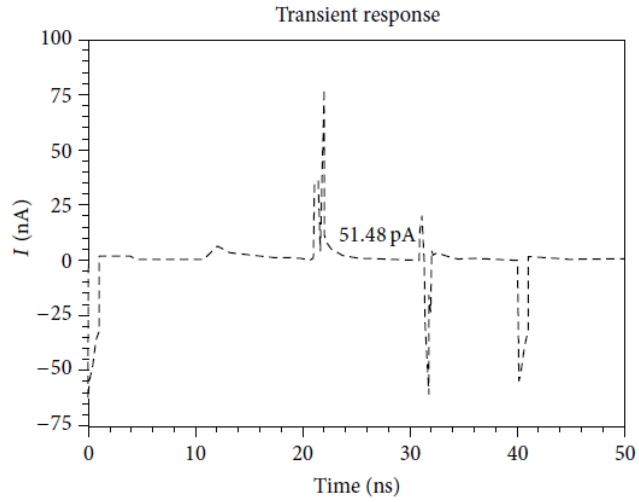


5(b): Leakage Power

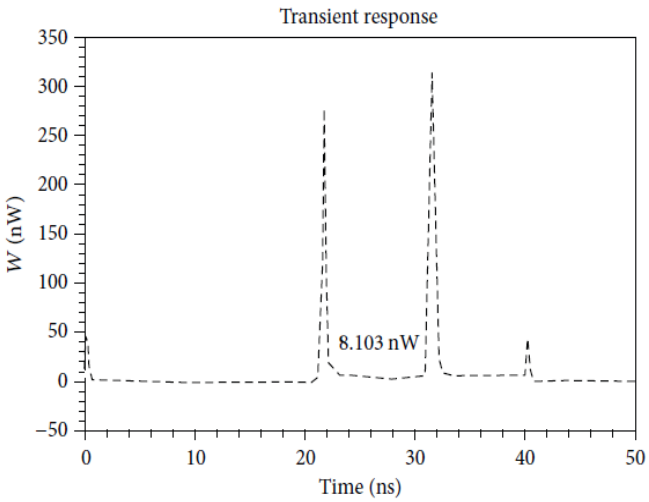
Figure 5: Leakage waveforms

High V_{th} NMOS leakage power and leakage current, simulation results are drawn and shown in figure 7(a, b) while sleep transistor is in off state. Leakage power and current has been noted to 20.6 nW and 51.9 pA respectively.

To generate the stacking effect gated V_{dd} is connected to FinFET with independent gate SRAM. Gated V_{dd} NMOS has been used where it is good for reducing leakage compared with PMOS. The additional gated V_{dd} is on off state while on unused portion with virtual ground. It is also noted the leakage current as 58.0 pA and leakage power as 20.65 nW. The total power reductions have shown in figure 8(a, b). Graphical representations of leakage have been shown in figure 9 with proposed techniques where figure 10 shows various techniques with same parameters.

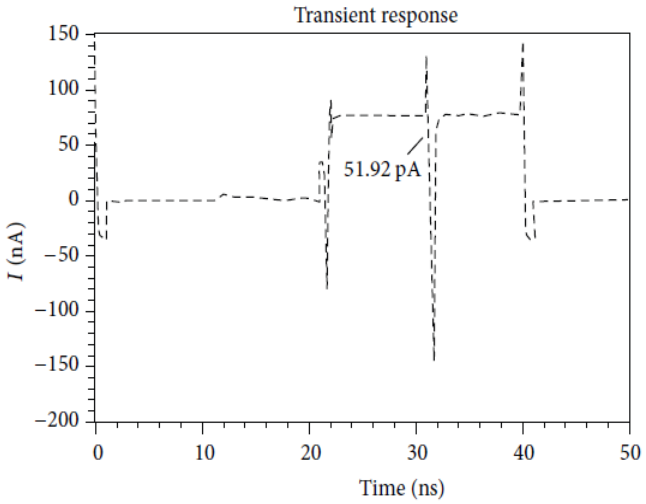


6(a): Leakage Current

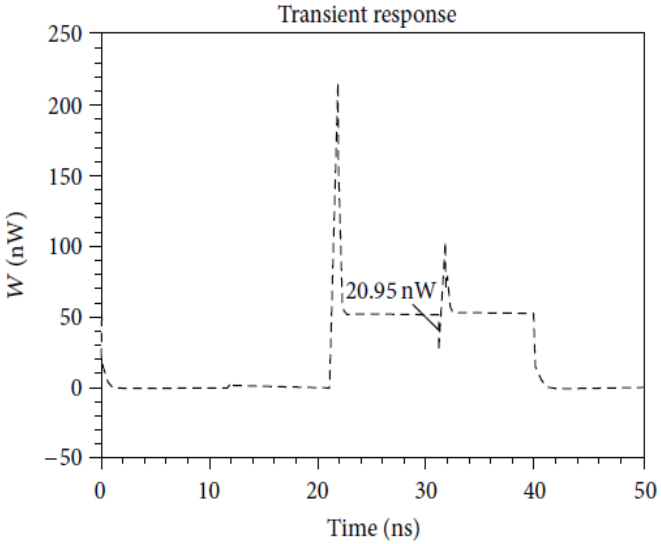


6(b): Leakage Power

Figure 6: High V_{th} PMOS waveforms

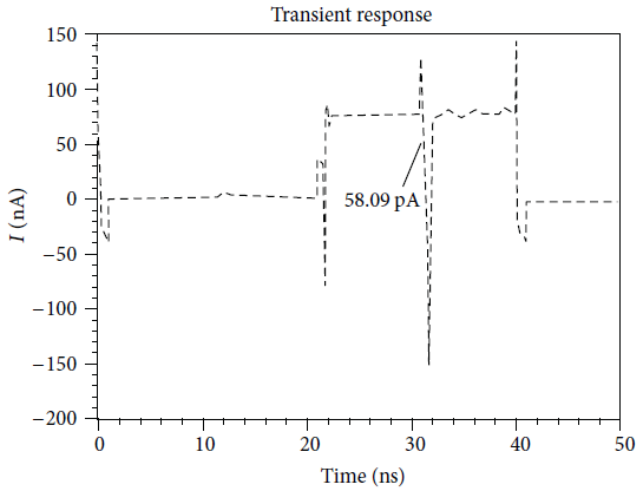


7(a): Leakage Current

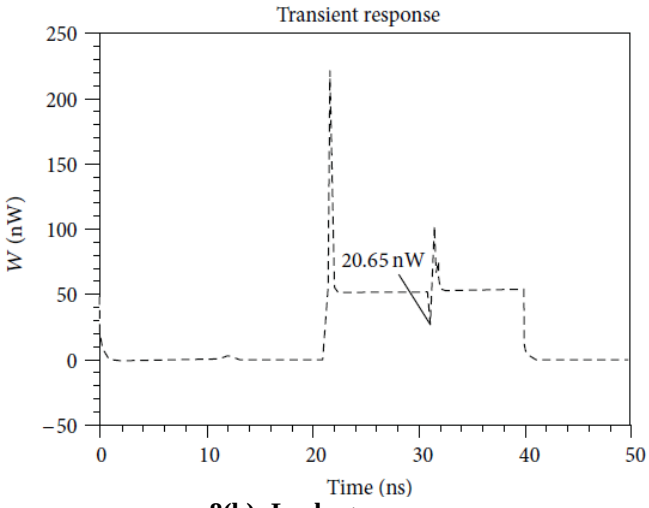


7(b): Leakage power

Figure 7: High V_{th} NMOS waveforms



8(a): Leakage Current



8(b): Leakage power

Figure 8: Waveforms for Gated V_{dd} technique

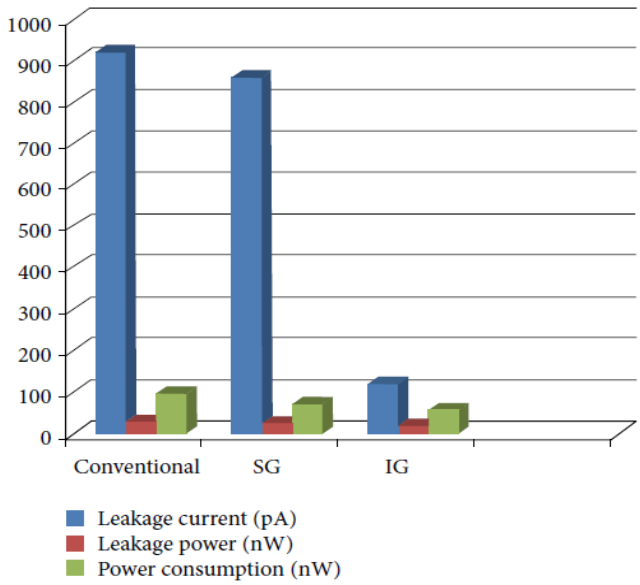


Figure 9: Graphical Representation

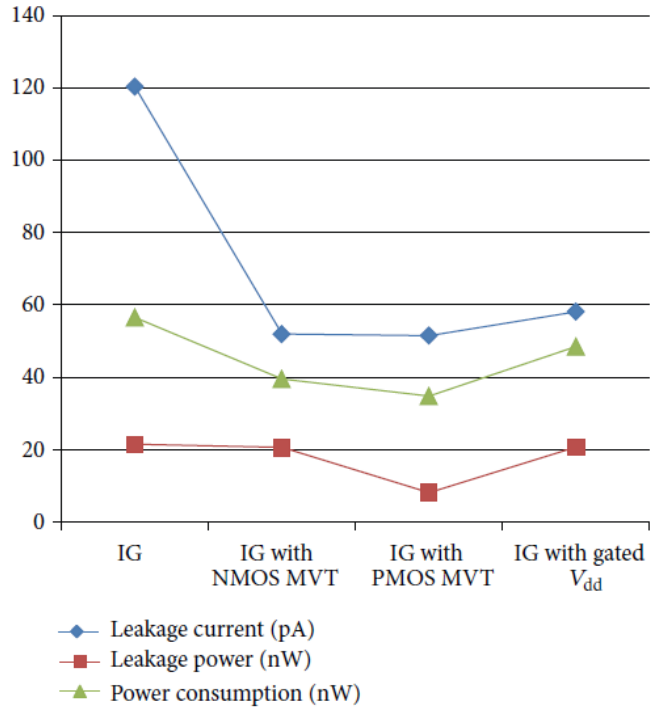


Figure 10: Comparative graphical representation

VI. CONCLUSION

Since SRAM cell is occupied in the area of about 90% in SoC, for efficient performance reduced leakage and power consumption is desirable. The results are simulated, illustrated the reduction of leakage current and power has been reduced to 94% using the FinFET with independent gate and proposed techniques compared by conventional MOSFET**.** Leakage current using high V_{th} NMOS has been reduced to 30% , 75% in high V_{th} PMOS and upto 25% in gated V_{dd} technique. However, leakage power using high V_{th} NMOS has been reduced to 95%, 94% in high V_{th} PMOS and 93% in gated V_{dd} technique. Therefore, it is observed that multithreshold voltage has strong on leakage control than gated V_{dd}. Finally, the proposed multithreshold technique is suitable for designing of IC as it consumes less power by proving reduced leakage.

References

[1] Chin E, Dunga M. Nikolic B. 2006. Design trade-offs of a 6T finFET SRAM cell in the presence of variations: In *Proceedings of the IEEE Symposium on VLSI Circuits*. 11, pp. 445-449.

[2] Kursun V. Tawfik S. 2007. Low power and stable finFET SRAM with static independent gate bias for enhanced integration density: In *ICECS procedings*. pp. 443-446.

[3] Fried D.M. 2004. *The Design, Fabrication and Characterization of Independent-Gate Finfets*: CornellUniversity.

[4] Gupta D. C. and. Raman A. 2012. Analysis of leakage current reduction techniques in SRAM cell in 90 nm CMOS technology: *IJCA*, 50(19).

[5] Mohanram K. and Rostami M. 2010. Novel dual-Vth independentgate FinFET circuits: in *Proceedings of the 15th Asia and South Pacific ASPDAC proceedings*, pp. 867-872.

[6] Mahmoodi Meimand H. Mukhopadhyay S. and Roy K. 2003. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits:*IEEE proceedings*, 91(2), pp. 305-327.

[7] Kursun V and Tawfik S. 2008. Portfolio of finFET memories: innovative techniques for an emerging technology: in *Proceedings of the ISOCC proceedings*, pp. I101-I104.

[8] Dasgupta S. Raj B. Saxena A. K. 2011. Nanoscale finFET based SRAM cell design: *IEEE C and S Magazine*, vol. 11(3), pp. 38-50.

[9] Jani R. Chaudhari U. 2013. A Study of circuit level leakage reduction techniques in cache memories: *International Journal of Engineering Research and Applications*, 3(2), pp. 457-460.

[10] Bhatt K. R., Jani R. Patel S. R.. 2013. Leakage current reduction techniques in SRAM: IJERT, 2(1).

[11] www.hindwai.com/journals