

HCI Degradation Effect on VDMOS Transistor with Geometric and Process Variations

H.H.M. Yusof

Lecturer, Faculty of Electronic and Computer Engineering, Universiti Teknikal Malaysia Melaka,
Hang Tuah Jaya, 76100 Malacca, Malaysia haziezol@utem.edu.my

N. Soin,

Associate Professor, Faculty of Engineering, University of Malaya. 50603 Kuala Lumpur, Malaysia. norhayatisoin@um.edu.my

W.B. Murti

Student, Faculty of Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia ubay0520@gmail.com

Abstract

In high power systems, the application of transistor has significantly increased and this includes the important of VDMOS type of transistor. However, reliability issues have always been addressed in high voltage and current operated applications. In order to counter this issues, various studies and analysis have been carried out till today. One of the well-known critical issue is known as Hot Carrier Injection (HCI). HCI happens due to high electrical field between source and drain of transistor. Therefore, several process parameters need to be understood before designing a transistor. Therefore, this paper aims to analyze HCI effect on the parameters of the transistor fabrication process which includes the geometric and process variations. In order to meet the objective, a high voltage VDMOS structure has been virtually fabricated in this work. This work results in a relationship among doping concentration, transistor material characteristics and geometrical variation.

Keywords: Reliability, High Power MOSFET, Hot Carrier Effect, HCI

Introduction

Since the application of Vertical Diffusion Metal Oxide Semiconductor (VDMOS) transistor tends to be used in high voltage and high current application, the reliability issue regarding this operation is concerned. One of the key reliability issue that occurs is the Hot Carrier Injection (HCI). Works on HCI in VDMOS transistor are less in number compared to other MOSFET devices. VDMOS transistor is diffused twice and it has a low doping drift region that exhibits high blocking voltage. Considering the reliability effect of p-channel VDMOS in 2012, Prijić *et.al* worked on Negative Bias Temperature Instability (NBTI). But, still there are scopes to work on the behavior of HCI in VDMOS [1]. The effect of HCI on VDMOSFET has been explained [2] but it emphasis on high voltage application. Threshold voltage (V_{th}) shift in VDMOS transistor due to bias temperature instability (BTI) has been demonstrated by Moens *et.al* but it has not considered the HCI effect [3]. This work is targeting

to relate the fabrication process parameters toward the hot carrier injection in VDMOS transistor since different process parameters such as oxide thickness, dielectric material, P-base doping concentration, N+ substrate doping concentration and N+ source doping concentration impact the reliability of VDMOS transistors. Also, it will define the critical parameters that influence the hot carrier injection. The relation between fabrication process parameters toward the HCI in VDMOS transistor can guide us to develop more advance structure with lesser reliability issues in future.

Device Simulation Conditions

Figure 1 shows the block diagram for the methodology of this research. In this research, we have made a comparison of processing parameters impact on both device characteristics and hot carrier effect (HCE). The comparison is based on oxide thickness by using silicon dioxide (SiO_2); different dielectric material in which silicon oxynitride (SiO_xN_y) is used; P-base doping concentration using Boron as dopant; N+ substrate doping concentration with phosphorous and N+ source doping concentration using Arsenic.

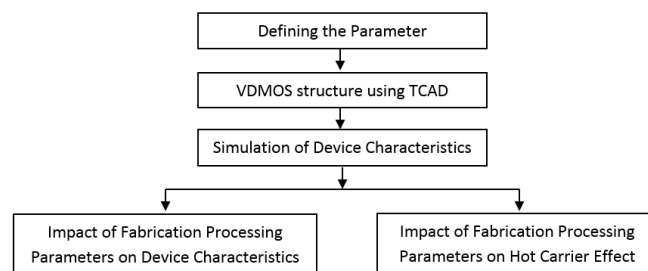


Fig.1. Methodology Block Diagram

Table 1 presents the parameters of the virtually fabricated VDMOS using Silvaco. The fabrication process is virtually done by TCAD Silvaco software and the characterization of the parameters and HCI is done by using ATHENA. Figure 2 shows the cross-sectional view of the VDMOS structure. The

HCI characterization is done by stressing the device at periodic time; 0.1 s, 0.1 s, 1 s, 1000 s and 10000 s.

TABLE.1. Parameters value of VDMOS structure

Parameter (Symbol)	Material/ Impurities	Value
Cell width (W _{cell})	Silicon	20 x 10 ⁻⁶ m
Gate width (W _G)	Polysilicon	14 x 10 ⁻⁶ m
Oxide thickness (t _{ox})	Silicon Dioxide	60 x 10 ⁻⁹ m
Channel length (L _{CH})	Boron	0.94 x 10 ⁻⁶ m
P-base junction depth (x _{jp})	Boron	1.94 x 10 ⁻⁶ m
N-drift region thickness (t _D)	Phosphorus	2.74 x 10 ⁻⁶ m
N+ substrate thickness (t _{sub})	Phosphorus	1.32 x 10 ⁻⁶ m
Doping concentration of N+ source (N _{N+})	Arsenic	3.5 x 10 ¹⁹ cm ⁻³
Doping concentration of P-base (N _P)	Boron	3.0 x 10 ¹⁷ cm ⁻³
Doping concentration of N-drift region (N _D)	Phosphorus	1.0 x 10 ¹⁵ cm ⁻³
Doping concentration of N+ substrate (N _S)	Phosphorus	1.0 x 10 ¹⁸ cm ⁻³

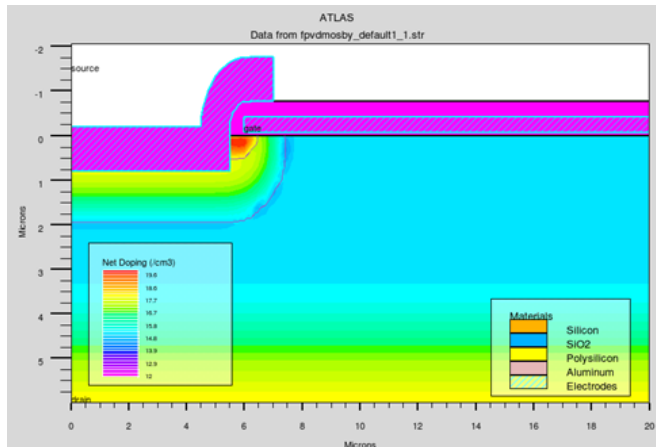


Fig.2. Cross-sectional of the fabricated VDMOS structure

Result and Analysis

A. Impact of Oxide Thickness on Device Characteristics without HCI Stress Test

This investigation is start by using silicon dioxide (SiO₂) as the dielectric material of the device. Figure 3 shows the linear relationship of the threshold voltage with oxide thickness.

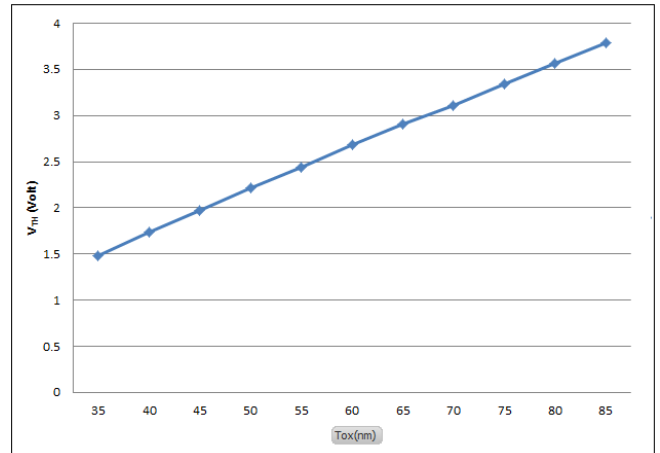


Fig.3. Plotted graph of t_{ox}/V_{TH} for SiO₂

The linear relation of threshold voltage with oxide thickness is consistent with equation (1) where the threshold voltage is defined by [4]:

$$V_{TH} = \frac{t_{ox}}{\epsilon_{ox}} \sqrt{4\epsilon_s k T N_P \ln \left(\frac{N_P}{n_i} \right)} \quad (1)$$

So it can be concluded that the threshold voltage change linearly with the change of oxide thickness.

B. Impact of Oxide Thickness on HCI Stress Test

The degraded threshold voltages are plotted in Figure 4. It shows that the degradation levels of different oxide thickness are almost the same level.

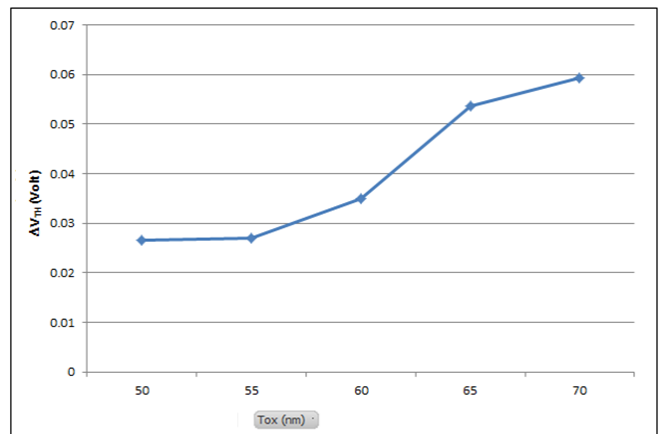


Fig.4. Plotted graph of t_{ox}/ΔV_{TH} for SiO₂

From the simulation results it can be concluded that the higher oxide thickness produces the higher threshold voltage degradation due to higher electrical field. This will lead into hot carrier injection and tend to make larger threshold voltage shifting.

For a device with silicon dioxide as dielectric material, increasing the oxide thickness will increase the interface trap density [5-7]. The gate of the device induced drain leakage current I_{gidl} as the effect of the oxide thickness and this explained by the equation (2).

$$I_{gidl} = A \cdot E_s \exp\left(\frac{-B}{E_s}\right) \quad (2)$$

where A and B are constants

$$A = \frac{q^2 \cdot m_r^{1/2}}{18 \cdot \pi \cdot h^2 \cdot E_{gap}^{3/2}}$$

$$B = \frac{\pi \cdot m_r^{1/2} \cdot E_{gap}^{3/2}}{2\sqrt{2} \cdot q \cdot h} = 21.3 \text{ MV/cm}$$

And E_s is the surface electric field given by

$$E_s \approx \frac{V_{gd} - 1.2}{3T_{ox}} \quad (3)$$

Thus, it is clear from equation (2) and (3) that I_{gidl} has direct relationship with HCI and oxide thickness. The incremental of oxide thickness will lead to worst performance against hot carrier injection. However, in order to mitigate HCI, electron from outside is pumped and trapped into dielectric. This trapped electron exaggerates the shift in I_{gidl} and hence influences the HCI.

C. Impact of Dielectric Material on Device Characteristics without HCI Stress Test

Silicon oxynitride has higher dielectric constant which is $7.5 \epsilon_0$ compared to silicon dioxide where the dielectric constant is $3.9 \epsilon_0$. The higher dielectric constant has been studied and used as a better material for gate dielectric [8]. Figure 5 shows the oxynitride resulting lower threshold voltage. This is proved by equation (1) where the dielectric constant has an inversely proportional relation toward threshold voltage.

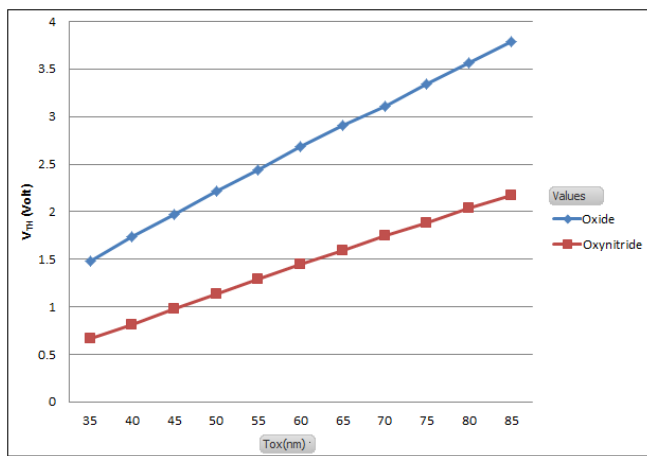


Fig.5. Plotted graph of t_{ox}/V_{TH} with different dielectric material

Compare to silicon dioxide, silicon oxynitride has lower energy bandgap. The energy bandgap has a proportional relation toward threshold voltage [9], therefore for dielectric material with higher dielectric constant produces lower threshold voltage as the energy bandgap is also lower.

D. Impact of Dielectric Material on HCI Stress Test

Simulation is done by varying the oxide thickness for different dielectric material from its default value of 60 nm. The device structure is then followed by stress test. The degraded threshold voltages are plotted in Figure 6. It shows the

threshold voltage for gate material with higher dielectric constant has smaller threshold voltage.

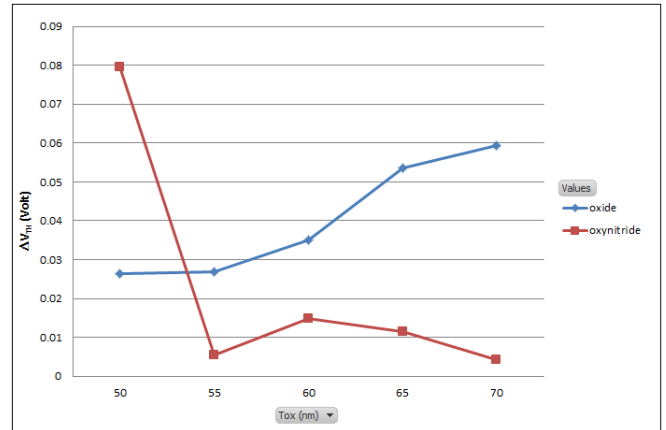


Fig.6. Plotted graph of $t_{ox}/\Delta V_{TH}$

Figure 5 also shows that in higher dielectric constant, higher oxide thickness creates smaller the threshold voltage shifting caused by hot carrier injection (not increasing as in lower dielectric constant).

E. Impact of P-Base Doping Concentration on Device Characteristics without HCI Stress Test

The boron material is used in the diffusion process of P-Base at different levels of concentration. Figure 7 shows the plotted threshold voltages are increased along the incremental of P-base doping concentration level.

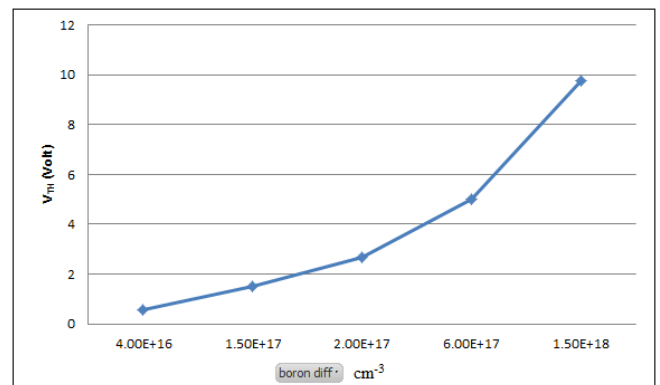


Fig.7. Plotted graph of N_P/V_{TH}

The relation between threshold voltage and P-base doping concentration is not a linear relation, as shown in equation (1) where the threshold voltage is proportional with the square root of P-base doping concentration.

F. Impact of P-Base Doping Concentration on HCI Stress Test

This investigation is done by varying the boron concentration from the process simulation. The boron concentration run in

process simulation will give a different concentration in device structure due to the diffusion process. The degraded threshold voltages are plotted in Figure 8. It shows that threshold voltage variance for this investigation is large. Also, the threshold voltage increases as the P-base doping concentration increase.

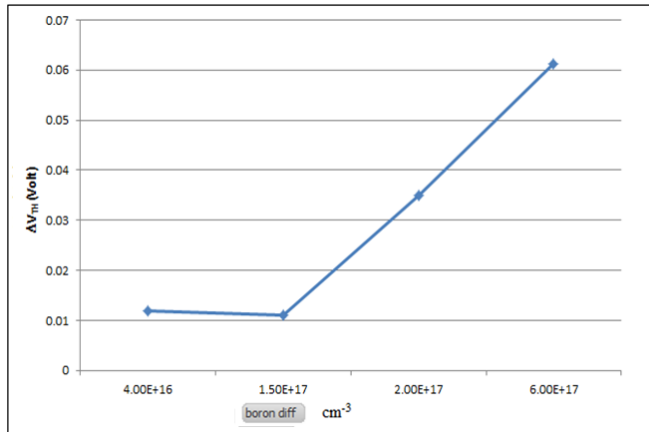


Fig.8. Plotted graph of $N_P/\Delta V_{TH}$

G. Impact of N+ Substrate Doping Concentration on Device Characteristics without HCI Stress Test

This simulation is done by varying the phosphorus concentration level in the N+ substrate doping process. Figure 9 shows the N+ substrate doping concentration has a linear relation toward threshold voltage, as the N+ substrate doping concentration increase the threshold voltage is also increase.

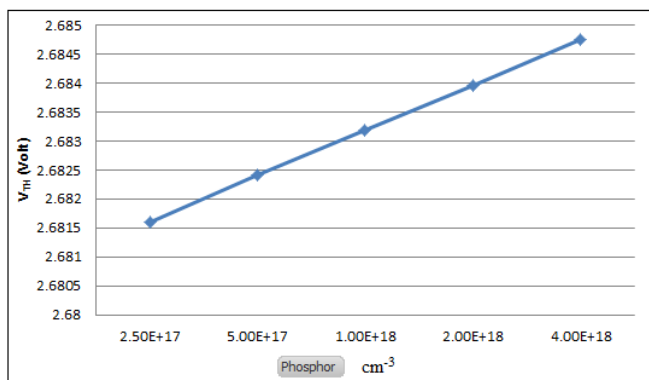


Fig.9. Plotted graph of N_S/V_{TH}

The threshold voltage variation is less than 1 %. Because of the less significant contributions in threshold voltage calculation, the threshold voltage is modeled without the N+ substrate doping concentration.

H. Impact of N+ Substrate Doping Concentration on HCI Stress Test

Figure 10 shows the plotted extracted value of simulation results. It shows a sudden threshold voltage shifting drop in the default value. But overall with the increase of N+ substrate

doping concentration the degraded threshold voltage caused by hot carrier injection is almost constant. So it can be concluded that the N+ substrate doping concentration does not have significant impact on hot carrier injection.

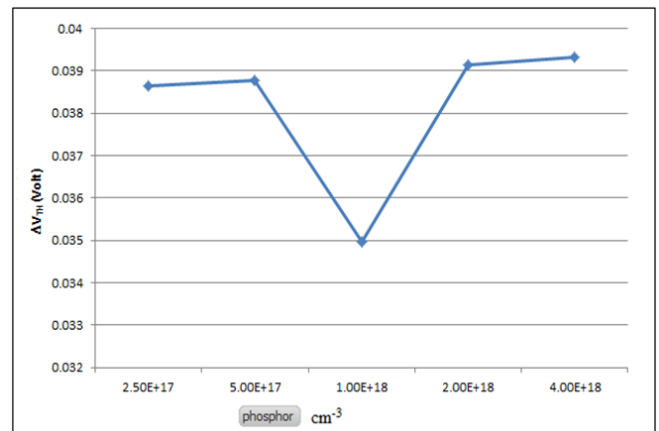


Fig.10. Plotted graph of $N_S/\Delta V_{TH}$

I. Impact of N+ Source Doping Concentration on Device Characteristics without HCI Stress Test

Simulation is done by varying the arsenic concentration level of the N+ source doping. This dopant has the same treatment as the boron concentration in P-base which is the double diffusion process.

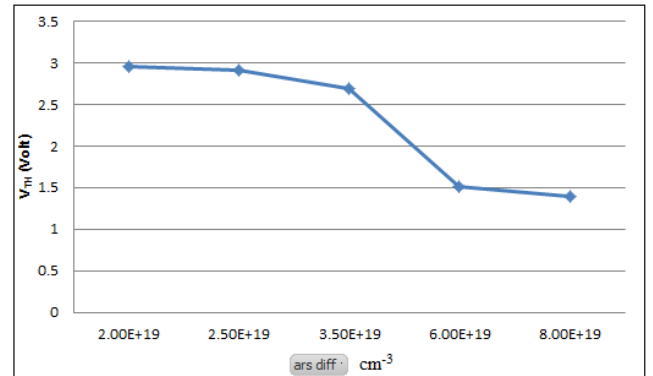


Fig.11. Plotted graph of N_{N+}/V_{TH}

The results in Figure 11 show that the variation of N+ source doping concentration are causing significant variation in threshold voltage of the device. The relation is inversely proportional where the higher N+ source doping concentration creates smaller threshold voltage.

J. Impact of N+ Source Doping Concentration on HCI Stress Test

Figure 12 plotted the extracted values of the simulation result. It shows the maximum degradation is on the highest N+ source doping concentration. So it can be concluded that the N+ source doping concentration has a proportional relation

toward threshold voltage degradation caused by hot carrier injection.

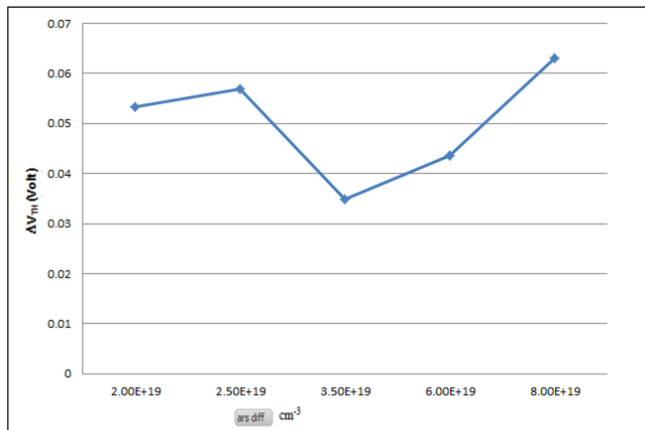


Fig.12. Plotted graph of $N_+/\Delta V_{th}$

Conclusion

In this paper, a high voltage VDMOS structure has been virtually fabricated. The device is simulated to find its basic characteristics. Five parameters including the thickness of the oxide, the dielectric material, N+ source doping concentration, P-base doping concentration, and N+ substrate doping concentration were analyzed to investigate the impact of the geometric and process variations toward device characteristics and toward the HCI in the device.

Threshold voltage of the device is significantly influenced by oxide thickness, N+ source doping concentration and P-base doping concentration. Oxide thickness and P-base doping concentration have a proportional relationship toward threshold voltage value of the device. N+ source doping has inverse relationship with threshold voltage where the relationship could be led by double diffusion technology that the N+ source doping concentration influence the graded doping profile of P-base doping concentration.

Dielectric material with higher dielectric constant can be used to improve the device performance against HCI in the device. It has been proved in this work that the higher dielectric constant has less threshold voltage degradation rate due to HCI.

Acknowledgement

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