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Horizontal and Vertical Packet Combining Scheme with maximum erroneous bits limit: Proposal and study

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Abstract
When a channel is error prone, error correction would likely result in better throughput compared to retransmission. Too many retransmissions in error-prone wireless environments not only create potential latency but also limit the overall bandwidth capacity. In general, an erroneously received packet is likely to possess some useful information, by which receivers can derive the original packet from a number of erroneously received copies. The issues of limited resources of wireless communication network lead to a pressing need for simple, efficient protocols and algorithms that can maximize the use of available resources in an energy efficient manner. The throughput of error correction codes is the main reason favoring in storage devices, digital subscriber lines and wireless communication and the simplicity and high error correction capability over noisy channels of packet combining scheme is the main reason for selection. So in this paper, an improved packet combining scheme with implementation of simple (7,4) Hamming code for horizontal checking and traditional packet combining scheme with maximum erroneous bits limit for vertical checking is proposed for better error correction and better throughput at the same time efficiently utilizing limited resources. Performance evaluation confirm that the proposed mechanism can significantly reduce average number of copies per packet, also reducing latency at the same time, thus increasing throughput and correction capability as compared to the existing packet combining mechanism.

Keywords: Hamming code, error correction, error detection, wireless channel, throughput, retransmission, packet combining scheme.

Introduction

Coding theory is concerned with reliability of communication over noisy channels. Error correcting codes are used in a wide range of communication systems from deep space communication, to quality of sound in compact disks and wireless phones. Digital data is transmitted over a channel (which could be a wire, network, space, air etc.) and there is often noise in the channel. The noise may distort the messages to be sent. Therefore, what the receiver receives may not be the same as what the sender sends. The goal of coding theory is to improve the reliability of digital communication by devising methods that enable the receiver to decide whether there have been errors during the transmission (error detection) and if there are, to possibly recover the original message (error correction)[1]. Data that is transmitted over a communication channel can be scratched; their bits can be masked or inverted by noise. To get rid of retransmitting the data we need to detect and correct the errors in the data. Some simple codes can detect but not correct errors [2, 3]; others can detect and correct one or more errors. The throughput of error correction codes is the primary motivation for favoring in storage devices, digital subscriber lines and wireless communication and the simplicity and high error correction capability over noisy channels of packet combining scheme is the main reason for selection. In 1950, Hamming introduced a single error correcting and double error detecting codes with its geometrical model [4]. In coding theory, (7, 4) Hamming is a linear error-correcting code that encodes four bits of data into seven bits by adding three parity bits. It is a member of a larger family of Hamming codes. Hamming's (7,4) algorithm can correct any single-bit error, or detect all single-bit and two-bit errors. In other words, the minimal Hamming distance between any two correct codewords is 3, and received words can be correctly decoded if they are at a distance of at most one from the codeword that was transmitted by the sender. This means that for transmission medium situations where burst errors do not occur, Hamming's (7, 4) code is effective (as the medium would have to be extremely noisy for two out of seven bits to be flipped) and for codeword to have two bits flipped out of seven bits, the medium would have to be extremely noisy of the order of 10^-3 to 10^-2. And in practical, channel does not happen to be extremely noisy all the time. That is why the simplest (7, 4) Hamming code which can correct single bit and detect double bit errors are selected for this study.

In order to achieve the desirable quality in high bit error rate wireless channels, several modifications for applying basic ARQ are found in literature where erroneous packets are combined and by applying logic, the error location is identified. Once error location is identified, bit inversion is done to error locations (Brute method). The technique is variably applied in Packet combining scheme. Packet combining [5] is a simple and elegant scheme of error correction in transmitted packet. In Packet combining scheme two copies of the erroneous packet are XORed bit-wise to locate the error position. On identification of errored location, receiver may apply brute force method for bit inversion to correct the errors. In conventional Packet combining scheme, if the first received copy is erroneous receiver will request for retransmission for next copy retaining the first erroneous copy without trying to correct the first received copy. But in the proposed study, transmitter will send the Hamming coded copy of the packet initially and at the receiver side error detection is done. If single error is there then it is corrected and for more than single error, receiver request for retransmission retaining the erroneous copy in its buffer. Thus, in this paper, an improved packet combining scheme is proposed which extract the advantages of high throughput of simple (7, 4) Hamming code and high error correction of traditional packet combining scheme. The (7, 4) Hamming code is implemented for horizontal checking and traditional packet combining scheme for vertical checking, at the same time efficiently utilizing limited resources. Since Hamming codes are perfect codes, that is, they achieve the highest possible rate for codes with their block length and minimum distance of three.

Related Work

A. Review of (7, 4) Hamming code:

Hamming code [6] is well known for its single-bit error detection & correction capability. Hamming codes can detect up to two-bit errors or correct one-bit errors without detection of uncorrected errors. Hamming code is based on the principle of adding 'r' redundancy bits to 'n' data bits such that $2^r \geq n+r+1$. To guarantee correction upto't' errors in all cases, the minimum Hamming distance in a block must be $d_{min}=2t+1$. The (7, 4) Hamming code that can correct a single-bit error which is detected with the help of parity/check bits and detects double bit errors has $d_{min}=3$. In mathematical terms, Hamming codes are a class of binary linear codes. For each integer $r \geq 2$ there is a code with block length $n = 2^r - 1$ and message length $k = 2^r - r - 1$. Hence the rate of Hamming codes is $R = k / n = 1 - r / (2^r - 1)$, which is the highest possible for codes with minimum distance of three (i.e., the minimal number of bit changes needed to go from any code word to any other code word is three) and block length $2^r - 1$. And large rate means that the amount of actual message per transmitted block is high. In this sense, the rate measures the transmission speed and the quantity $1-R$ measures the overhead that occurs due to the encoding with the block code. The Hamming single-bit correction code is implemented by adding check bits also called parity bits to the output message according to the following pattern [7]:

i) The message bits are numbered from left to right, starting at 1.
ii) Every bit whose number is a power of 2 (bits 1, 2, 4, 8,…) is a check bit.
iii) The other is the output message bits (bits 3, 5, 6, 7, 9,…) contain the data bits, in order.

Each check bit establishes even parity over itself and a group of data bits and can be found with the help of Ex-OR operation [6].

A data bit is in a check bit's group if the binary representation of the data bit's number contains a 1 in the position of the check bit's weight. For instance, the data bits associated with check bit 2 are all those with a 1 in the 2's position of their binary bit number—bits 2, 3, 6, 7, and so forth.

Table 1. A Layout of Data and Check Bits for (7, 4) Hamming code:

Bit position	7	6	5	4	3	2	1
Bit number	111	110	101	100	011	010	001
Data bit	D4	D3	D2		D1		
Check bit				C4		C2	C1

C1 is a parity check on every data bit whose position is xx1
C1 = D1 xor D2 xor D4
C2 is a parity check on every data bit whose position is x1x
C2 = D1 xor D3 xor D4
C4 is a parity check on every data bit whose position is 1xx
C4 = D2 xor D3 xor D4

So 7-bit codeword generated is $D_4D_3D_2C_4D_1C_2C_1$. To find the value of check/parity bit, that which parity should be zero and which should be one, the Hamming bit at bit position 1 is selected such that there is even parity at bit positions 1, 3, 5, 7, the Hamming bit at bit position 2 is selected such that there is even parity at bit positions 2, 3, 6, 7 and the Hamming bit at bit position 4 is selected such that there is even parity at bit positions 4, 5, 6, & 7. Now the received codeword is compared to the transmitted codeword and error syndrome is generated as

S1= C1 xor D1 xor D2 xor D4
S2 = C2 xor D1 xor D3 xor D4
S3= C4 xor D2 xor D3 xor D4

If error syndrome is all zeros then no error occurs at the received codeword so no correction is required but if error syndrome is non-zero then correction is required and the value of error syndrome identifies the erroneous bit.

B. Review of Packet Combining (PC) scheme

Chakraborty et al in [8] suggested a simple technique where the receiver will correct limited error, one or two bit error, from the received erroneous copies. The PC scheme implemented with many existing backward error correction code with modifications is studied in [9, 10, 11, 12, 13 and 14]. Chakraborty's PC scheme is illustrated below:

(i) Packet Transmitted: 01010101
(ii) Packet received erroneously: 11010101 (First Packet)

The receiver requests for retransmission of the received erroneous packet but keeps in store the received erroneous packet. The transmitter retransmits the packet, but again the packet is received by the receiver erroneously as "00010101." Chakraborty proposed that the receiver can correct the error by using two erroneous copies by a bit wise XOR operation between erroneous copies, in the present example as follows:

First erroneous copy 11010101

Second erroneous copy 00010101

XOR 11000000

The error locations are identified as first and/or second bit from the left. Chakraborty suggested that the receiver apply bit inversion of the bit(s) in error location(s) one after another followed by the application of error decoding method in use. In the example the average number of brute application will be 0.5, and in general 2^{n-1} if n bits are found in error.

Proposed Horizontal and Vertical Packet Combining Scheme with maximum erroneous bits limit and analysis

In conventional Packet combining scheme, if the first received copy is erroneous (whether single bit or more) receiver will request for retransmission for next copy retaining the first erroneous copy without trying to correct the first received copy. Thus bandwidth is utilized in feedback path as well as in retransmitting the copy of the same packet. It also increases the latency of the system.

In this study, we propose horizontal and vertical packet combining scheme for better error correction, higher throughput and reduced latency. The operation and the block diagram of the proposed technique is as depicted in the fig. 1 and fig.2 [2]. Initially, the source node transmits a copy of the packet using (7, 4) Hamming code. Receiver performs error detection on the received copy and the following cases may happen:

i. If no error or single error is detected; receiver performs error correction using Hamming code and responds by sending acknowledgement (ACK) message.

ii. Error can occur in check bits or message bits. Since (7, 4) Hamming code has minimum distance of 3 which means it can detect two bit errors and can correct single-bit error. So single bit errors which occur in message bits are corrected using Hamming code and ACK is sent to the transmitter. If error occur in parity or check bits then no correction is required since check bits are introduced for redundancy and from established (7, 4) Hamming code it is known that every bit whose number is power of 2 is a check or parity bits.

iii. If double error is detected, then the receiver stores this erroneous copy and request for retransmission of the same packet by sending negative acknowledgement (NAK) messgae to the transmitter.

Now transmitter transmits normal copy of the same packet and at the receiver side, error detection is perform on the received second copy and if copy is received erroneously, receiver performs packet combining scheme using second received copy and the copy previously stored. And these two copies are XORed to get the error locations. Based on these bit locations, possible combinations of bits are applied to generate all possible candidates, one of which is likely to be the correct packet. Now apply CRC to determine correct packet. If the packet get corrected using PC scheme then ACK is sent to the transmitter and transmitter transmits the next packet using Hamming code.

Also to increase the efficiency or to reduce the complexity of the packet combining scheme, maximum limit of erroneous bit(s) locations are set, above which PC scheme cannot be implemented. The complexity of the bit inversion process to get correct copy is given by [13]:

$$C=2^{2n\alpha}-2 \quad (1)$$

Where n is the packet size, α is bit error rate.

Thus, even for medium-sized packets and at moderate BER, random fluctuations of the channel may make the bit inversion procedure extremely complex. To make the scheme implementable, an upper limit of computational complexity is defined. If the total number of "1's" in a XORed pair of erroneous copies exceeds, N_{max}, the pair is discarded, and either a new pair is chosen or a retransmission is sought. In this case, $P(i,j)$ is given by [13],

$$P(i,j) = 1 - \left[\frac{(n-i)!(n-j)!}{n!(n-i-j)!}\right] \quad \text{if } i+j \le N_{max} \quad (2)$$

$$= 1 \quad \text{if } i+j > N_{max} \quad (3)$$

Where $P(i,j)$ is the probability that two copies with i and j errors, respectively and n is the packet size.

The idea of setting maximum limit is to avoid unnecessary bit pattern searching which is being employed by the PC scheme which consumes most of the bandwidth and the time. Thus efficiency of the system is maintained.

The following analysis can be made for the proposed horizontal and vertical Packet combining scheme:

i.Unlike conventional PC where two erroneous copies of the packet is necessary to find the correct packet if the first copy is received with errors i.e. retransmission is requested for the same packet which logically means decreasing the throughput of the system, the proposed technique employ PC scheme only on demand basis if the Hamming decoding method fails. The aggregate numbers of packet being transmitted in the proposed packet combining scheme is lesser than that of conventional PC scheme. Assume a packet is made of N bits. For the suggested technique, total number of bits to be transmitted ={[N(first copy) + (3N/4)(check bits)]}=1.75N in lieu of 2N in PC if the first copy is received with an error. Since the number of bits transmitted for the proposed technique is lesser than the conventional Packet combining scheme, the throughput of the proposed packet combining scheme is higher than PC logically.

ii.Since horizontal checking is done using Hamming code on the received erroneous packet and vertical checking using conventional packet combining scheme so two-dimensional checking performed on single packet leads to better error correction as compared to the techniques where only Hamming code or only packet combining scheme is applied. It provides better correction capability as one bit error correction under each 4 bits block of the first copy is possible by the Hamming code followed by PC if the copy cannot be corrected by Hamming code method.

iii. Due to the setting of maximum limit of erroneous bit positions in this technique, complexity in searching correct bit patterns is reduced thus reducing time consumption and extra load of the system.

iv. One major advantage of the proposed technique is low latency. When (7,5) Hamming code corrects the erroneous copy in the first attempt of packet transmission only one propagation time (tp) or Round Trip Transfer (RTT) delay is used. One tp or RTT is at best needed for a corrected packet in horizontal and vertical packet combining (HVPC) scheme. Thus HVPC scheme doesn't add any extra delay to the transmission.

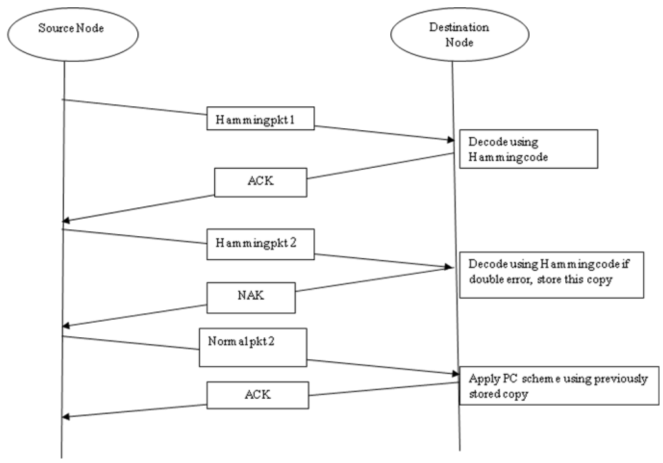

Fig.1. Proposed Horizontal and vertical Packet Combining Scheme

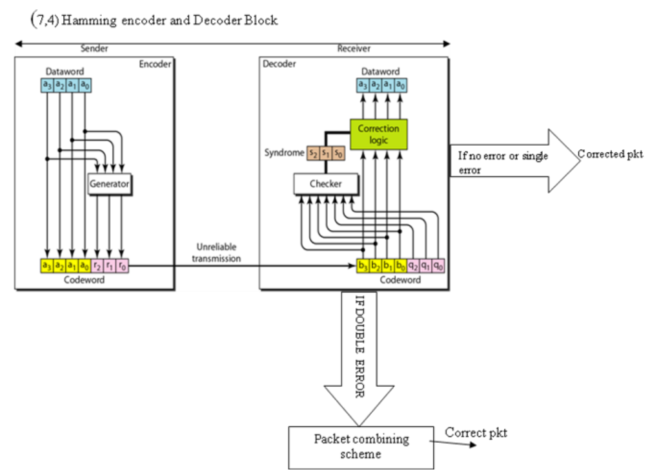

Fig.2. Proposed block diagram of Horizontal and Vertical Packet Combining scheme

Idea will be clearer after going through the examples:

i. Data to be transmitted is say 1010 so calculating check bits as

$C1=D1\oplus D2\oplus D4= 0\oplus 1 \oplus 1=0$

$C2=D1\oplus D3\oplus D4= 0\oplus 0 \oplus 1 =1$

$C3 =D2\oplus D3\oplus D4=1\oplus 0\oplus 1=0$

Transmitted codeword is $D_4D_3D_2C_4D_1C_2C_{1=}$ 1010010

At the receiver side, received codeword is say with one-bit flipped as 10**0**0010; a receiver detects presence of one bit error and calculates an error syndrome as

$S1=P1\oplus D1\oplus D2\oplus D4 = 0 \oplus 0 \oplus 0 \oplus 1=1$

$S2= P2 \oplus D1\oplus D3\oplus D4 = 1\oplus 0 \oplus 0 \oplus 1=0$

$S3=P4 \oplus D2\oplus D3\oplus D4 = 0 \oplus 0\oplus 0\oplus 1=1$

So error syndrome calculated is $S_3S_2S_1$=101 that means fifth bit from right is erroneous and the corrected codeword is 1010010 and again it goes to error detection and data sent from transmitter is $D_4D_3D_2D_1$=1010. Now receiver will acknowledge correction reception of data by sending back ACK packet to the transmitter.

<u>For double-bit error</u>

If the received codeword for the same example is say 1100010, receiver performs error detection and found to be double error. Receiver calculate new error syndrome as

$S1=P1\oplus D1\oplus D2\oplus D4= 0 \oplus 0 \oplus 0 \oplus 1=1$

$S2= P2 \oplus D1\oplus D3\oplus D4 = 1\oplus 0 \oplus 1\oplus 1=1$

$S3=P4 \oplus D2\oplus D3\oplus D4 = 0 \oplus 0\oplus 1\oplus 1=0$

So new error syndrome calculated is $S_3S_2S_1$=110 that is sixth bit from right is the erroneous bit and the corrected codeword is 1000010 and again it goes to error detection but since (7, 4) Hamming can only correct single bit so it cannot be corrected now and the received data with error is 1100. Now receiver responds by sending NAK to the transmitter, keeping erroneous copy say it copy1 in its buffer.

Transmitter transmits second copy of the same packet in normal form as 1010. At the receiver, it is received with an error as say 0010. Now receiver apply packet combining scheme using this received copy say called it copy2 and previously stored copy1 using Ex-OR operation to find the erroneous positions as

Copy1 =	1100
Copy2 =	0010
=	1110

Receiver detects the positions of erroneous bits and apply brute force to generate all possible candidates and all the generated candidates undergo error detection test and thus correct packet is received. Thus, horizontal checking using simple Hamming code and vertical checking using packet combining scheme done on single packet to get the correct one leads to two dimensional checking of packet which obviously leads to better error correction.

ii. Data to be transmitted is 1111, calculating check bits as

$C1=D1\oplus D2\oplus D4= 1\oplus 1 \oplus 1=1$

$C2=D1\oplus D3\oplus D4= 1 \oplus 1\oplus 1 =1$

$C3 =D2\oplus D3\oplus D4=1\oplus 1\oplus 1=1$

Transmitted codeword is $D_4D_3D_2C_4D_1C_2C_1$ =1111111

At receiver, received codeword is 0111111, it calculates error syndrome as

$S1=P1\oplus D1\oplus D2\oplus D4= 1 \oplus 1 \oplus 1 \oplus 0=1$

$S2= P2 \oplus D1\oplus D3\oplus D4 = 1\oplus 1 \oplus 1\oplus 0=1$

$S3=P4 \oplus D2\oplus D3\oplus D4 = 1 \oplus 1\oplus 1\oplus 0=1$

So syndrome calculated is $S_3S_2S_1$=111 that means seventh bit from right is erroneous and the corrected codeword is 1111111 and again it goes to error detection and actual data sent from transmitter is $D_4D_3D_2D_1$=1111. Now receiver will acknowledge correction reception of data by sending back ACK packet to the transmitter.

For double-bit error

If the received codeword is 0011111, receiver performs error detection and found to be erroneous. Receiver calculate new error syndrome as

$S1=P1\oplus D1\oplus D2\oplus D4= 1 \oplus 1 \oplus 1 \oplus 0=1$

$S2= P2 \oplus D1\oplus D3\oplus D4 = 1\oplus 1 \oplus 0\oplus 0=0$

$S3=P4 \oplus D2\oplus D3\oplus D4 = 1 \oplus 1\oplus 0\oplus 0=0$

So new error syndrome calculated is $S_3S_2S_1$=100 that is fourth bit from right is the erroneous bit and we know that the fourth position is check bit position and the corrected codeword is 0010111 and again it goes to error detection and found to be erroneous. since (7, 4) Hamming code can only correct single bit since packet cannot be corrected it means that more than single bit errors occur in the received codeword and the received data with error is 0011. Now receiver responds by sending NAK to the transmitter, keeping erroneous copy say it copy1 in its buffer. Transmitter transmits second copy of the same packet in normal form as 1111. At the receiver, it is received with an error as say 1101. Now receiver apply packet combining scheme using this received copy say called it copy2 and previously stored copy1 using Ex-OR operation to find the erroneous positions as

Copy1 = 0011
Copy2 = 1101
= 1110

Receiver detects the positions of erroneous bits and apply brute force to generate all possible candidates and all the generated candidates undergo error detection test and thus correct packet is received.

As clear from examples, we have employed PC scheme on demand basis if Hamming code fails to correct more than single bit error. With this approach we are using the useful information present in the received erroneous copies of Hamming code and further using this information to enhance the performance of conventional PC scheme. Thus the probability of error being detected and corrected is higher in the proposed scheme resulting into lower packet error rate.

Conclusion

In this study, new scheme is proposed to recover packet using horizontal and vertical approach of packet combining scheme. Unlike conventional PC where two erroneous copies of the packet is necessary to find the correct packet if the first copy is received with an error(s), the proposed technique employ PC scheme only on demand basis. If the packet get corrected in the first attempt itself (higher probability of getting corrected by Hamming code), the aggregate number of packet being transmitted in the proposed packet combining scheme is lesser than that of conventional PC scheme. Since the number of bits transmitted for the proposed technique is lesser than the conventional Packet combining scheme, the throughput of the proposed packet combining scheme is higher than PC logically. Since horizontal checking is done using Hamming code on the received erroneous packet and vertical checking using conventional packet combining scheme so two-dimensional checking performed on single packet leads to better error correction as compared to the techniques where only Hamming code or only packet combining scheme is applied. And the low latency of the proposed scheme is analyzed qualitatively.

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