International Journal of Applied Engineering Research ISSN 0973-4562 Volume 10, Number 18 (2015) pp 38664-38670

A Low-Power Sensor Processor with a Approximation-based Fractional Wakeup Timer for Long-Term Sleep of Wearable Sensor Devices

Daejin Park
Research Professor School of Electronics Engineering Kyungpook National University boltanut@knu.ac.kr

Jeonghun Cho
Associate Professor, School of Electronics Engineering Kyungpook National University jcho@knu.ac.kr

Abstract
The proposed chip is an ultra low-power sensor processor specifically designed for deep-sleep synchronization of wearable glasses to realize 3DTV vision effect, which can be widely applied for traditional IoT sensor devices using long-term sleep operations. This proposal implements a newly designed fractional-order synchronizer by adjusting the synchronization accuracy of the stereovision without external sync information using a heavy RF-baseband chip. The fractional-order synchronizer enables accurate synchronization based on the approximation method of the fractional residue regardless of sync-clock speed and allows the input wireless sensor to be turned off to provide perfect flicker-free synchronization in deep-sleep operating mode. The implemented one-chip solution uses less than roughly 11%(10x) of the operating current that major commercial shutter glasses use. While the input wireless sensor is off, the internal synchronization experiences only a 1.5% deviation in the sync timing over the running time of a two-hour movie. This enables a perfect flicker-free feature without any interruption in the synchronization of stereovision and reduces the operating current by the perfect synchronization in deep-sleep mode. This paper describes the system architecture, including the details of the proposed techniques and identifies the system key concepts and functions.

Keywords: Low-power wakeup timer, Power mode, Sensor processor. Approximation

Introduction

New demand for 3DTV home theaters is beginning to grow. There are many ways to deliver the 3D visual effect [1][2]. Many electronic appliance companies have adopted LCD active shutter glasses (SG) to implement the stereoscopic 3D visual effect [3][4][5] in Full-HD resolution (1080p).

Fig. 1(a) shows a stereoscopic 3DTV system using active shutter glasses. The 3DTV continuously transmits sync packets that allow the 3DTV active shutter glasses to synchronize the on/off switching of the lens for 3D stereovision. The sync processor in 3DTV active shutter glasses has to receive the input sync packets, consuming large amounts of current to perform packet analysis and reconstruct the sync timing to drive the LCD lens.

In addition, SG technology needs the complex SG chip and on-board battery, compared to film-type patterned retarder (FPR) and experiences the excessive flicker-effect which has been the source of complaints of eye fatigue and poor picture quality [6]. The low-cost, low-power, and flicker-free features of 3DTV active shutter glasses are needed to boost the SG technology compared to FPR.

The flicker effect of shutter glasses is caused mainly by stereovision cross-talk when synchronization failure happens. When the wireless receiver input is broken up by external noise, 3DTV users often experience a flicker effect, illustrated in Fig. 1(b)(c). To overcome the flicker-effect that arises from synchronization failures, shutter glasses include a high-performance sync processor to perform noise filtering [7]. Furthermore, several 3DTV manufacturers are adopting the expensive Bluetooth. The existing approach of commercial sync processors is not cost-effective and shows no consideration for low-power operation due to their use of a heavy wireless front-end and synchronization based on a integer-point synchronizer that requires a high-speed CPU clock, which leads to more power consumption.

In this paper, we propose our techniques for the flicker-free low-power synchronization of 3DTV active shutter glasses powered by our newly designed hardware. This paper is organized as follows. In Section II, the motivation and system architecture are introduced. Section III describes the details of the proposed techniques. The measurement results and discussion are presented in Section IV. Finally, Section V concludes the paper.

Motivation and system architecture

Fig. 1(d)(e)(f) illustrates the operation of the proposed sync processor. The concept is to use a design approach with fractional-order circuits and systems [8] to accurately reconstruct the internal sync timing in fractional order scale between two independently clocked systems. Because the 3DTV and shutter glasses are independently clocked systems that must share sync timing, synchronization by a conventional integer-point synchronizer would require a high-speed sync-clock. The accumulation of synchronization errors is caused by the absence of the external sync timing [9] caused by the external noise.

We present a newly designed hardware called a fractional-order synchronizer, which operates in fractional order scale. It enables the accurate synchronization of the two independently clocked systems of the 3DTV and the active shutter glasses with a slow local clock. It also supports synchronization during a specific period of time without receiving any sync packets. Although there are several approaches to performing synchronization between independently clocked systems [10][11][12][13], our approach is especially focused on

minimizing power consumption by providing a reasonable resolution of synchronization at a low-speed clock frequency and turning off the wireless input during a specific period of time for deep-sleep synchronization.

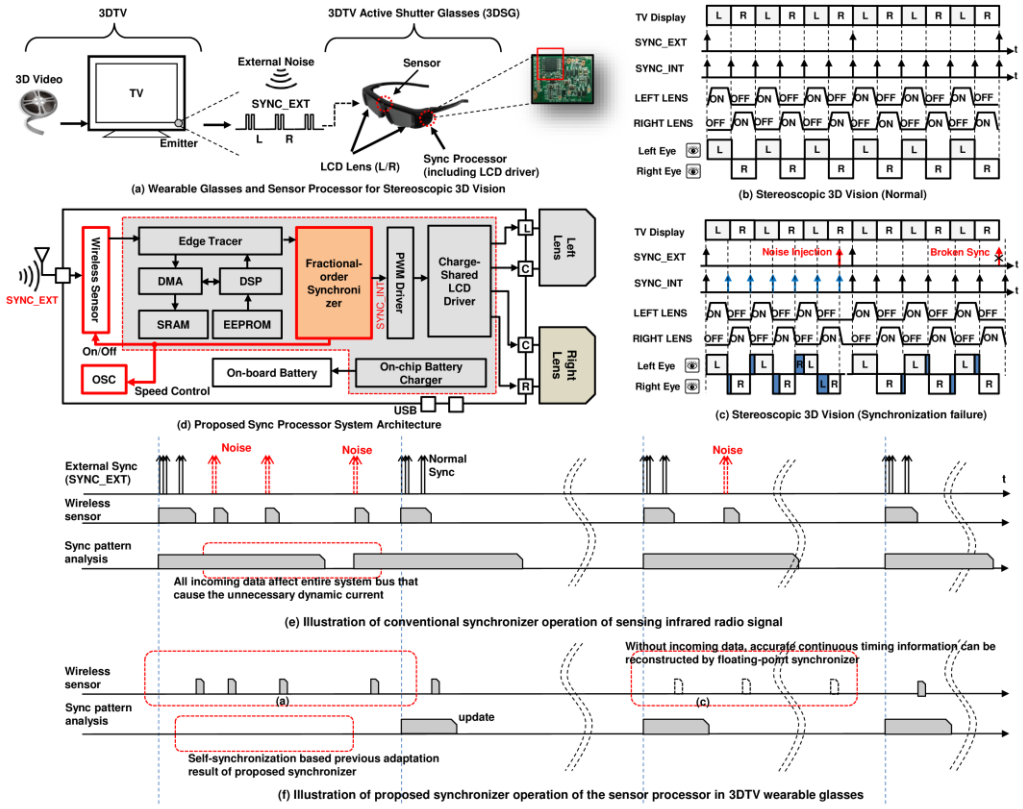

Fig. 1. Proposed sync processor architecture and its operation.

Proposed Techniques

The proposed sync processor is implemented through the following two techniques for flicker-free synchronization in low-power operation.

A. Perfect synchronization based on fractional-order synchronizer architecture

Fig. **Error! Reference source not found.**(a) shows the conventional integer-point synchronizer and the data path that it uses to measure the input sync duration on an integer-order scale. The duration of external sync (SE) timing is simply measured and divided into the internal sync (SI) timing by the local clock in the 3DTV shutter glasses. The sync reconstruction by the conventional integer-point synchronizer is described in the following equation [Eq. 1]:

$$SI_{fixed} = \frac{T_{SE(i)} - T_{SE(i-1)}}{N_{SI}} = SI_{ideal} \pm \Delta(error) \qquad (1)$$

Due to the two independently clocked systems in the 3DTV and active shutter glasses, synchronization based on the integer-point synchronizer always evokes a fraction of the error described in Eq.(1), compared with the ideal sync duration, which is caused by the independently clocked local sync-clock. The integer-point synchronizer clock resolution must be increased to decrease this fractional error. This results in more power consumption.

Fig. (b) illustrates the sync reconstruction by the integer-point synchronizer from the received SE timing. When the external sync packet is received, the fractional error does not accumulate, because the received sync is used as a reset for the current error. However, if the sync packet is absent, the small fractional error in the synchronization will gradually increase and accumulate. Therefore, the sync processor always has to receive the sync packets, which results in more power consumption. Fig. **Error! Reference source not found.**(c)(d) shows the proposed fractional-order synchronizer implemented in a fractional-order concept. This timer compensates for the fractional error in the synchronization by employing two independent parts of the timer. The following equations [Eq. (2),(3),(4)] describe the data path of the proposed hardware block for the fractional-order synchronizer to enable the measurement in the fractional-order scale.

$$SI_{floating} = SI_{integer-part} \pm SI_{fractional-part} \qquad (2)$$

$$SI_{integer-part} = \frac{T_{SE(i)} - T_{SE(i-1)}}{N_{SI}} \qquad (3)$$

(4)

This fractional-order data path is meant to compensate for the

counter value of the integer timer when there is an overflow of the fractional timer by the amount accumulated in the fractional part, which is the N-bit shifted to represent the N-bit resolution. Because the residual part of the result divided by the local clock is represented as a fractional part with N-bit resolution, the fractional error compared with the original sync duration can be dramatically reduced to $1/2^N$. The accumulation error will be distributed inside the one internal sync clock because its integer part of the timer count is always compensated for by the currently calculated fractional part. We implemented our approach to the concept of the fractional-order synchronizer using only two types of timers with a reasonable number of counter bits.

The automatic sync adaptation based on the fractional-order synchronizer is illustrated in **Error! Reference source not found.**(e). The adaptation hardware operates it automatically without the CPU or software processing. The SE (external sync) transmitted by clock domain A (3DTV) has to be re-synced and reconstructed into the internal sync timing for the LCD lens switching. The previous adaptation result of the sync timing will be used to predict the next sync timing. The sync reconstruction engine, including the fractional-order synchronizer and the automatic sync adaptation algorithm, is described by Eq. (5),(6),(7),(8),(9) and (10). The predicted sync timing is accurately adjusted as the fractional order scale represented by Eq. (3),(4). The predicted internal sync timing is adjusted for the $PHASE_{adaptation}$ to minimize the $PHASE_{error}$. The long-term prediction is performed to trace the rapid change of the external sync timing insensitively.

$$SI(n)=FREQ_{adaptation}+PHASE_{adaptation} \quad (5)$$

$$SI(n)=\overline{SI(n)}+PHASE_{error}\pm\Delta \quad (6)$$

$$\overline{SI(n)}=\frac{\sum_{i=k}^{n}(SE(i)-\overline{SI(i-1)})}{s^{n-k}} \quad (7)$$

$$SI(i)=\frac{T_{SE(i)}-T_{SE(i-1)}}{N_{SI}}\pm\frac{residue(\frac{SI_{integer-part}}{N_{SI}})*2^N}{N_{SI}} \quad (8)$$

$$PHASE_{adaptation}=PHASE_{error}-\Delta \quad (9)$$

$$\Delta=T_{SI}(i+1)-T_{SE(i)} \quad (10)$$

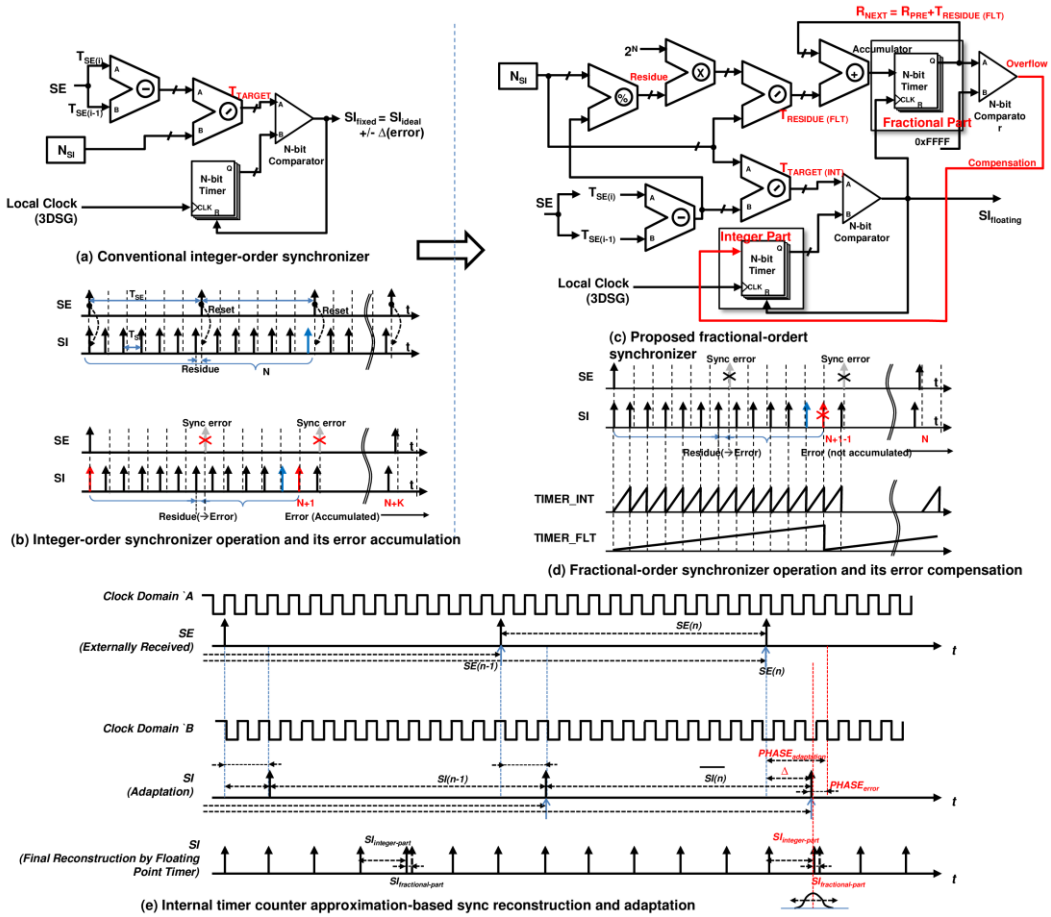

Fig. 2. Conventional integer-point synchronizer and proposed fractional-order synchronizer.

B. Universal edge tracer

The 3DTV shutter glasses must receive the exact specific sync patterns defined by various 3DTV manufacturers with a single chip. The case-by-case software-driven approach to decode various 3DTV sync formats requires a large-code ROM size and a long CPU time. The operating current of the sync processor depends on the CPU time required to run the software to analyze the sync patterns.

To achieve low power, a small size, and general-purpose reusability, we adopted the edge tracer concept to track the common information monitored with the edge phase and edge distance for the incoming packets transmitted from 3DTV and to delay the sync pattern analysis requiring fast CPU resources. We integrated a dedicated SRAM buffer with the edge tracer to trace the incoming packets without using the CPU.

During the tracer operation, the CPU can hibernate to minimize the systemâ€™s power consumption. The overhead to wake up from the hibernation mode is very small compared with an external sync pulse period. The CPU wakes up for a specific short period, during which it analyzes the edges traced into the SRAM buffer.

Fig. (a) shows the overall architecture of the edge tracer. The input sync pulses are accumulated in the SRAM via DMA bus. The traced edges are analyzed by the trail-made DSP. Fig. (b) is the field structure used to describe the general information about the edges. We minimized the field information to reduce the SRAM size needed by the edge tracer. In addition, the matching hardware could be generalized and easily reconfigured with the registers control for the specific pattern matching. Fig. (c) shows an example of incoming sync patterns affected by external noise.

Fig. (d) is an example of edges traced into the SRAM buffer. We manage the SRAM buffer by using a ring type to increase the area of utilization. At the specific time, we perform the analysis of the past N number of edges accessed from the end-point of the SRAM buffer. Fig. (e) shows the operation of the window-matcher DSP used to scan the traced data in the SRAM buffer. This special DSP hardware is reconfigured with the registersâ€™ control to match the correct patterns for specific edge phases, the number of counts, and the time distance between edges. This block chooses specific patterns matched with predefined field values and merges them into the event group to be easily used by the sync reconstruction engine, as shown in the following section.

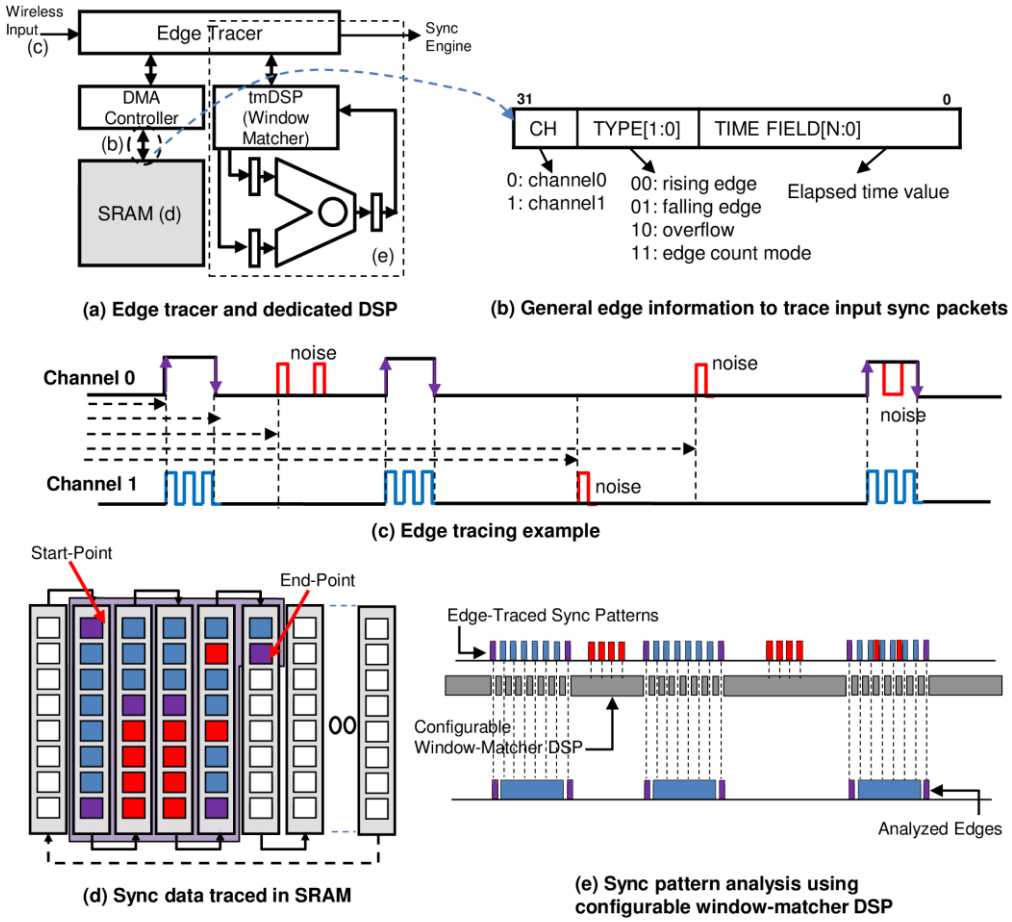

Fig. 3. Edge tracer architecture to trace the incoming sensing data.

C. Deep-sleep synchronization by fractional-order synchronizer

The label err-integer shows the error caused by the integer-point synchronizer. The error caused by the integer-point synchronizer lies within a wide range of error variation compared with the results of the fractional-order synchronizer. As the clock frequency decreases from 2MHz to 200KHz, the counter error caused by the integer-point synchronizer is

proportionally increased to nearly 30%, as shown in Fig. (a). In this situation, the viewer may feel the 3D vision flicker from the stereovision cross-talk due to sync reconstruction failure.

The label err-fractional shows that the error caused by the fractional-order synchronizer deviates by nearly 0%, regardless of the clock speed, described in Fig. (b). In accordance with this result, we can decrease the clock speed to reduce the operating current on the sync reconstruction block while still providing accurate resolution. The error caused by the fractional-order synchronizer is bound to the reasonable number of errors in the low-speed clock, as shown in Fig. (c).

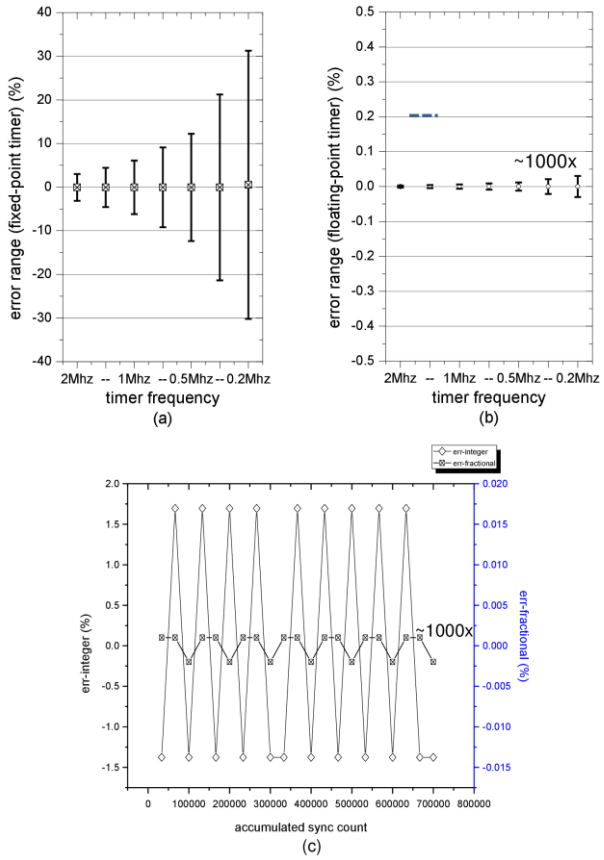

Fig. 4. Comparison of the synchronization errors.

Chip implementation, measurement results, and discussion

We fabricated the proposed sync processor using 0.18um 2-poly 6-metal embedded-flash CMOS technology. Fig. (a) summarizes the chip features and Fig. (b) shows its micro-graph. The 2.4 x 2.3 mm^2 chip area contains an additional 8,500 logic gates for the fractional-order synchronizer. The 3DTV active shutter glasses integrated with our sync processor were verified to work with the major commercial 3DTV sets and 3D laptops, as shown in Fig. **Error! Reference source not found.**(c). We analyzed the sync packet patterns of the commercial 3DTV shutter glasses to implement the compatible software codes and replaced the existing on-board chip with our sync processor [Fig. **Error! Reference source not found.**(d)(e)] to utilize the on-board LCD active glasses.

Fig. **Error! Reference source not found.** shows the performance of the fractional-order synchronizer which provides accurate synchronization for random noise environment in Fig. **Error! Reference source not found.**(a). The synchronization result in Fig. **Error! Reference source not found.**(b) is nearly 0% error without any CPU-based calibration. However, Fig. **Error! Reference source not found.**(c) shows the conventional synchronization by the integer-point synchronizer and digital correction by software powered by CPU. Fig. **Error! Reference source not found.**(d) shows the result of an error in the disabled mode of the input sync receiver to show the self-compensation performed by the fractional-order synchronizer.

Even though the input sync receiver is disabled in Fig. **Error! Reference source not found.**(e), the sync reconstruction by the fractional-order synchronizer results in only just under 0.75% deviation compared with the original sync period after one hour has elapsed without any input sync. The experiments were repeated many times and the result range from 0.5% to 1.5%. This means that the sync processor can be isolated from the external noise and that the 3DTV user can enjoy flicker-free 3D content without receiving any external sync pulse during a specific time window.

When the initial sync information analysis is performed, a fast clock speed is needed; moreover, its operating current is maximized only for a short period of time. The clock speed can be decreased thanks to the accuracy of the fractional-order synchronizer, leading to dynamic power reduction. When the input sync packets are stable, the input sensor turns off to enter a deep-sleep mode.

We compared our operating current results with those of major commercial shutter glasses, as shown in Fig. **Error! Reference source not found.**. The operating current of our glasses is less than roughly 11% (10x longer battery time is available) of major commercial shutter glasses operating currents, which improves our original results (25%) [14][15] from the COOLChips XIV presentation. With the enabling of all the proposed techniques, the power consumption of the sync processor is about 0.592mW (on-board 3.7V battery).

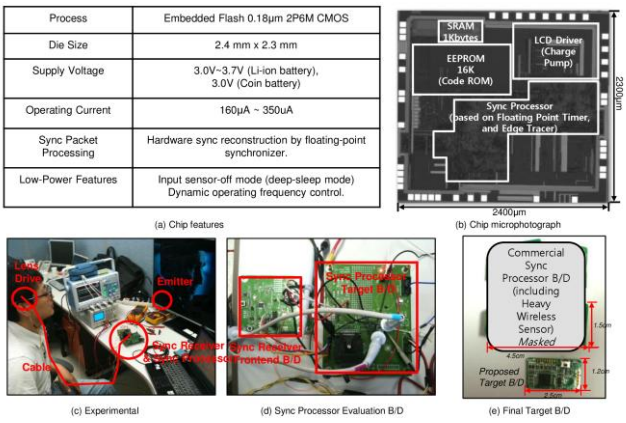

Fig. 5. Chip features and top micro-photograph.

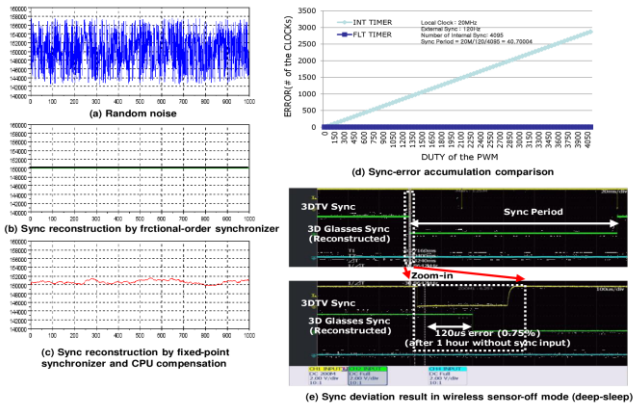

Fig. 6. The performance of proposed synchronizer.

Conclusion

A low-power hardware sensor processor especially designed for wearable glasses has been implemented with a fractional-order synchronizer for deep-sleep synchronization and noise-free sync reconstruction, which can be widely applied for traditional IoT sensor devices using long-term sleep operations. The proposed chip adopted a design approach of fractional-order circuits by adjusting the accuracy of the fractional-part timer to accurately synchronize the two independently clocked systems between 3DTV and wearable glasses in a deep-sleep mode. The evaluation results demonstrate that the proposed power-saving techniques are very effective and still provide accurate flicker-free synchronization for stereoscopic 3D. The accurate sync reconstruction based on the fractional-order synchronizer makes it possible for the operating frequency to be dynamically re-adjusted for low-power operation with the speed control of the synchronizer clock; furthermore, the input wireless sensor can be turned off in deep-sleep mode with just 1.5% deviation of the sync timing over two hours of movie playtime. Our proposed approach reduces power consumption to less than a maximum of about 11% compared with other major commercial processors and enables ten times longer battery time without any external noise interruption.

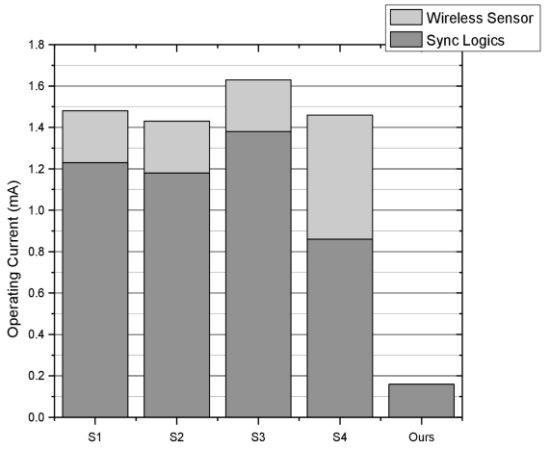

Fig. 7. Power reduction results (compared with commercial chip).

Acknowledgement

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education(2014R1A6A3A04059410).

References

[1] N. Holliman, N. Dodgson, G. Favalora, and L. Pockett, "Three-dimensional displays: A review and applications analysis," *Broadcasting, IEEE Transactions on*, vol. 57, no. 2, pp. 362–371, June 2011.

[2] L. Onural, "An overview of research in 3DTV," in *Systems, Signals and Image Processing, 2007 and 6th EURASIP Conference focused on Speech and Image Processing, Multimedia Communications and Services. 14th International Workshop on*, June 2007, p. 3.

[3] A. Srivastava, J. de Bougrenet de la Tocnaye, and L. Dupont, "Liquid crystal active glasses for 3D cinema," *Display Technology, Journal of*, vol. 6, no. 10, pp. 522–530, Oct. 2010.

[4] P. Tsang, "Apparatus for three-dimensional display," in *US Patent No.6510002*, 2003.

[5] L. Noble, "Three dimensional viewing glasses," in *US Patent No.4907860*, 1900.

[6] W. Tam, F. Speranza, S. Yano, K. Shimono, and H. Ono, "Stereoscopic 3DTV: Visual comfort," *Broadcasting, IEEE Transactions on*, vol. 57, no. 2, pp. 335–346, June 2011

[7] E. Ulusoy, G. Esmer, H. Ozaktas, L. Onural, A. Gotchev, and V. Uzunov, "Signal processing problems and algorithms in display-side of 3DTV," in *Image Processing, 2006 IEEE International Conference on*, Oct. 2006, pp. 2985–2988.

[8] A. Elwakil, "Fractional-order circuits and systems: An emerging interdisciplinary research area," *Circuits and Systems Magazine, IEEE*, vol. 10, no. 4, pp. 40–50, 2010.

[9] W. J. Dally and J. W. Poulton, *Digital systems engineering*. plus 0.5em minus 0.4emCambridge University Press, 1998.

[10] L. Sarmenta, G. Pratt, and S. Ward, "Rational clocking [digital systems design]," in *Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on*, Oct. 1995, pp. 271–278.

[11] W. Dally and S. Tell, "The even/odd synchronizer: A fast, all-digital, periodic synchronizer," in *Asynchronous Circuits and Systems (ASYNC), 2010 IEEE Symposium on*, May 2010, pp. 75–84.

[12] W. Stewart and S. Ward, "A solution to a special case of the synchronization problem," *Computers, IEEE Transactions on*, vol. 37, no. 1, pp. 123–125, Jan. 1988.

[13] K. Yun and A. Dooply, "Pausible clocking-based heterogeneous systems," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*,

vol. 7, no. 4, pp. 482–488, Dec. 1999.

[14] D. Park, T. G. Kim, C. Kim, and S. Kwak, "A low-power sync processor with floating-point timer and universal edge tracer for 3DTV active shutter glasses," in *IEEE Symposium on Low-Power and High-Speed Chips (COOLChips XIV)*, April 2011, pp. 147–149.

[15] D. Park and T. G. Kim, "A sync processor with noise robustness for 3DTV active shutter glasses," in *SoC Design Conference (ISOCC), 2010 International*, 2010, pp. 147–149