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Design of CPW Based Wideband Efficient Power Amplifier for Wireless Applications

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ABSTRACT

In this paper the author has given a new technique of designing power amplifier (PA) using 50Ω matched coplanar waveguide (CPW) component in order to improve power efficiency for K-band and other wireless application. In this present work CPW line is used in order to provide broadband multi-section matching networks which could improve bandwidth, output power, power gain and power added efficiency (PAE). This new technique of designing PA also enhances the data transmission rate and achieves maximum output power in the desired frequency band. This design process is simulated in ADS.v.12 using predictive technology model (PTM) 65nm CMOS process. A simulation result of PA achieves a reflection parameter of -43.06dB at 23GHz with forward gain of 15.6dB over the frequency band of 20.5-24.5GHz. The best part of this novel approach is to achieve PAE of 58% using

the concept of coplanar waveguide, since it provides perfect matching between input and output port of the device.

Index Terms- Power Amplifier, Co-planar waveguide (CPW)

I. INRODUCTION

A PA is a nonlinear circuit capable of amplifying a 'large' signal at a given frequency or in a given frequency band which converts the DC supply power into a specific amount of radio frequency (RF) or microwave power. The generation of RF/microwave power is required not only for wireless transmission, but also in applications such as radar, industrial, scientific, and medical (ISM) fields. Modern wireless communications systems offer a number of services besides voice calling to the increasing number of mobile users. Example of service is video calling, video streaming, internet browsing and downloading. These increasing demands on mobile services require the implementation of high data rate transmission in the emerging communications systems. High data rate in turn results in broad modulation bandwidths. Therefore, spectrally-efficient PA has to be used to effectively exploit the reserved bandwidth for the communications standard [1].

Achieving these requirements together is a challenging task in power amplifier design, because of the trade-off between the design parameters. The main trade-off is that between efficiency and linearity. Any increase in the efficiency of the power amplifier comes usually at the expense of its linearity and vice versa [2]. The design of wideband high efficiency power amplifiers is another challenging task, which will be considered in this article.

The demand for low power operation and greater miniaturization are forcing the levels of integration to great extent between RF and IF circuits and enhance the data transmission rate and also maximize the bandwidth efficiency in the limited frequency for applications such as wideband wireless communication, automotive radar and satellite radio [3]. With new conception of coplanar waveguides (CPW) in place of inductors is to provide broadband level for the matching networks which could be used to improve output power and PAE [4]. To design a wideband power amplifier using CMOS technology that maintains a high efficiency at broad range of frequencies is more complicated and challenging task that has forced research community to work in the area of monolithic microwave integrated circuit (MMIC). Moreover, power-amplifier miniaturization and integration for small-cell applications are vitally needed and keeping the same high-performance capability.

Power amplifiers involve a balancing of many different parameters, including PAE, maximum output power, maximum stable gain, power dissipation, input/output matching and breakdown voltage. As with many RF component designs, these requirements are often in conflict with one another, for example achieving good linearity usually comes at a cost in PAE. Thus the aim of this article is to design of PA that would maintain a high efficiency over a broad range of frequencies used by a number of standards, which is a burning topic of research for microwave application. In article [5] the author has designed a PA module in which a single-ended two stage

Class AB, PA is adopted for its higher power efficiency and better linearity and it can be used for 3G mobile communications. A novel dual band transmission line parallel Doherty amplifier architecture has been implemented for active antenna arrays and base-station applications in next-generation communication systems which are based on the reactance compensation technique [6]. A complete frequency response analysis and bandwidth extension of the Doherty amplifier has been derived for output power and efficiency versus input voltage and frequency, based on microstrip transmission lines with reduced impedance transformation ratio [7]. Stacked FET millimeter wave power amplifiers using on-chip shielded coplanar waveguide transmission lines have achieved maximum power added efficiency up to 38% [8, 9].The early class-F PA designs using multiple resonators were introduced by Tyler and extended by using lumped-element multi-resonator output networks for high-power AM-broadcast transmitters, from LF through HF [10, 11].

In this article a CMOS PA using matched CPW component for K-band wireless applications is proposed. A co-planar waveguide line in place of LC circuit is used to provide broadband matching networks in order to improve performance parameters. This paper is organized as follows: Section II presents microwave PA design parameters considered for its implementation. Section III presents design and analysis of CMOS PA using co-planar line for impedance matching. Section IV discussed about the simulation results. Finally, conclusion is discussed in section V followed by references in last section of this article.

II. MICROWAVE PA DESIGN PARAMETERS

The basic building block of a PA is the active device (transistor), which plays a main role in determining the capability of the PA in terms of output power, gain, efficiency, linearity and bandwidth. Various bipolar and field-effect device technologies have been developed since decades to meet the continuing demands of communications systems.

The most important design parameters of a PA include power added efficiency (PAE), drain efficiency (η_d), output power (P_{out}), and power gain (G_p). The relationship between the parameters, PAE,η_d,P_{out}, and G_p is obtained from the principle of conservation of energy applied to the PAs structure, as shown in Figure1.

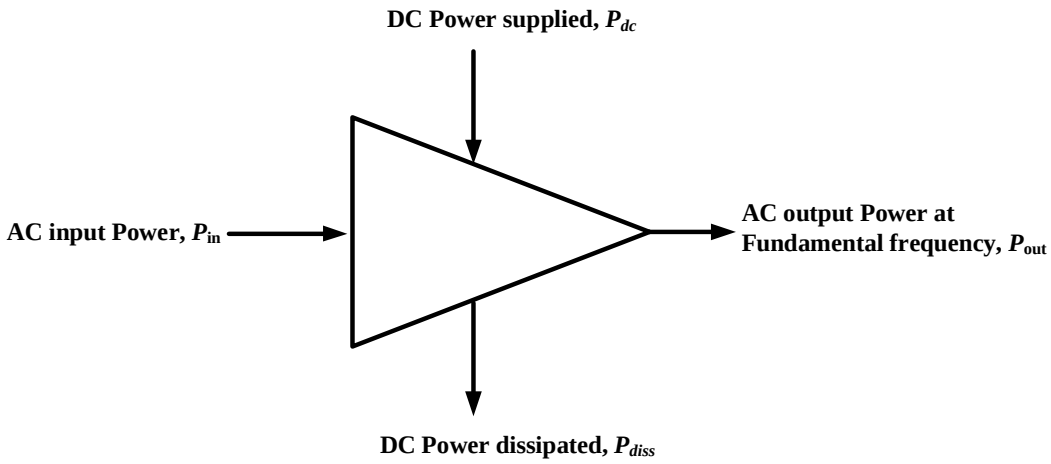

Fig.1 PA block diagram.

The total input power must equal the total output power, so that

$$P_{in} + P_{dc} = P_{diss} + P_{out} \quad (1.1)$$

Where, P_{in} is the ac input power, P_{dc} is the dc power supplied, P_{out} is the ac output power, and P_{diss} is the total power dissipated in the transistor.

The efficiency of power conversion is called the "PAE", which is defined as,

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad (1.2\ a)$$

Using equation (1.1), it can also be shown that

$$PAE = \frac{P_{dc} - P_{diss}}{P_{dc}} = \eta_d \left[1 - \frac{1}{G_p}\right] \quad (1.2\ b)$$

Where,

$$\eta_d = \frac{P_{out}}{P_{dc}} \quad (1.3)$$

and,

$$G_p = \frac{P_{out}}{P_{in}} \quad (1.4)$$

Equation (1.2b) shows that the efficiency of dc to ac power conversion depends on the power dissipated in the active device. Hence in order to obtain a maximum PAE, the power dissipated in the active device must be minimized.

Minimization of power dissipation in the active device and the maximizing of the output power at the fundamental frequency is the main objective in the design of the high efficiency PAs.

III. POWER AMPLIFIER DESIGN AND ANALYSIS

The proposed schematic of PA circuit is shown in Fig.2 which includes bias circuit, input matching network and output matching network. A two-stage power amplifier circuit is composed of coplanar lines as a matching purposes and DC voltages.

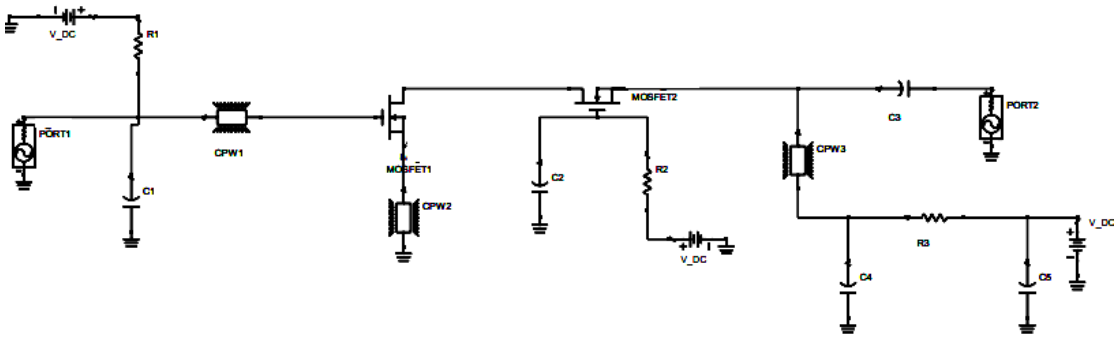

Fig.2 Proposed Schematic of power amplifier.

In this article the author has achieved maximum output power and efficiency by improving input matching using CPW line in order to diminish signal distortions caused by reflection and hence enhances linearity of the device. Input and source impedance (50Ω) matching is composed of CPW1 and CPW2. On the other hand, output matching network of L-type is composed of C3, C4, C5 and CPW3, so load impedance of 50Ω is transformed to the best load value, thus the required output power can be obtained. Coplanar waveguide line instead of inductor is the key to design a matching network because it determines the quality of the matching network. In power amplifier, matching network could also be used to adjust the amplifier gain flatness. The circuit is simulated by advanced design system (ADS) using 65nm CMOS process. The chosen design specifications of MOS transistors under low supply voltage of 1.2V for the simulation are shown in Table 1.

TABLE.I Component values and coplanar line dimensions of proposed power amplifier

CPW1	W=0.46mm,L=2.25mm
CPW1	W=0.54mm,L=3.67mm
CPW1	W=0.54mm,L=2.75mm
C1	1.96fF
C2	1.23PF
C3	1PF
C4	1fF
C5	1.2fF
R1	52.8 Ω
R2	52.5 Ω
R3	57.0 Ω
M1 width(μm)	94.5
M2 width(μm)	96
VDD	1.2V

IV. RESULTS AND DISCUSSION

The variation of return loss and forward gain versus frequency at desired band of operating frequency is shown in Fig.3. Thus power amplifier shows excellent return loss of -43.06dB at 23GHz within 4GHz bandwidth, which clearly depicts its wideband characteristics. Two-stage amplification is used and due to this power gain S_{21} is achieved more than 10dB at the range of frequency between 22.5GHz to 24.5GHz which meet better design requirements. The simulated variation of magnitude of PAE versus average input power which shows PAE is about 58% when input average power is around 0dBm as shown in Fig 4. The result clearly shows that with input power increasing PAE also increase which is in accordance with the designed specification of the PA for broadband matching. The total power consumption for two stage CMOS PA is 11.2mW from 1.2V power supply. Fig.5 shows layout of PA with final area of 0.74 mm^2. Table II. Shows the comparison of various parameters of reported earlier with present work. The maximum of S21 is reached nearby the centre frequency of 23GHz by optimizing capacitance and width of coplanar line parameters. Thus the desired outcome of the objective has been achieved in this present article as compared to earlier reported work.

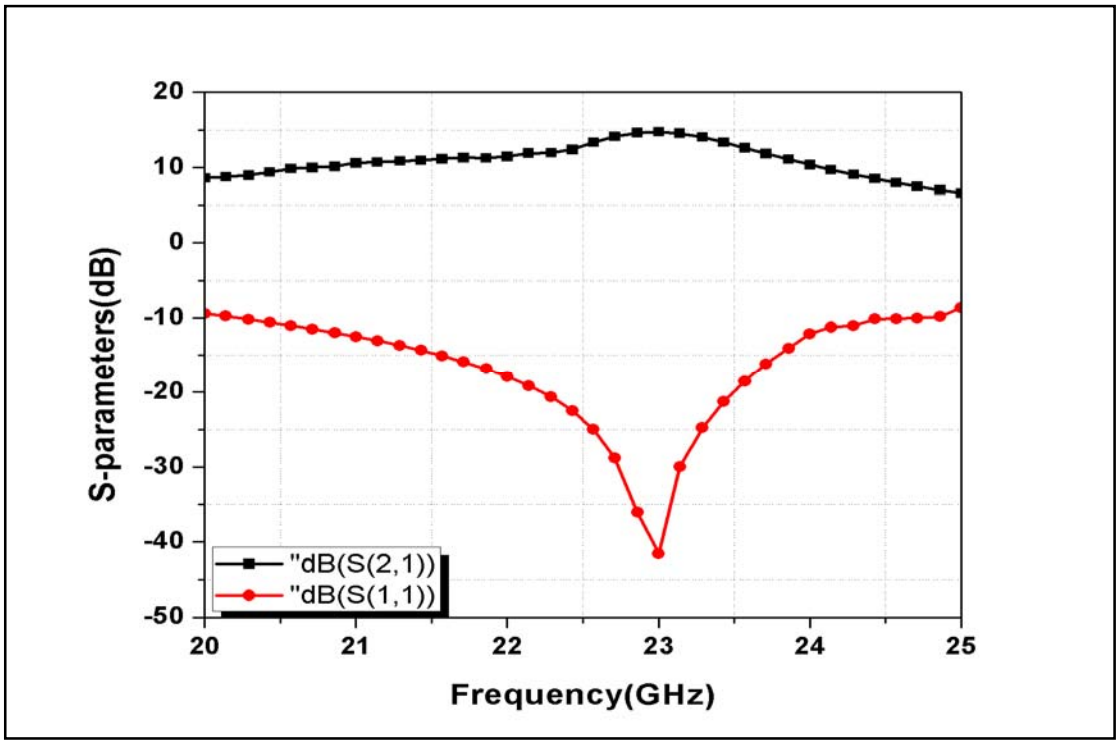

Fig.3 Return loss and Forward gain Vs Frequency

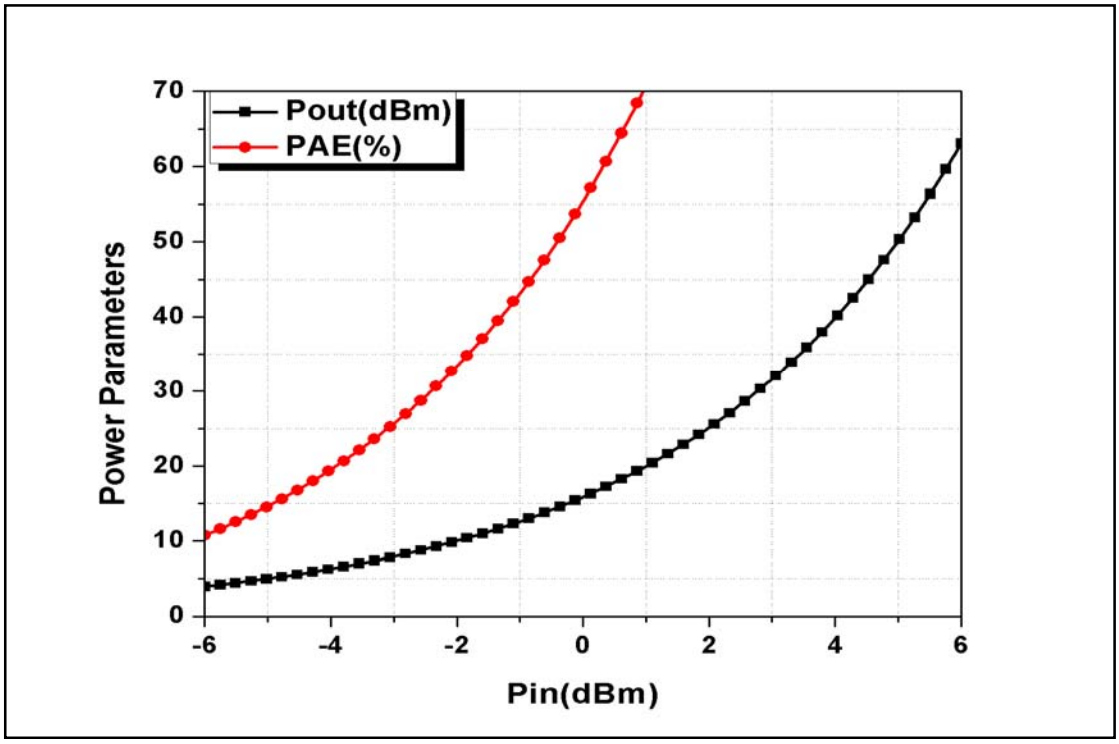

Fig.4 PAE &Output power Vs Pin (dBm)

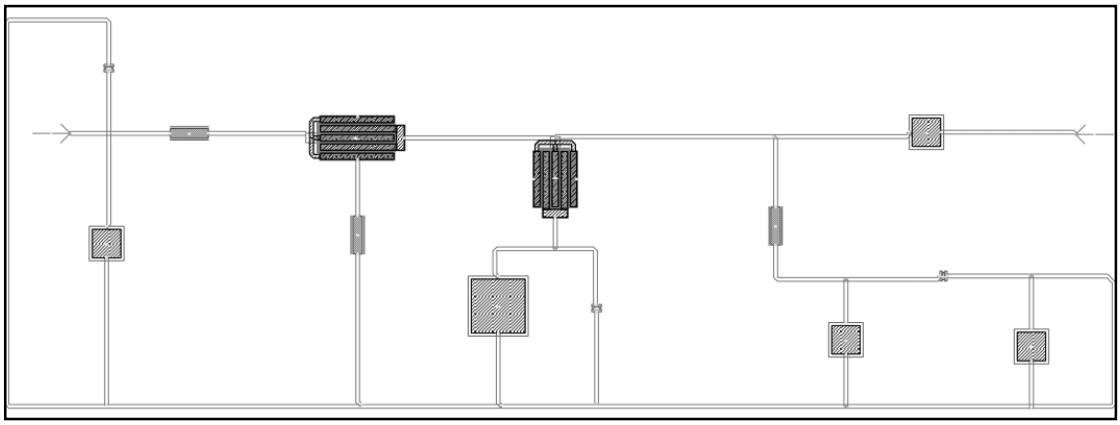

Fig.5 Layout snapshot of PA

Table II. Comparison of circuit design with previous reported paper

Parameters	**[5]**	**[6]**	**Current work**
Technology (µm)	0.18	0.18	0.065
Freq (GHz)	2.1	2.6	23
Supply voltage (V)	2.5	2.5	1.2
S_{11} (dB)	NA	NA	-43.06
S_{21} (dB)	30.5	6.5	15.6
Pout (dBm)	30.1	39	14.96
PAE (%)	51.98	73	73

Table II shows the comparison of various design parameters like operating desired band of frequency, supply voltage, return loss, forward gain, output power, power added efficiency and the technology used in this present article as compared to previous reported work. The comparison table clearly depicts that this PA design is much more efficient to meet the designed criteria.

V. CONCLUSION

The novel design of proposed CMOS PA using CPW line has been designed and implemented for wideband wireless application in the frequency band of 22.5-27GHz in this article. The state of the art of this proposed work achieves a reflection parameter of -43.06dB at 23GHz with forward gain of 15.6dB over the frequency band of 20.5-24.5GHz. The power gains are more than 10dB of broadband within 22.5GHz to 24.5GHz, and PAE is over 58%. Thus Performance standards are met for the CMOS PA for wireless applications by using a new technique of CPW line to provide broadband multisection matching network and to meet the desired design criteria.

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