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Hardware Architecture Implementation Of Wallace Tree Multiplier Using 180nm Technology

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Abstract

Multiplier are basic element in electronic circuits. These multipliers are used mainly in digital signal processing and processor applications. today we are using low power multipliers with high clock frequencies plays a dominant role. Currently demand is power efficient, high speed, and low power. In this architecture we are mainly using different type of full adders and compressors which can be used to reduce the complexity of the Wallace tree multiplier.

Index Terms— Wallace tree multiplier, conventional cmos full adder, transmission gate full adder, gdi xnor fulladder, 4:2 compressor, 5:2 compressor

I. INTRODUCTION

In olden days multiplication is carried out by sequence of addition, subtraction and shift operations. Multiplication can be done by series of repeated additions. Basically it attributes multiplicand and multiplier. The multiplier is multiply the multiplicand in number of times the process of multiplication is done and finally generates the partial products. In most of the digital computers, the operands usually contains same number of bits usually it interpreted as integers. generally the product is twice the length of operand to preserve the information content. Addition is suggested the arthematic definition is slow it almost replaced by an algorithm that makes use of positional representation. Generally multiplier is divided in to two parts. The first one is generation of partial products and second one collects and add them.

The multiplication principle is decompose in to two folds that is evaluation of partial products and shifted partial products. It is done successive additions of colums

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of the shifted partial products. Multiplication therefore performs a multi operand operation.

Power dissipation plays a crucial role in present vlsi design platform. To satisfy the MOORE'S law and consumer electronic products power efficient and low weight, low power VLSI design is manditary. Dynamic power dissipation plays a crucial role due to charging and discharging capacitance of the circuit. The formula for dynamic power dissipation is $p_d=c_lv^2f$.power reduction can be done in many methods like reduction in supply voltage V, out put capacitance C_l, and finally switching activity based on frequency F. in this paper we are describing a Wallace tree multiplier based on small full adders and compressors which leads to reduction in power and and improve the speed of operation. Battery life of electronic is limited low power increases the life span of the battery.where section 11 describes the complete motivation of work and adders and compressors are implemented in section 111 simulation results and graphs are in section1v and finally conclusion in v.

II. IMPLEMENTATION OF WALLACE TREE MULTIPLIER

Wallace tree multiplier was invented by an Australian scientist chris Wallace in 1964.the multiplication of two numbers is done fastly by using Wallace tree multiplier.and this structure is looks like a tree structre.it indicates the addition process for one column of partial products.finally three step procedure is required for the formation of Wallace tree multiplier is described as: (1) bit products formation (2) bit product reduction in to two matrix by means of carry save adder. (3) remaining two rows by using carry propagation adder.the representation of Wallace tree multiplier as shown in below.

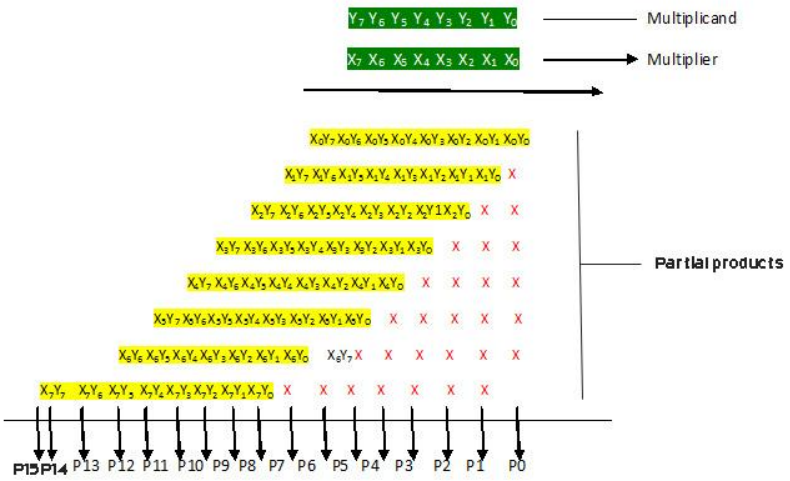

Fig 1: Wallace representation

Block diagram representation of Wallace tree multiplier as shown in below.the intermediate state reductions canbedone by the carry save adder and the final step additionisdone by carry propogation adder.if less number of pp(partial products) less number of carry save adders is required. The entire process is done by means of tree likefashion and it attributes the matrix format of (3,2).

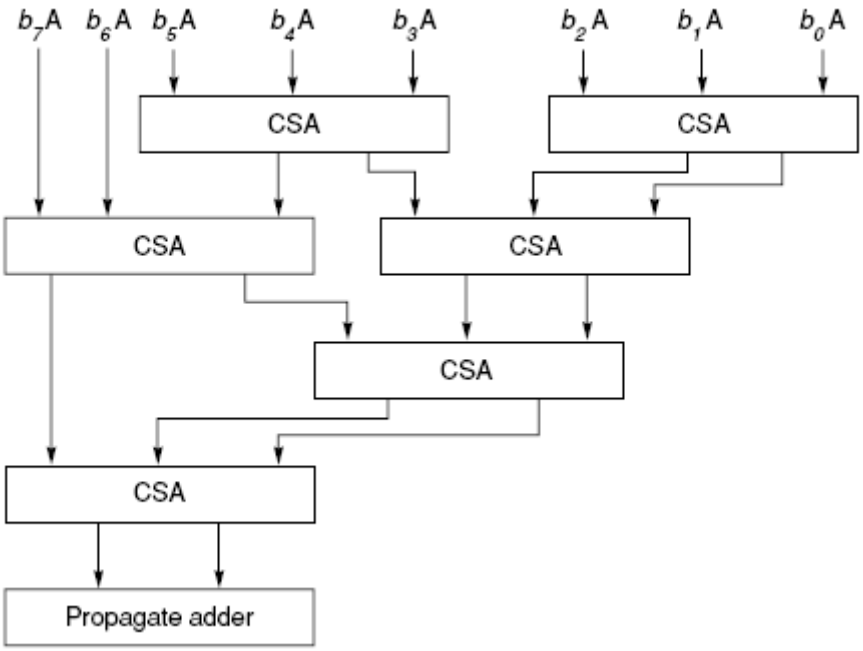

Fig: blocks representation

In wallace tree multiplier more number of carry save adders is active at an time. Mainly the usage of Wallace tree multipler the column addition is active at a time. And the layout has to be complexity in Wallace tree multiplier because it attains like a tree like fashion.and the sum of partial products is parallel. For multiplication purpose the adder plays a dominant role for which we are using different type of adders as described below.

A. Using full adders for implementing wallace tree multiplier.

1) Conventional CMOS full adder:

Adder plays a dominant role in multiplier and used in computer arithmetic. The truth table of one bit full adder as shown in below.

A	B	Carry-In	Sum	Carry-Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 3: basic table representation

The Boolean function for this truth table as:
SUM= $\overline{A}BC+A\overline{B}C+AB\overline{C}+BAC$
CARRY=AB+BC+AC

Here, A and B are adder inputs and C is carry input,sum is SUM output and CARRY is carry output. generate G occurs when the carry is internally generated by the adder. If propogate signal,P is true the CARRY-IN signal is passed to the CARRY OUT(carry).when C is true. because the carry-in of the current bit is determined by the lowest of two operands.the delay of the circuit is depends upon the generation of the carry. The schematic for the conventional cmos full adder as shown in the below.

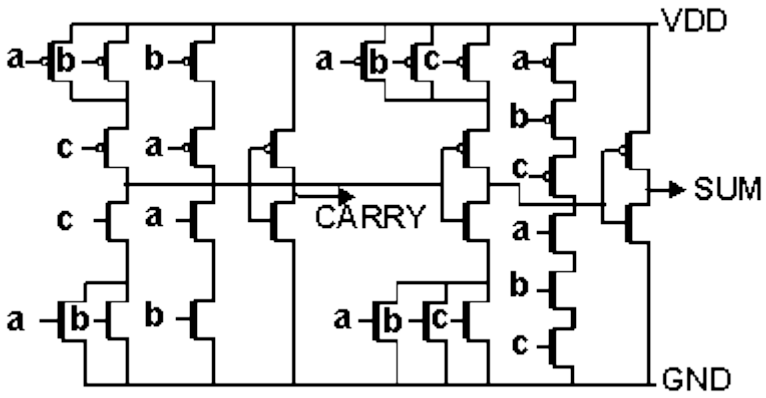

Fig 4: conventional cmos full adder

2) Transmission gate full adder:

Transmission gate full adder consists of n- channel transistor and p-type transistor have common source and drain connection but different gate connection. Modes of operations done separately for n and p devices separately. When the input signal is low or 0 both n and p devices are off hence the circuit attains high impedance. Where when the input signal is high both of n and p devices are on hence the circuit of the input is transferred to the out of the circuit.the schematic structure for transmission gate full adder as shown in below.

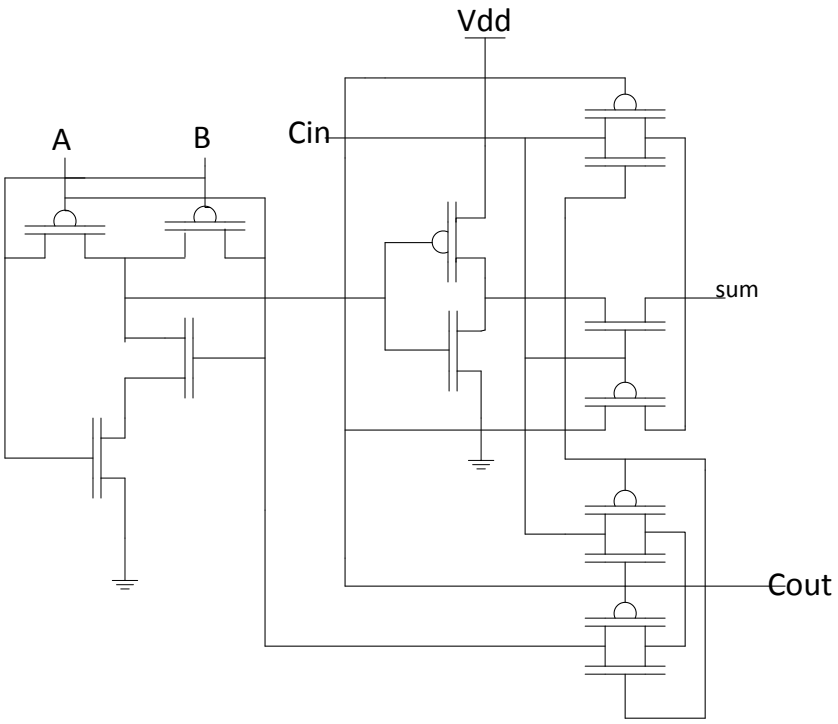

Fig :5 transmission gate full adder

3) Gate diffusion input (gdi) xnor full adder:

Gate to diffusion input (gdi) is an new technique used in low-power digital combinational circuit design. It reduces power consumption, delay and area, for maintaining low complexity of logic design. Mainly the gate to diffusion input contributes mainly three differences there are:

1) Gdi cell contains three inputs (common gate input of nmos and pmos), p(input to the source/drain of pmos), n(input to the source/drain of nmos).
2) Bulks of both nmos and pmos are connected to n and p. it can arbitarly biased in contrast with cmos inverter.

Basic schematic of gate to diffusion input (gdi) cell as shown in below:

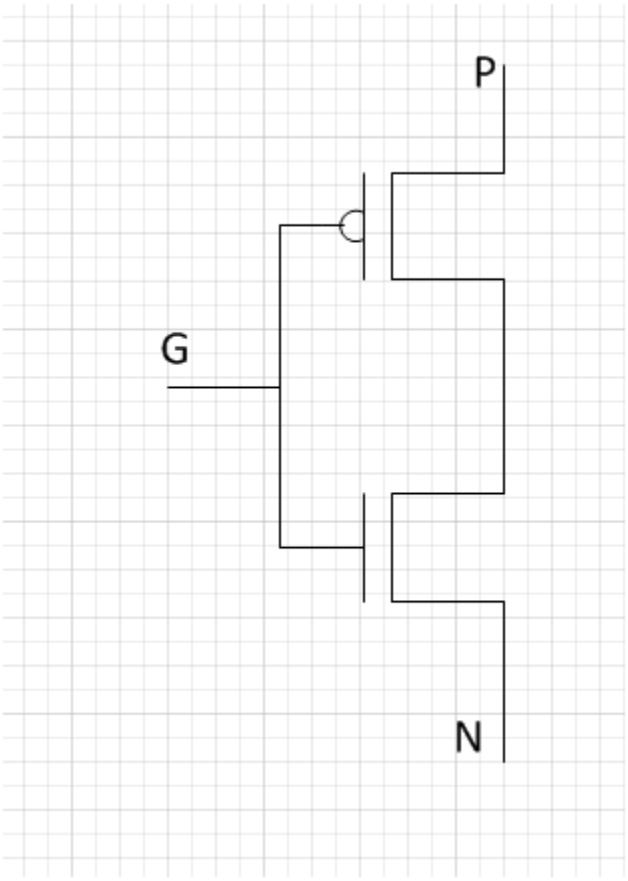

Fig :6 basic gdi cell

The simple input configuration of gate to diffusion input(gdi) attains different Boolean functions.most of these functions are complex in cmos and pass transistor logic(ptl)implementations. The input configuration as shown in below:

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	F3
B	0	A	AB	F4
C	B	A	A'B+AC	F5
0	1	A	A'	NOT

Fig:7 gdi table

GDI xor and xnor gates are based on the applications of gdi technique.each of them requires 4 transistor.the schematic of gdi xor gate as shown in below.

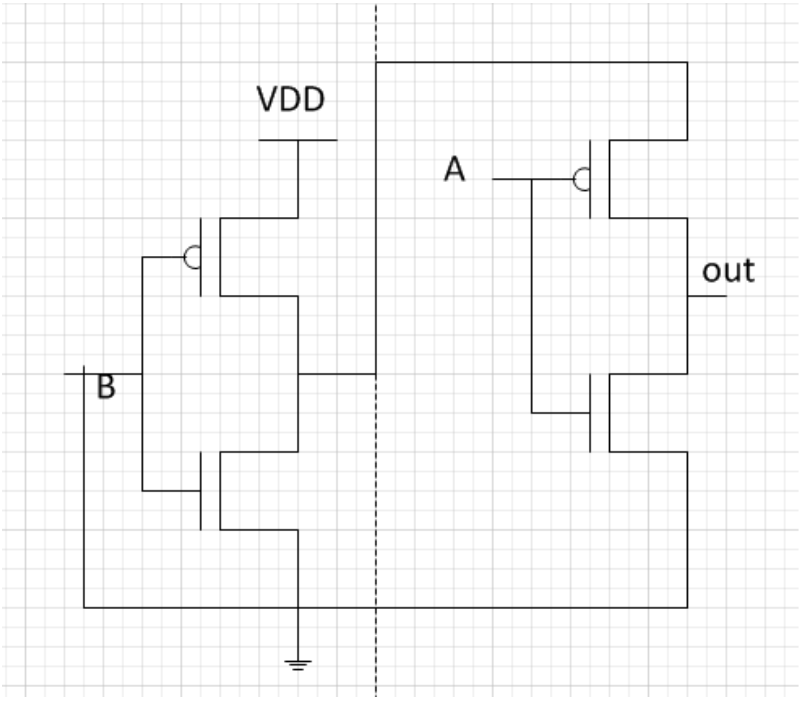

Fig: 8 gdi xor gate

the schematic of gdi xnor gate as shown in below:

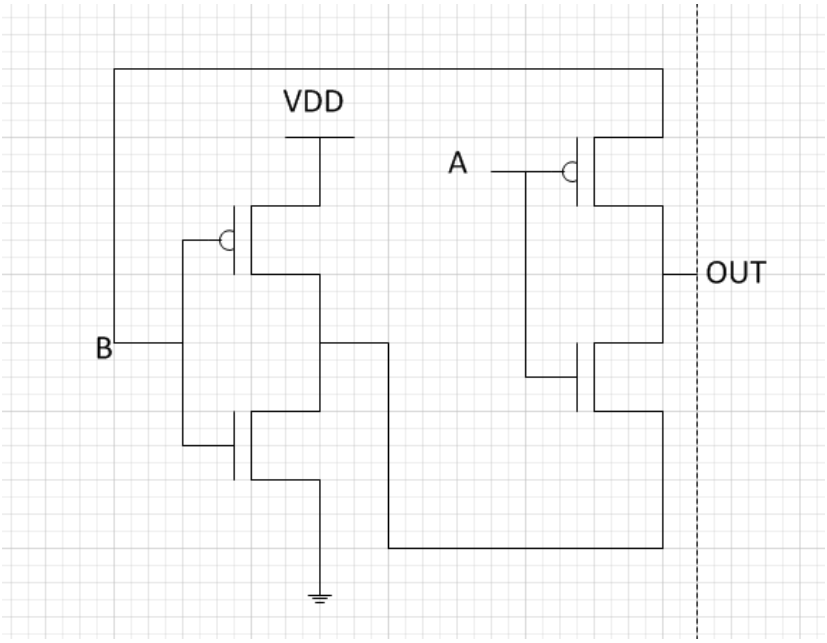

Fig :9 gdi xnor gate

The transistor level implementation of gdi xnor full adder as shown in below. It attains 4t delay for sum and 3t delay for cout in worst case. this gdi xnor full adder attains the low power constumption.

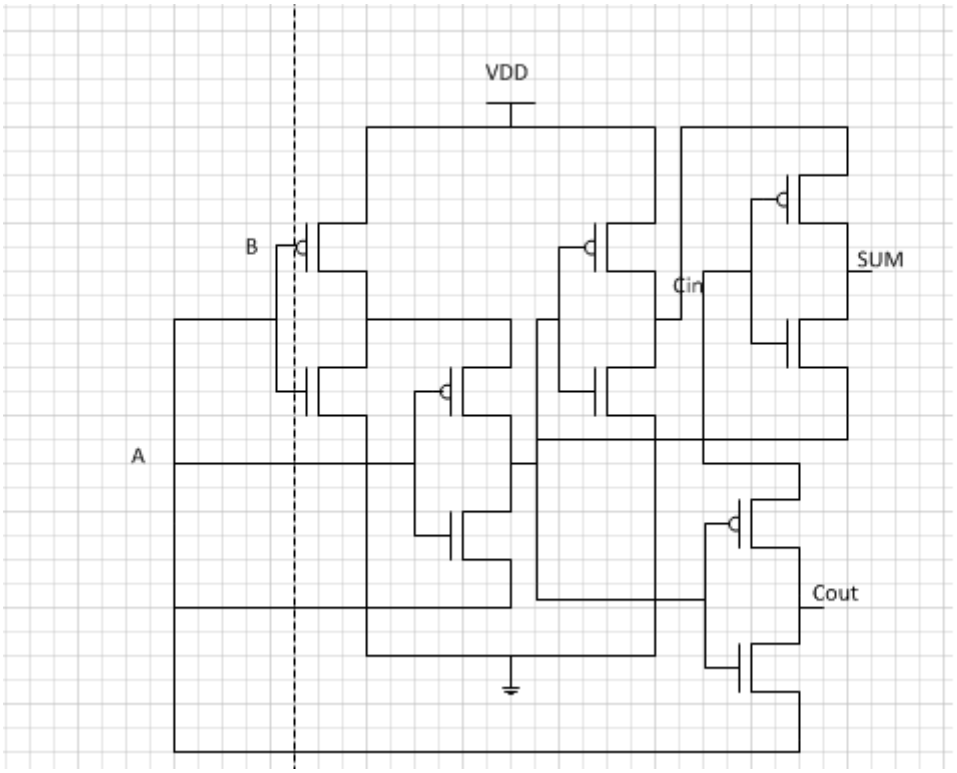

Fig:10 gdi xnor full adder

4) 4:2 compressor:

4:2 compressor attributes 4 inputs and carry-out. This implementation involves better critical path delay of 3 xors and hence reducing the critical path by 1 xor delay. The equations and schematic for 4:2 compressor as shown in below.

$$Sum=(x1 \oplus x2).\overline{X3 \oplus x4}+\overline{(x1 \oplus x2).(x3 \oplus x4)}.cin+\overline{(x1 \oplus x2).x3 \oplus x4+\overline{(x1 \oplus x2).(x3 \oplus x4)}.cin}$$

$$Cout=(x1 \oplus x2).x3+\overline{(x1 \oplus x2)}.x1$$

$$Carry=(x1 \oplus x2 \oplus x3 \oplus x4).Cin+\overline{(x1 \oplus x2 \oplus x3 \oplus x4)}.x4$$

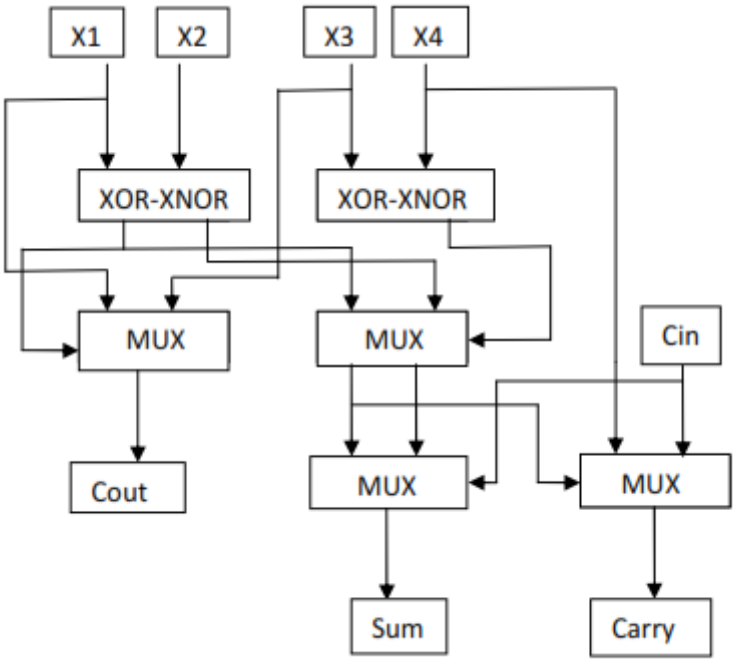

Fig 11 4:2 compressor block

5) 5:2 compressor:

5:2 compressor is widely used for high precision and high speed multipliers. 5:2 compressor attributes seven inputs and four outputs. Five inputs are the primary inputs such as x1,x2,x3 x4 and x5, and other two inputs cin1 and cin2 tottaly contains seven inputs with same weight receive their values from neighboring compressor of one bit binary lower significance. And three outputs cout1,cout2, and weighted one bit binary order.the equation and schematic for 5:2 compressor as shown in below.

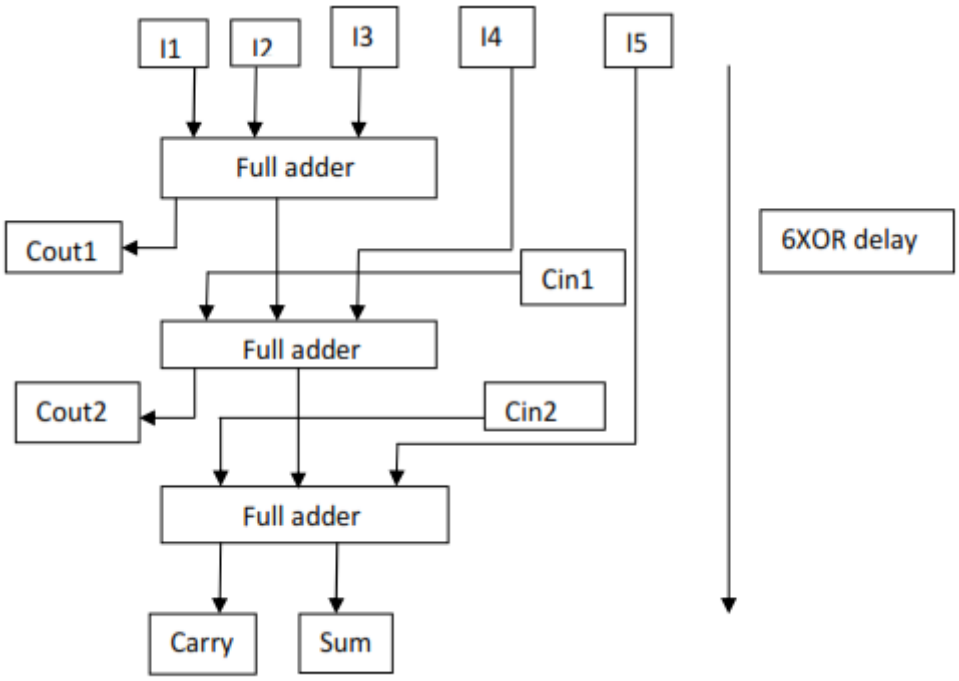

Fig:12 Compressor using full adders

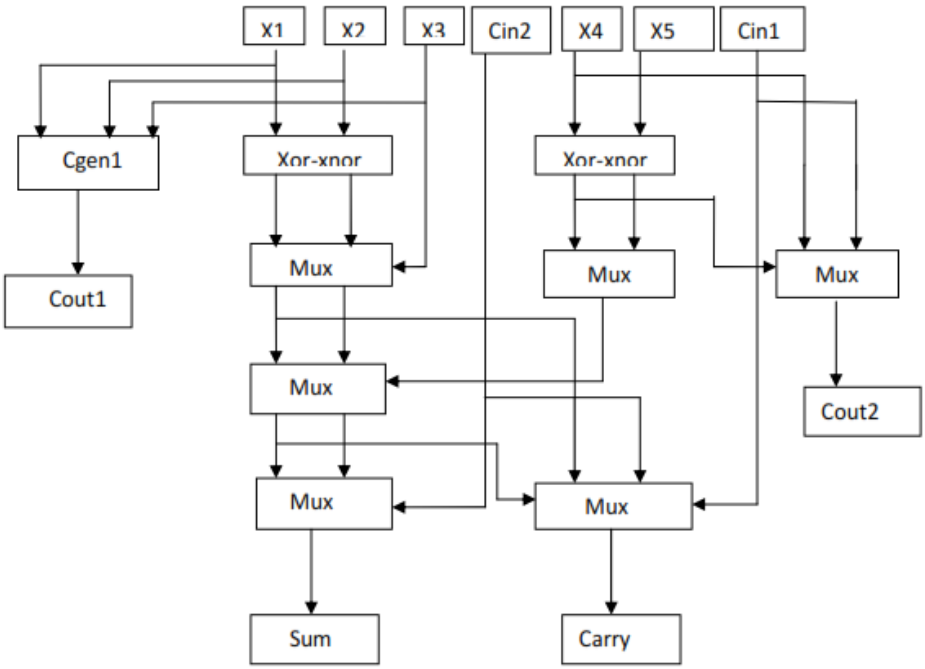

Fig :13Compressor block with xor-xnor

III. Result and simulation analysis:

Here we are described about different type of adders and compressors.all the analysis are done in cadence virtuso.the layout of adders are shown in below and the result analysis and plotted graphs.

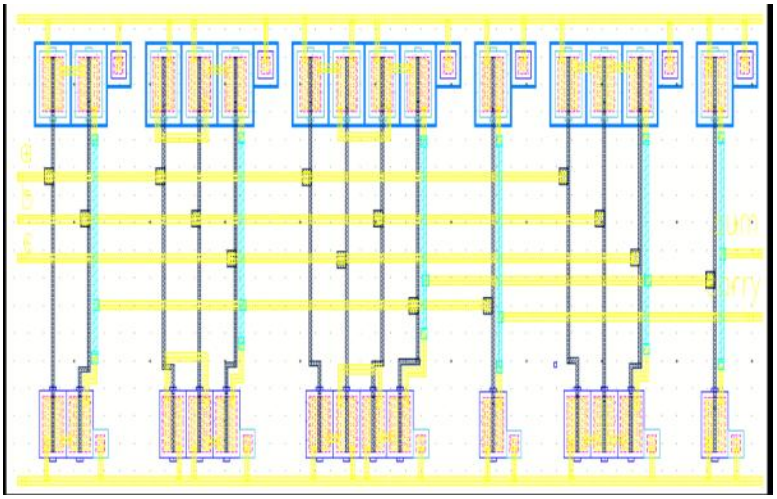

Fig :14 layout of csfa

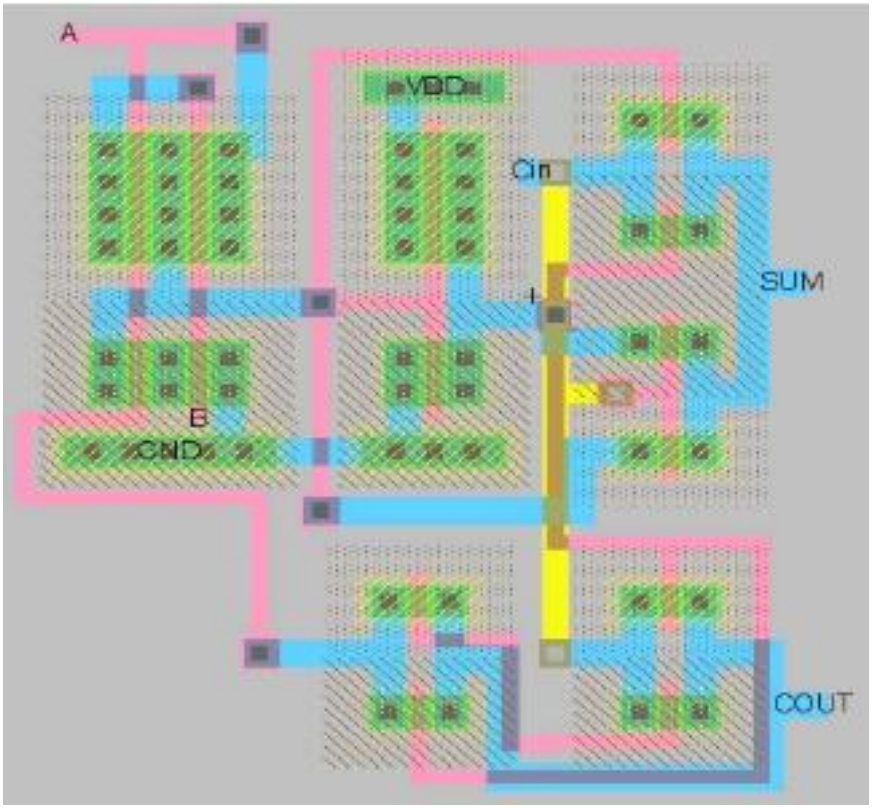

Fig :15 layout of tgbfa

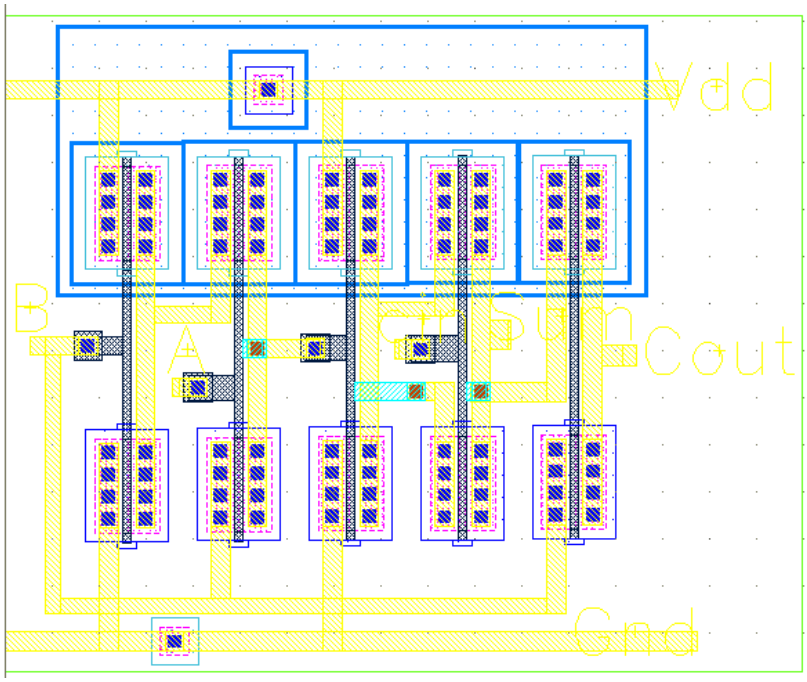

Fig :16 layout of gfa

The plotted wave forms as shown in below:

Fig:17 Conventional cmos full adder wave form

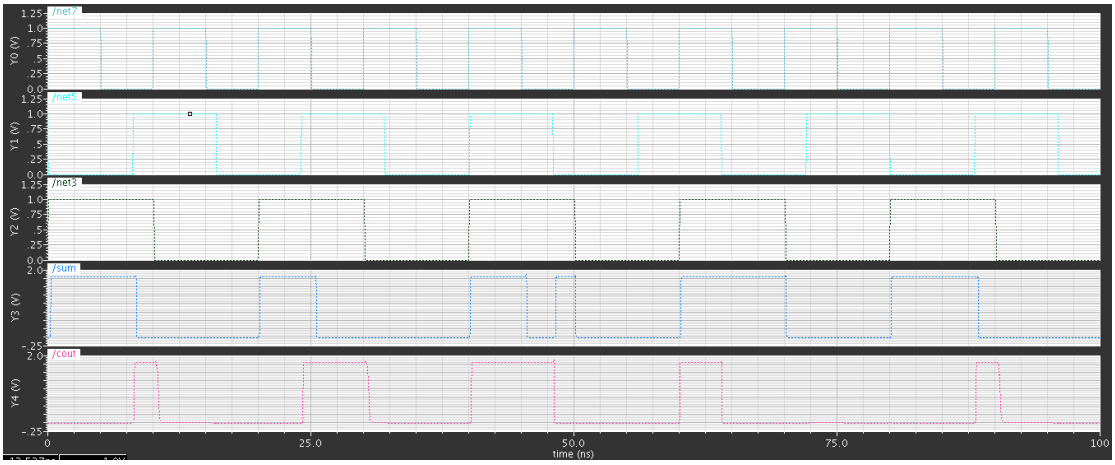

Fig:18 transmission gate full adder wave form

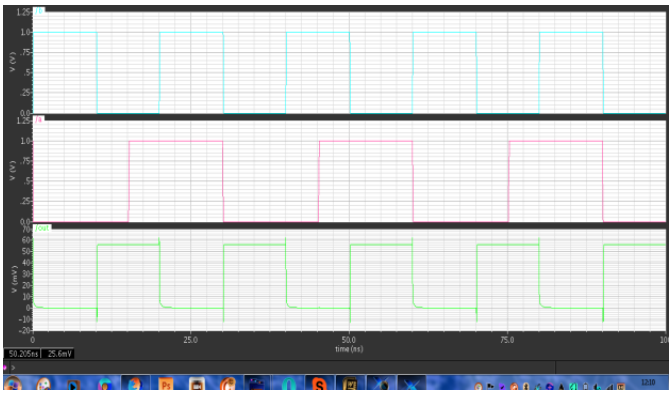

Fig:19 gdi xor wave form

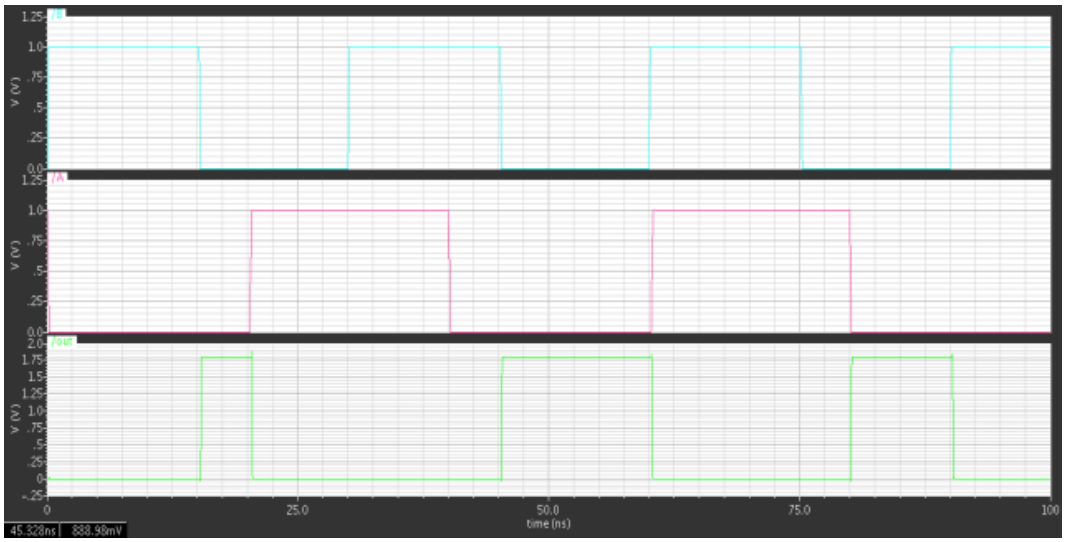

Fig:20 gdi xnor wave form

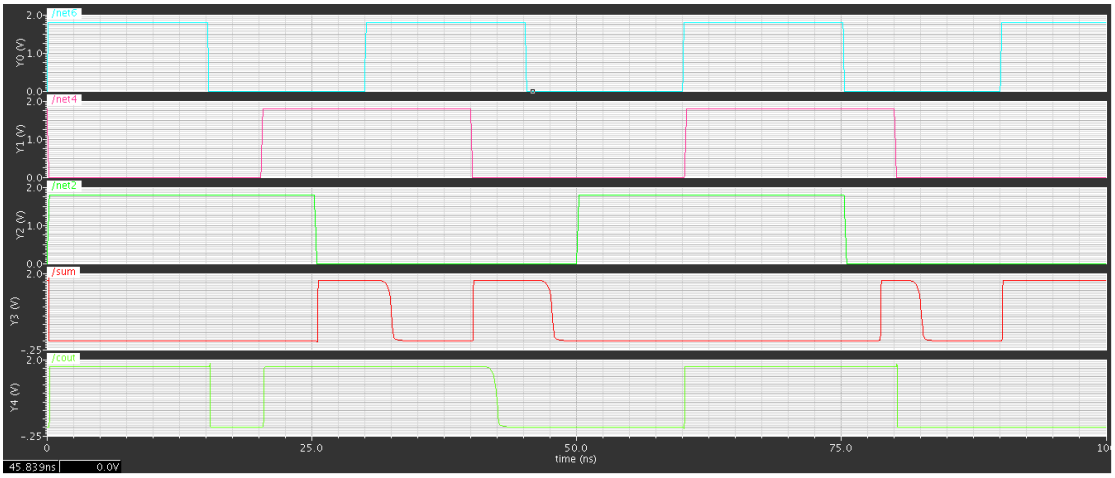

Fig:21 gdi xnor full adder wave form

Comparison in terms of delay, using different type of adders as shown in below.

Input			Conventional CMOS Fulladder(ns)		Transmission Gate Fulladder(ns)		GDI-XNOR Fulladder(ns)	
A	B	Cin	Sum	Cary	Sum	Carry	Sum	Carry
0	0	0	0.44	0.27	0.5	0.32	0.1	0.48
0	0	1	0.02	0.71	0.01	0	0.63	2.29
0	1	0	0.26	0.18	0.87	0.67	0.6	0.33
0	1	1	0.31	0.91	0.2	0.14	0.87	0.14
1	0	0	0.71	0.38	0.18	0.32	0.16.	0.32
1	0	1	3.21	0.06	0.63	0.91	0.38	0.01
1	1	0	0.15	0.27	0.4	0.46	0.06	2.3
1	1	1	0.31	0.63	0.06	1.81	0.32	0.2
Average Delay(ns)			0.67	0.42	0.35	0.57	0.39	0.75
WorstCase Delay(ns)			3.21	0.91	0.87	1.81	0.87	2.29

Fig:22 tabulated results of delay

Power plays a crucial role in low power vlsi our main target is to attain the low power and high speed performance of the circuit.

In cadence virtuso tool we get the power caliculations in terms of the (ms).

Power caliculations for the different type of adders:

Name of the circuit	Power(mw)
Conventional cmos full adder	0.193mw
Transmission gate full ader	0.112mw
Gdi xnor full adder	0.57mw

Fig:23 tabulated results of power

Plotted graphs as shown in below:

Inputs(8-bit Multiplier And Multiplicand)	Average Power consumption in (mw)		
	Conventional Wallace tree Multiplier(3682)	Proposed Wallace tree multiplier(1532)	Percentage %
11100110*11001100	55.647	3.32	92.4%
11000100*00111000	48.84	3.91	91.7%

Fig:24 tabulated results of conventional and proposed results

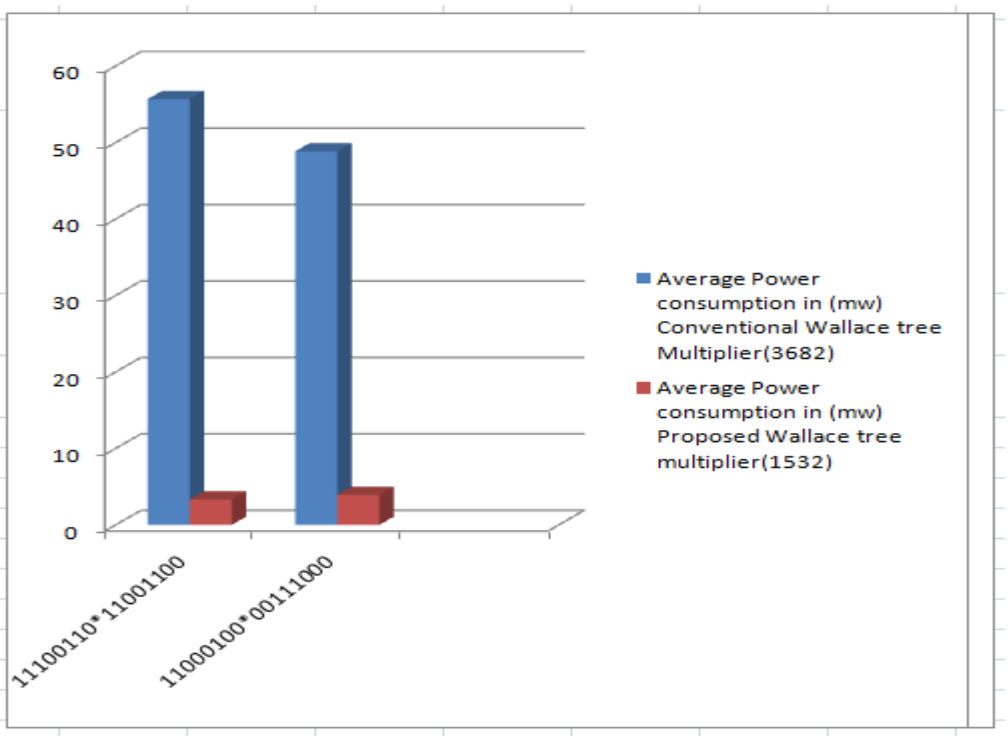

Fig:25 conventional results to proposed results

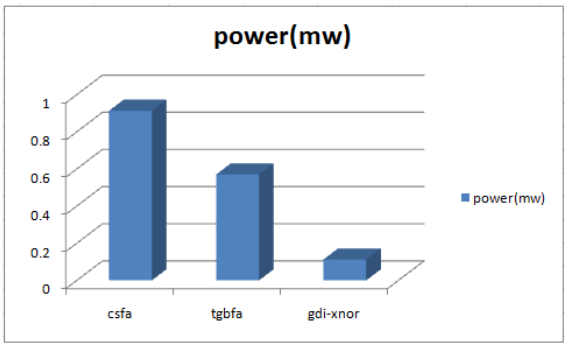

Fig:26 power calculations

III. CONCLUSION

After comparative analysis of various full adders, GDI XNOR full adder, transmission gate full adder and Conventional CMOS full adders are selected for Wallace tree multiplier. In this paper implementation of Wallace tree multiplier is made using TGA, GXFA and CSFA. After designing Wallace tree multiplier by using three different adder circuits, now it is a tread of situation. Where area and power are the main criteria, GXFA is a best suited and where speed is the only criteria, CSFA is best suited as an adder circuit. Whereas Wallace tree multiplier using TGA gives good result in all the criteria. It consumes little more area than GXFA but very less than CSFA. Results can be compared with and we can observe, 42% transistors are saved, results in reduction of area, and reduction in power at improved speed of operation.

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