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A 2.89ppm/°C Current Reference Generation with Temperature Compensation using 90-nm CMOS Circuit

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Abstract

This paper presents a low-power and low-voltage CMOS based reference current system, stable against temperature variation using 90 nm CMOS technology. Comparatively less power consumption of 2.02 µW is achieved by the circuit. The circuit is intended to compensate the variation in threshold voltage and mobility of MOSFETs with temperature. MOSFETs in this circuit are biased at their ZTC point to achieve temperature compensation and the circuit generates a reference current that is compensated against temperature variation. It attains a temperature coefficient of 2.89 ppm/°C for a drift of 20°C to 160°C.

Keywords-Current reference; low-power; temperature compensation; CMOS current reference; temperature coefficient(TC).

I. INTRODUCTION

The progress of ultra-low power based LSIs is a hopeful area of study in microelectronics. Low power based LSI applications are most suitable for portable and implantable medical systems. Such applications have to function with very low power, preferably, less than microwatts. The first step toward such LSIs, is to build up current and voltage reference circuits which is be capable of functioning with a very low current. The circuits operating in the subthreshold region, [1] is mandatory to accomplish such low-power operation. Current reference and voltage reference circuits are some of the most vital building blocks in analog and mixed-signal circuits. Current references are more commonly used than voltage references in complex analog circuits, where long metal lines are used. Unlike voltage references Current

references are independent of voltage drop in the interconnects. However, these circuits confront various problems like sensitivity of output current to variation in supply voltage and temperature. Therefore, current references which are stable against temperature are inevitable for exact operation of any analog, digital and power electronic system. A current reference circuit is mainly used to supply a bias current where high precision is essential. The bias current provided by a current reference circuit ensures the stable and precise operation of the analog circuit in which it is used.

The most familiar technique experimented for reference voltage or current generation is the bandgap reference method [2, 3]. In this method, the reference current or voltage is generated by combining the base-emitter voltage V_{BE} of a bipolar transistor, with the difference between the base-emitter voltages of two bipolar transistors ΔV_{BE}. V_{BE} has negative TC where as ΔV_{BE} has a positive TC. As they need high resistance to attain subthreshold operation, it require a huge area, and this makes conventional bandgap references inappropriate to be included in ultra-low power LSIs.

A Compact temperature-independent current reference was introduced to generate a temperature compensated reference current which contain five MOS transistors and two integrated resistors [4] using 0.35µm CMOS technology for a temperature ranging from-30°C to 100°C.TheTC attained by this system was 150ppm/°C. Another method using temperature and process compensation current mirror [TPC-CM] [5] was developed for a temperature ranging from 20°C to 100°C using 0.35µm CMOS technology. But it consumed large power. The current reference circuit involving subthreshold CMOS circuits [5], introduced a new method for generation of temperature compensated reference current. But that system failed to achieve a low TC below 600ppm/°C.

II. PROPOSED SYSTEM

The proposed reference current generation system has a voltage bias generation circuit, current generation circuit and a compensation circuit [8]. The current generation circuit is to generate a reference current, the bias generation circuit is to provide biasing for the current source transistor in the current generation circuit.

The V-I characteristics of MOSFETs shows negative TC. The principle parameters affecting drain current are mobility, threshold voltage, gate oxide capacitance and gate source voltage. Among these, mobility and threshold voltage are strongly dependent on temperature [9].

$$\mu(T) = \mu(T_o)\left(\frac{T_o}{T}\right)^{3/2} \tag{1}$$

where µ(T) is electron mobility at absolute temperature, T, and To is the reference temperature at which the value of reference mobility, µ(To), is measured.` When temperature is increased the [9] threshold voltage decreases. Thus, threshold voltage has a negative temperature coefficient.

$$V_T(T) = V_{T_o}\left(\alpha_{V_t} T + 1\right) \tag{2}$$

where αVt represent the temperature coefficient which is negative for threshold voltage. The gate oxide capacitance [9] also has a similar linear dependence. Therefore, it has negative temperature coefficient as explained by the equation:

$$C_x(T) = C_{x_o}\left(\alpha_{c_{xo}} T + 1\right) \tag{3}$$

Process variation largely occurs due to changes in doping concentration and gate oxide thickness. Threshold voltage and mobility of the MOS transistor get affected by these factors. As the current generated by current generation circuit varies with temperature as discussed above, a circuitry is to be added to compensate for the variation in the current. The circuit diagram for the current reference circuit is shown in figure 1.

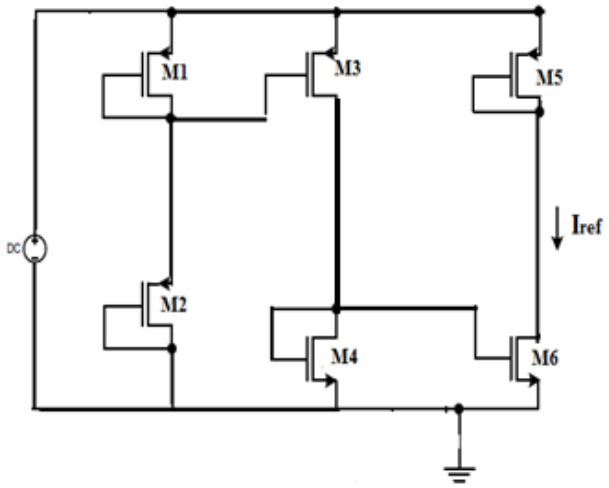

Fig.1. circuit diagram for the current reference circuit

In this circuit, some selected MOSFETs are allowed to be biased at their ZTC point (Zero Temperature Coefficient point), so that the current through them appears to be invariant with varying temperature. Transconductance characteristics for NMOS and PMOS were plotted separately for required temperature range and the point of convergence obtained in the plot is measured to be their ZTC point. Current and voltage will have a positive TC and a negative TC respectively below it's ZTC point, where as they have a negative temperature coefficient and positive temperature coefficient respectively above ZTC point. The current generation circuit is designed in 90 nm technology to produce a current of 5nA. But this current varies with variation in temperature. An additional circuitry is added for temperature compensation.

The current through M4 has a negative temperature coefficient. To counteract this variation, an additional circuit is designed such that it introduces a positive temperature coefficient in the mirrored current. The transistor M6 is biased below

their ZTC point, to have a positive temperature coefficient for current. The transistor M6 is made wide in order to operate the transistor below their ZTC point to accomplish high positive temperature coefficient. Transistor M5 is biased slightly below its ZTC point, and this tends to compensate for the negative TC current through M4.

The two MOSFETs, M3 and M4 operate in saturation region and are biased at their ZTC points to avoid the variation of current with temperature. The PMOS transistor, M3, acts as current source; and it is placed at its ZTC point by controlling its gate voltage. The transistor M4 is biased at its ZTC point and was designed to obtain required current. For a short channel MOSFET the saturated drain current[10] is given by

$$I_D = C_{ox} W v_{sat} \left(V_{GS} - V_{th}\right) \tag{4}$$

where v_{sat} is saturation velocity within transistor.

The bias generation circuit is a voltage divider circuit formed by two diode-connected PMOS transistors (M1 and M2). The transistors chosen for bias generation circuit were all be of the same type; so that the characteristics of all the transistors will behave the same way over process variations.

The transistor M6 in correction circuit is a current mirror with respect to the transistor M4 in the current generation circuit. However, M4 and M6 are not matched transistors and therefore, M6 different ZTC point. As a result, M6 is biased below its ZTC point, which tends to compensate for the negative TC current through M4.

III. RESULTS AND DISCUSSION

A 5 nA Current reference is generated using 90 nm CMOS process. It is designed to produce a constant current over a temperature ranging from 20°C to 160°C. The circuit is designed to operate with a power supply of 1V.The transistor M4 in figure 1 is biased at its ZTC point. The ZTC point is identified as a point where transconductance curves of different temperature intersect. Figure 2 shows the transconductance characteristics for NMOS with a particular $\frac{W}{L}$ ratio. The curves meet at a voltage, V_{GS} =0.42V.This point is considered to be the ZTC point for NMOS over the temperature range of 20°C to 160°C.

The uncompensated circuit generates current with a stability of-3095ppm/°C. Figure 3 shows the current with negative temperature coefficient generated by current generation circuit. Current decreases from 3.8 nA to 1.6 nA as temperature increases from 20°C to 160°C.

A temperature compensated current generated in the compensation circuit has a TC of 2.89ppm/°C over a temperature ranging from 20°C to 160°C. The total power consumption was noted to be 2.02µW. Figure 4 shows a graph plotting output current with variation in temperature.

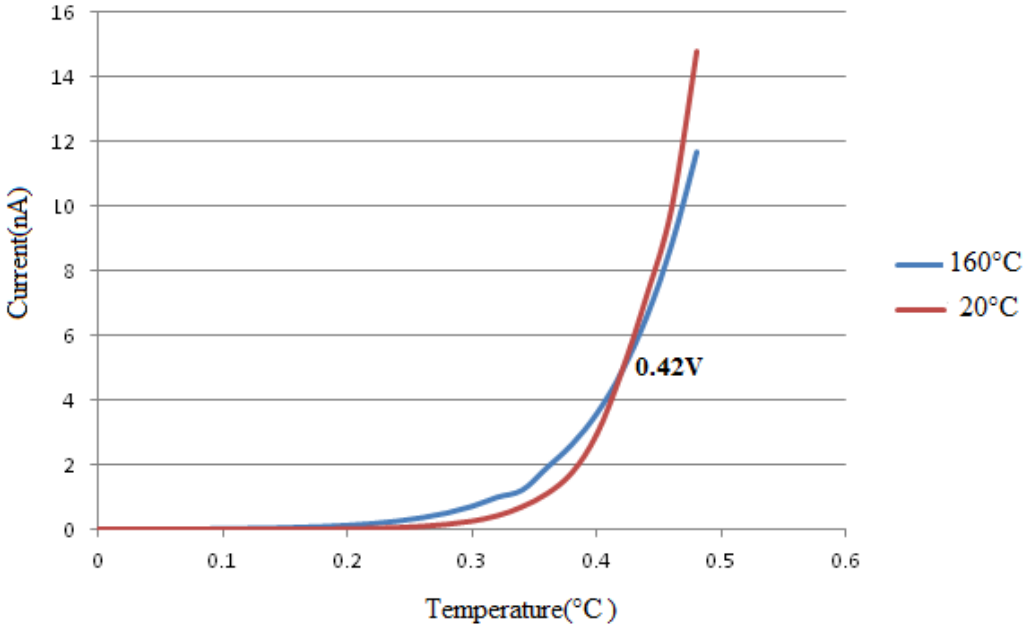

Fig.2. Transconductance characteristics for NMOS

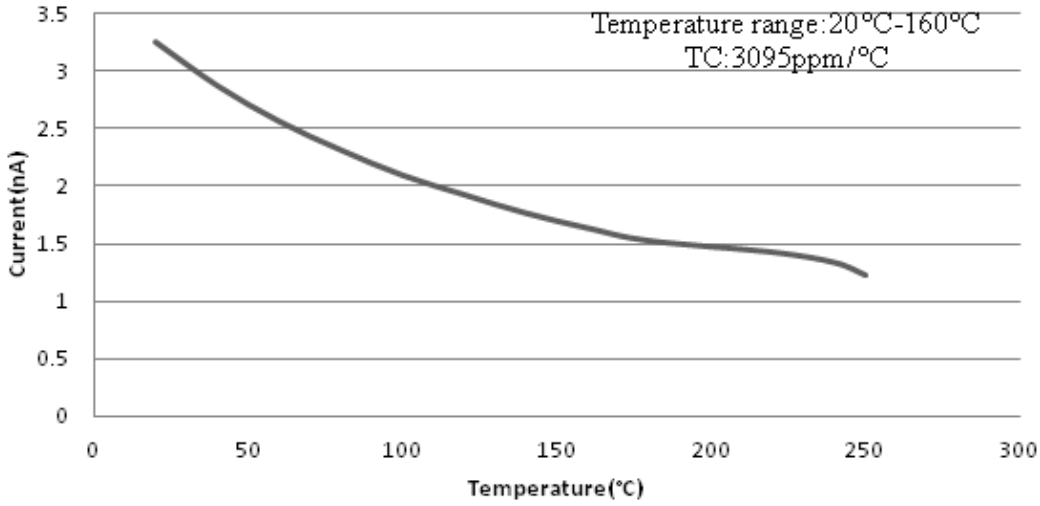

Fig.3. Current generated by current generation circuit

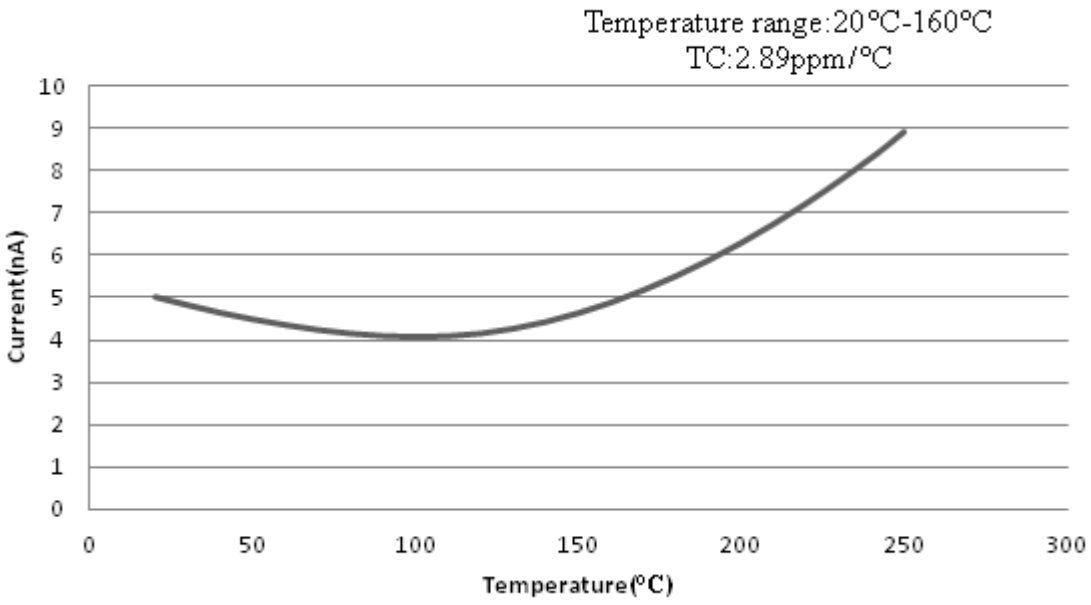

Fig.4.Output current verses Temperature

IV. CONCLUSION

A temperature compensated CMOS based current reference is discussed and simulated using 90nm CMOS technology process. The circuit achieves a stability of 2.89ppm/°C between 20°C and 160°C with a power consumption of 2.02µW.This performance of the circuit is compared with CMOS current references analyzed in the existing literature. Table 1 shows a comparison of current reference circuits discussed in literature.

TABLE 1. CURRENT REFERENCE CIRCUITS PERFORMANCE

	Franc Fiori [3]	Junghyup Lee [6]	Ken Ueno [5]	This work
Process	0.35µm	0.18 µm	0.35 µm	90nm
Voltage supplied(V)	2.5	1.2	1.8	1
TC (ppm/°C)	28	24.9	600	2.89
Temperature range	-30°C-100°C	0°C-100°C	0°C-80°C	20°C-160°C
Power consumed	NA	1.4µW	1µW	2.02 µW

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