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Design of Two Stage CMOS Operational Amplifier with Enhanced Slew Rate for High Speed Applications

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Abstract

In this paper the design of two stage CMOS operational amplifier with enhanced slew rate has been presented. The circuit has been simulated using BSIM4 model with 50nm CMOS process. The simulation results show that the settling time for rising edge is 10ns and for falling edge transition is 60ns respectively. Results also show that with reduced compensating capacitor, the slew rate is further enhanced by 9.2mV/ns which takes 40ns for the output to reach the peak voltage of 400mV.

Keywords: Operational amplifier, CMOS, slew rate.

I. INTRODUCTION

The rapid increase in chip complexity which has occurred over the past few years has created the need to implement complete analog-digital subsystems on the same integrated circuit using the same technology. For this reason, implementation of analog functions in MOS technology has become increasingly important, and great strides have been made in recent years in implementing functions such as high-speed DAC'S, sampled data analog filters, voltage references, instrumentation amplifiers, and 'so forth in CMOS and NMOS technology [1]. In the recent years developments in the field of wireless communication and biomedical signal processing demand of analog circuits working on low supply voltages and reduced power dissipation has been increased.[2-3]. Operational amplifiers are key elements in analog processing systems and are an integral part of many analog and mixed signal systems. As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers in CMOS technology becomes more critical [4]. Number of rail to rail operational amplifier design based on the complementary PMOS and NMOS transistors and constant-gm has been reported [5-7]. Several

approaches have been reported for operational amplifier design by using both fully differential and pseudo-differential configurations respectively. The pseudo-differential structure requires the common mode feedback circuit (CMFB) for designing the operational amplifier [8-10].

In this paper the design of a two stage CMOS operational amplifier has been presented. The paper is organized in the following way. Section II contains the circuit of two stage operational amplifier. Section III contains the circuit structure for enhanced slew rate CMOS operational amplifier. Finally section IV shows the simulation results for the CMOS operational amplifier circuits.

II. DESIGN OF TWO-STAGE CMOS OPERATIONAL AMPLIFIER

Fig.(1) shows the schematic of a two stage CMOS operational amplifier design which is driving the 1pF load capacitor. In this configuration when a high input is applied to non-inverting input terminal, the transistor M2 turns on and the gate of the transistor M7 goes low. Due to the absence of any current source in series with the transistor M7, the load capacitor is charged quickly. The bias current of the differential amplifier limits the rate of change of output voltage because of displacement current through coupling capacitor. The displacement current arises due to any variation in the output voltage.

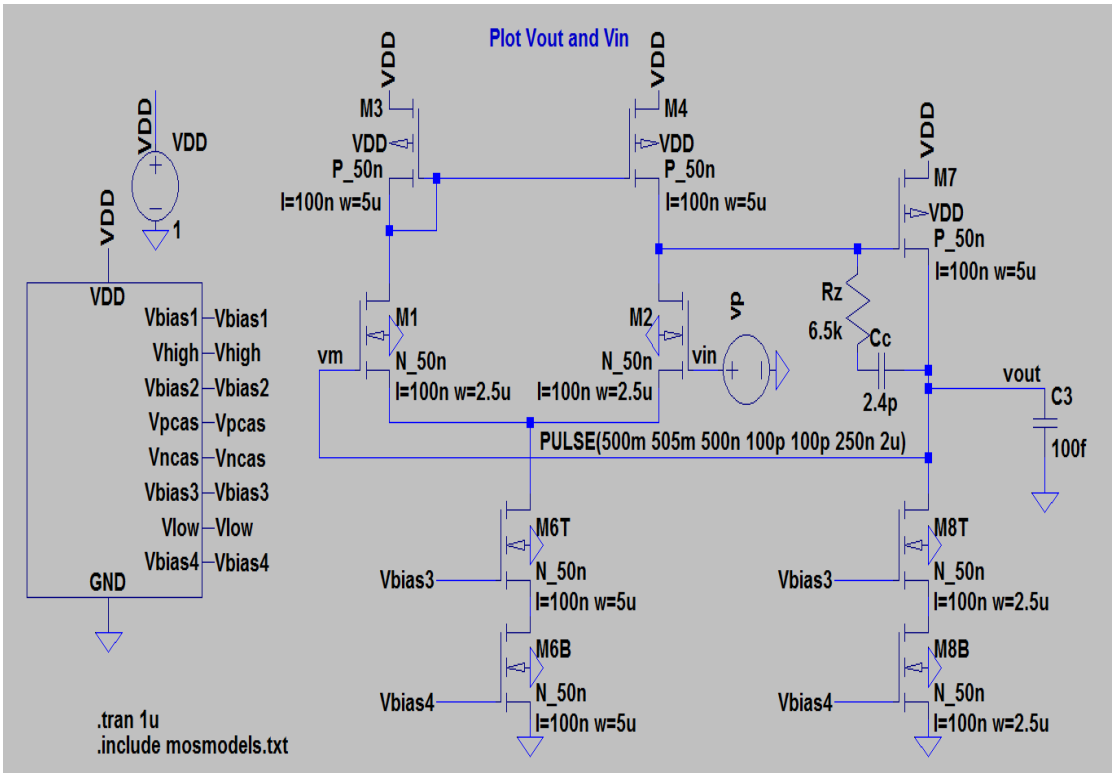

Fig.1: Two stage CMOS Operational Amplifier driving the load of 1pF.

III. CIRCUIT STRUCTURE FOR TWO STAGE CMOS OPERATIONAL AMPLIFIER WITH ENHANCED SLEW RATE

Fig. (2) Shows the circuit structure for the two stage CMOS operational amplifier with enhanced slew rate using the indirect compensation technique. In this design both the load capacitor and compensating capacitor are discharging through the transistor which is responsible for constant current source. The circuit also eliminates the additional power which is present in the schematic given by fig.(1). This is due to the current in the compensating capacitor is passing through the pull-up transistor to the output of the differential transistor.

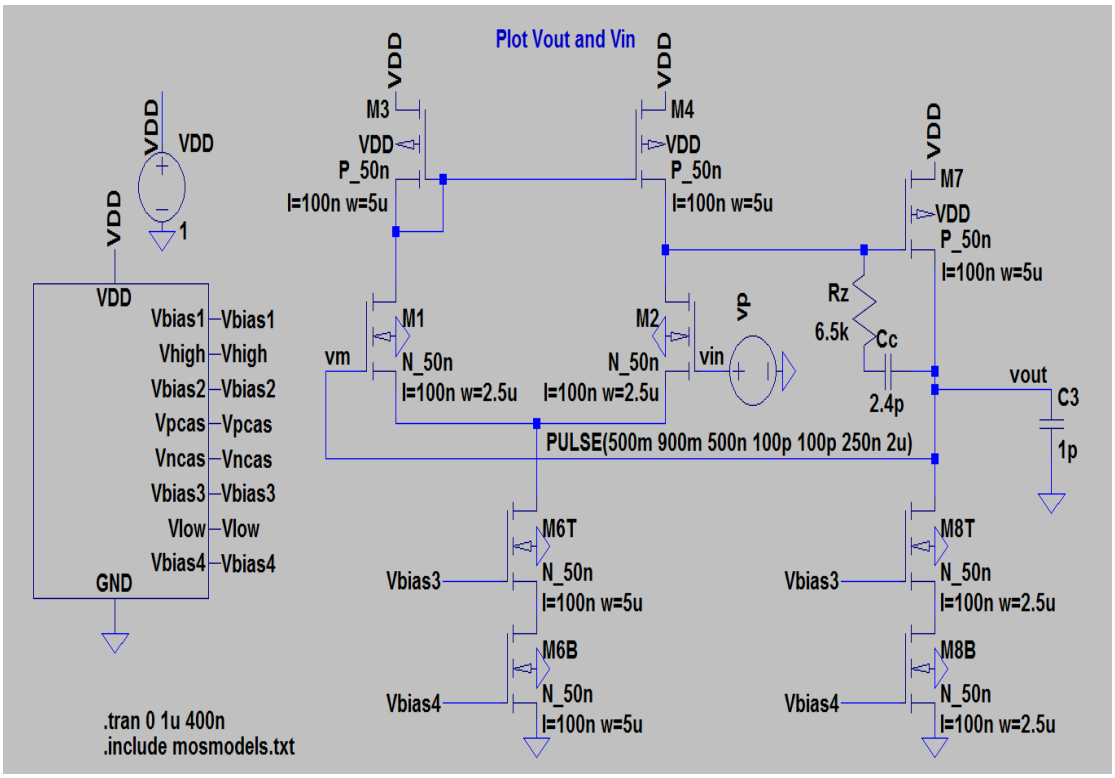

Fig.2: Circuit structure for the two stage CMOS operational amplifier with enhanced slew rate.

IV. RESULTS AND DISCUSSIONS

Fig (3) shows the simulated step response when an input pulse amplitude from 400mV to 800mV is applied to the operational amplifier circuit given by fig.(1). The result shows that it takes 40ns to change the voltage across the coupling capacitor since the variation in the output voltage is 350mV. When the signal changes from 800mV to 400mV, it takes 96 ms to settled the output voltage. Result also shows that a slew rate of 6mV/ns is obtained.

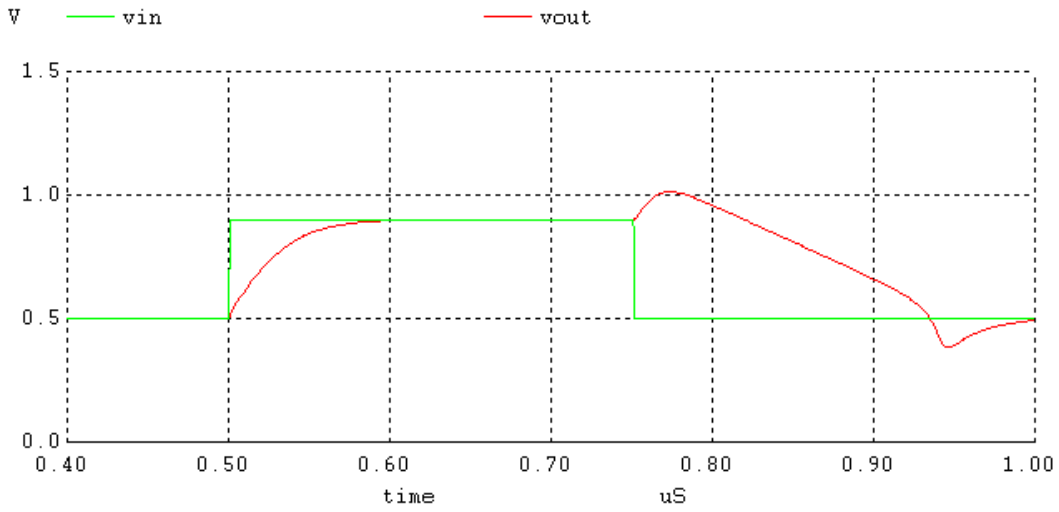

Fig.3: Simulated step response when an input pulse amplitude from 400mV to 800mV is applied to the operational amplifier circuit given by fig.(1).

Fig.(4) shows the simulated step response when the same input pulse (400mV to 800mV) is applied to the modified schematic given in fig.(2). Results show that the settling time for rising transition is 10ns whereas for the falling transition it is about 60ns. This reduction in the time is due to the reduced size of compensating capacitor which is about eight times smaller than the same for the circuit given by fig.(1). The response also shows that it takes about 40ms to settled the output voltage from 800mV to 400mV. Simulated result shows the slew rate for this design is 9.2mV/ns.

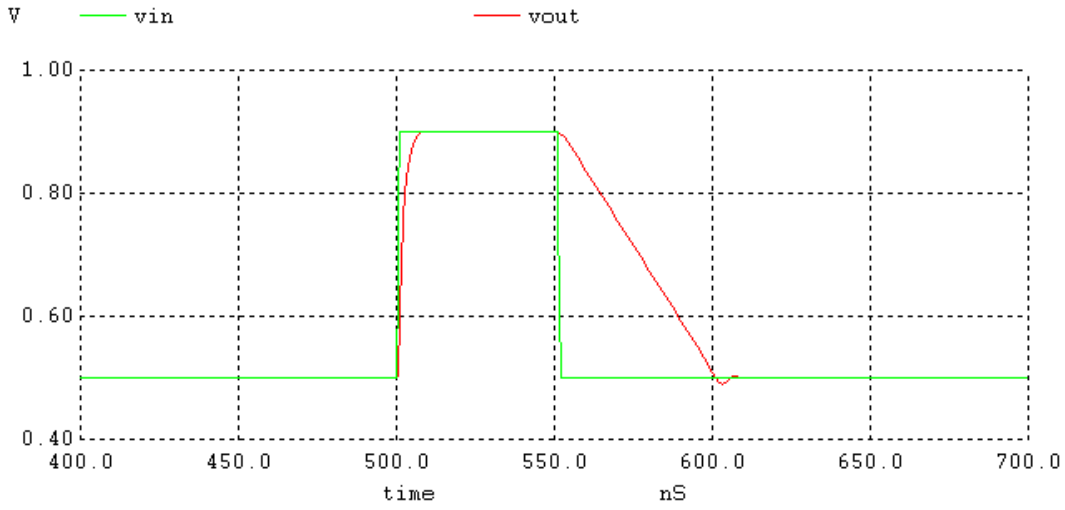

Fig. 4: simulated step response when the same input pulse (400mV to 800mV) is applied to the modified schematic given in fig.(2).

V. CONCLUSION

In this paper the design of a two stage CMOS operational amplifier with enhanced slew rate has been presented. Simulation results show that the operational amplifier takes 40ns to settled the output voltage from 800mV to 400mV. Results also show that the slew rate for this design is enhanced to 9.2mV/ns from the 6mV/ns.

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