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Capacitance Modeling of Single and Double-Walled Gate Wrap Around Carbon Nanotube Array Field Effect Transistor

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Abstract

Gate WrapAround Transistor is known for its good channel control than a planar gate devices.The electrostatic analysis of Single and Double-WalledGateWrap Around (SWGWA &DWGWA) CarbonNanotubearray Field Effect Transistors (CNTFET) is presented. Three major capacitances are theoretically modelled for dielectric strength of gate oxide(k1), Source/Drain length(Lsd), pitch distance between the channels(s), number of channels per gate(N), normal distance between gate and the channel(h)and gate height(Hgate). The screening and imaging effects of neighbouring channels and the individual walls are included.It is found that the proposed deviceanalysis shows improvedcapacitance values with increase in gate dielectric values, source/drain lengths,normal distance between gate and the channel and number of channels for DWGWA CNTFET. The capacitance values of device containing DWGWA are at least 1.6 times and at most 2 times greater than that of SWGWA CNTFET.The increase in s distance is limited by rate of decrement in capacitance values.This investigation projects an excellent benefit of using gate wrap around transistors with multi wall carbon nanotubes.

Index Terms: Gate-to-channelcapacitance(Cgc),fringe capacitance(Cof), gate to gate capacitance(Cgtg), pitch distance(s), Source/Drain length(Lsd) and gate height(Hgate).

Introduction

Most recently researchers turn their interest in disclosing the secrets hidden in small device structures.The nanostructures viz nanotube, nanowire, Nano beltandetc., has promisingperformancefor their application in electronic components.Nanowireor nanotube MOSFET has goodcontrol over theconducting channel because of

thecylindricalgate electrode as discussed by E.Ramayya et.al [1].AnisurRehmanet. al [2]intheir work, states that nanowire or nanotubeexhibiting onedimensions (1D) electron transport results in high mobility. This is because of reduced density of states for scattering and propagation modes.Carbon nanotube has emerged as an alternate material for larger to smaller structures ranging in nanometre scale. Particularly in electronics field, CNT transistors provide superior flexibility withencouraging presentation.

Benjamin Iniguez et. al [3] proposed charge-based modelling for double gate MOSFET, gate all around MOSFET and FinFET.From Poisson's equation, an analytical charge control model is obtained for developing full channel current and small-signal models. They found that Gate all around shows the best performance for both extrinsic and intrinsic devices.Bastien COUSIN et. al [4] presented a compact analytical modelling of quantum-mechanical effects for cylindrical Gate-All-Around MOSFET. It is found that the model suits for carrier confinement in the nanowire.The objective of modelling is to provide new device designs and to learnthe limitations. Modelling explores new device structures with different principles. MOSFET models are a) Charge control model, b) Meyer model, c) Velocity saturation model, d) Capacitance model, e) Small-signal model and f) Advanced MOSFET modelling.For simulating dynamic eventsin MOSFET, the stored charges of the devices that is, capacitance model has to be considered[5].

To develop the cumulative effect, multi channels is preferred over single channel. Planar gate capacitance with multiple cylinders is discussed by Jie Deng et.al[6]which gives an idea about the major capacitance distributions in cylindrical conducting channels. Modelling of array of cylindrical planar gate is done and accurately analysed for 1-D devices. They modelled gate capacitance comprising of gate channel, fringe and gate to gate capacitances including all screening and parasitic capacitances. Increasing the number of channels in the array and gate height will increase the device speed they concluded.DWCNTis the simplest form of multiwall CNT. It provides high current and power handling capacity due to good thermal, mechanical and electrical properties. Double walled array of planar gate is analytically modelled and the device performance is studied byJunZh. Huang et.al[7]. All screening and imaging effects of neighbouring as well as the individual walls are considered. It is found that the delay can be decreased by 15% and cut off frequency can be increased by 30% using the double-walled channels in array.Three major capacitances a) gate-to-channel, b)fringe& c) gate-to-gate capacitance are modelled for gate all around array of parallel and cylindrical conductors by Md. RakibulKarimAkanda et.al [8]. The proposed model for 1-Dgate wrap around device shows remarkable improvement over that ofplanarin [6].Carbon nano tube is studied for its intrinsic characteristics and high device performance by J.Appenzeller [9] and declares that CNT offer intrinsic advantage with high mobility and ultra-thin body channel. Also, scaling down is necessaryto meet the above advantages and co-axial gate allows optimum gate channel control.

In this research paper, the advantages of bothcylindrical array Gate Wrap Around and double-walled channelled CNTFET are taken for the electrostatic device analysis;single-wallis comparedwithdouble-wall channelled arrayof gate wrap around

CNTMOSFET device. It is found that the double-wall channelled device exhibits improved performance in its capacitance values than that of single-walled channel.Channel is considered to be intrinsic while source and drain are heavily doped. Here, key capacitances are modelledand studied for variousparameters such as dielectric value of gate oxide(k_1), the pitch distance between the channels(s), the normal distance of the gate and channel(h), Source/Drain length(Lsd) and the number of channels(N)for study. It is found that,higher the dielectric value of gate oxide, greater the performance of the device capacitance. Increasing's','Lsd','h' has their own limitations. More number of channels provides appreciable improvement in the capacitance value.

The paper is so organised that the distribution of the capacitances of the device is dealt in Section II, the modelling equations for calculating various capacitances of the device in Section III, the results and discussions with plots in Section IV and the conclusion inSection V.

Capacitance Distribution

For simple discussion three channels are taken. Gate oxide is taken with high κ dielectric material 'κ1'and for substrate the dielectric value is 'κ_2'. The distance between the centre of the adjacent channels being's',the diameter of the outer wall is 'd_o' and that of inner is 'd_I'.The outer and inner diameters of the channels are 2 and 1.34nm respectively. The device structure is supported on Si base. Fig.1.2 illustrates the distribution of gate-to-channel capacitances and fringecapacitances respectively. 'h' is the distance between the centre of the cylinder and the metal gate. The inner and outer wall radius of the walls is denoted as r_I and ro respectively. Fig.3. shows thereal charge Q and its image charges Q1 and Q2 and fig.4 depicts the charge profile of the channel. Let A and B are adjacent channels, Q1 and Q2 are the image line charges of Q, while Qo and QIdenotes charge of outer wall, inner wall of the channel. The neighbouring channelseffects each other,the individual wallsdisturbs each otherto cause a parasitic capacitance called fringing capacitance due to screening and imaging effects. These parasitic capacitance tends to reduce the total outputcapacitance which has to be considered carefully while designing nano devices.

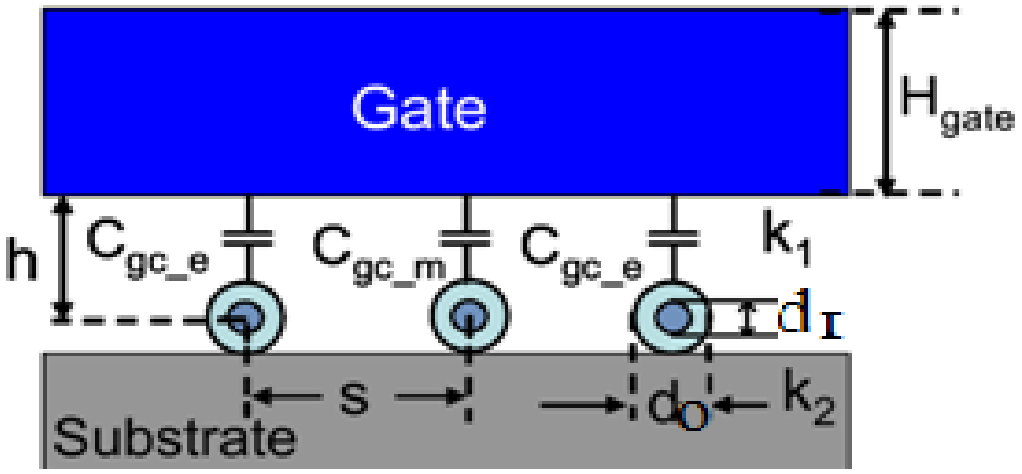

Figure 1: Distribution of Gate to Channel Capacitances

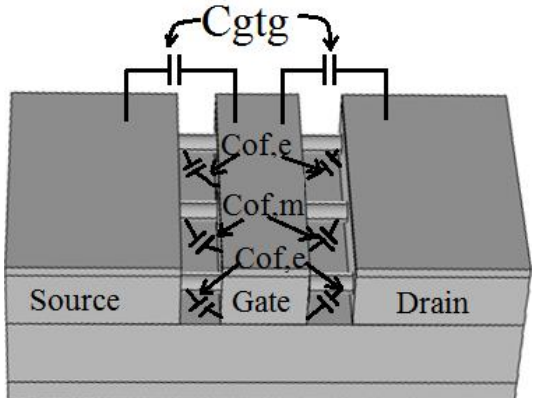

Figure 2: Distribution ofFringe capacitances and Gate-to-gate Capacitance

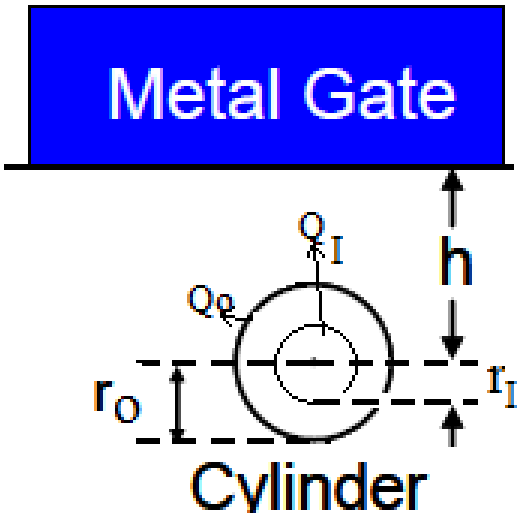

Figure 3: The real charge Q and its image charges Q1 and Q2

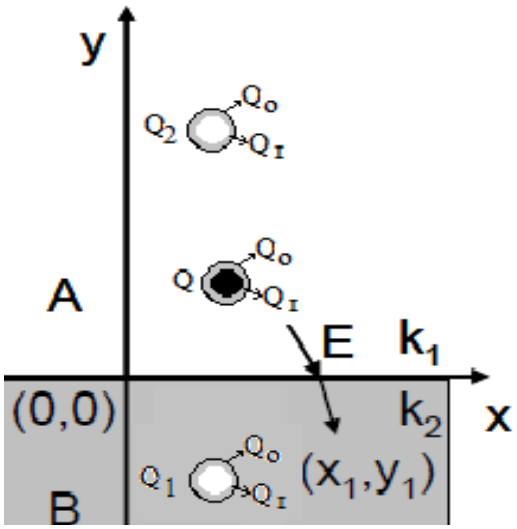

Figure 4: Charge Profile of A Cylinder

Capacitance Modelling

The key capacitors that are modelled in this paper are

1. The capacitance between gate and channel (Cgc)
2. The fringe capacitance (Cof)
3. The gate-to-gatecapacitance or capacitance between gate and source or drain(Cgtg)

Gate To Channel Capacitance(C_{gc})

The role of*Cgc* is significant in determining the drive current of the device. The screening effects of neighbouring parallel cylinders and imaging effects of individual walls are taken for consideration for modelling *Cgc*.Fig.4a.indicates the real charge Q and its image charges Q1 and Q2,Fig.4b.depicts charge profile of a cylinder. Two real and image line charges, one due to mirroring effect of metal gate and the other image line charge λ_1Qdue to$\kappa_1 \neq \kappa_2$are taken. In addition to the potential difference caused by the individual cylinders there is potential difference due to screening effects of neighbouring cylinders.

Gate to channel capacitance *(Cgc)*ofDWCNT is oftwo parts, i.e. Capacitancebetween

1. Gate and outer wall of the channel *(Cgc,o)* and
2. Gate and inner wall of the channel*(Cgc,I).*

Cgc,o is calculated as in [7] and [8].

$$Cgc,o = \frac{1}{\frac{1}{Cgc,o^{(o)(o)}} + \frac{1}{Cgc,o^{(o)(I)}}} \quad (1)$$

Where, $Cgc,o^{(o)(o)}$- Gate channel capacitanceof the outer wall and the screening effects of other DWCNT.

$Cgc,o^{(o)(I)}$- Gate channel capacitancedue to screening effectsof the inner wall.

$Cgc^{(o)(o)}$is furtherdivided into$Cgc,e^{(o)(o)}$and $Cgc,m^{(o)(o)}$.The first case is for the channels at end of the array and the second is for the middle ones. $Cgc,e^{(o)(o)}$is effected by the neighbouring channel at one side alone whereas$Cgc,m^{(o)(o)}$is effected by channels at both the sides. They are calculated from [7],[8]and [9].

$$Cgc,o^{(o)(o)} = \begin{cases} Cgc,e^{(o)(o)} = \frac{Cgc,inf.Cgc,sr}{Cgc,inf+Cgc,sr} \\ Cgc,m^{(o)(o)} = 2.Cgc,e^{(o)(o)} - Cgc,inf \end{cases} \quad (2)$$

Where, *Cgc,inf* -is the gate channel (outer wall) capacitance without any screening effects.

Cgc,sr- the equivalent capacitance includingthe screening effects of the other channels in the array.

Cgc,inf is calculated as in [9] for cylindrical GWA CNTFET,

$$Cgc,inf = \frac{2\pi\kappa_1\varepsilon_0}{cosh^{-1}\left(\frac{2h}{d_o}\right)+\frac{1}{3}\lambda_1 ln\left(\frac{2h+2d_o}{3d_o}\right)} \quad (3)$$

Where,λ_1- is the pre-factor that accounts for the interface of dielectrics κ_1 and$\kappa_2$with different values, calculated as in [7][9].The above equation is similar to the planar gate [7] & [8], the term $\frac{1}{3}$stands for gate all aroundtransistors. Similarly suchtermsin (5),(11),(12) &(13) are highlighted in bold blue font.

$\lambda_1 = \frac{\kappa_1-\kappa_2}{\kappa_1+\kappa_2}$(3a)*Cgc,sr*is estimated by taking

a) The potential drop between gate and outer wall and
b) The potential drop due to the screening effects of the double walls of the neighbouringDWCNT [8].

$$Cgc,sr = \frac{1}{\frac{1}{Cgc,sr^{(o)(o)}}+\frac{1}{Cgc,sr^{(o)(I)}}} \quad (4)$$

Where,$Cgc,sr^{(o)(o)} =$

$$\frac{4\pi\kappa_1\varepsilon_0}{ln\left(\frac{s^2+2(h-r_o).\left[h+\sqrt{h^2-r_o{}^2}\right]}{s^2+2(h-r_o).\left[h-\sqrt{h^2-r_o{}^2}\right]}\right)+ln\left(\frac{s^2+2(h-r_o).\left[h+\sqrt{h^2-r_o{}^2}\right]}{s^2+2(h-r_o).\left[h-\sqrt{h^2-r_o{}^2}\right]}\right)+\lambda_1 ln\left(\frac{(h+d_o)^2+s^2}{9r_o^2+s^2}\right).tanh\left(\frac{h+r_o}{s-d_o}\right)} \quad (5)$$

Here,

$$Cgc,sr^{(o)(I)} = \frac{Q_A^{(o)}}{Q_A^{(I)}} Cgc,sr^{(o)(o)} \quad (6)$$

$$Cgc,o^{(o)(I)} = \frac{Q_A^{(o)}}{Q_A^{(I)}} Cgc,inf \quad (7)$$

Next is to find outGate and inner wall of the channel*(Cgc,I)* [8],which comprises of

1. The effects of inhomogeneous gate dielectric and the imaging effects of other neighbouringGWADWCNT.
2. The imaging effects of the outer wall.

$$Cgc,I = \frac{1}{\frac{1}{Cgc,o^{(I)(o)}} + \frac{1}{Cgc,o^{(I)(I)}}} \quad (8)$$

$$Cgc,I^{(I)(o)} = \frac{Q_A^{(I)(o)}}{Q_A^{(o)}} Cgc,o \quad (9)$$

$$\mathrm{Cgc,I^{(I)(I)}} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{d_o}{d_I}\right)} \quad (10)$$

Where,do and are $d_I$diametersof the cylinder
*a*isLattice Constant(2.49A°)

Fringe Capacitance (C_{of})

The capacitance between gate and source *(Cgs)*,the capacitance between gate and drain *(Cgd)*,the capacitance between gate and the channel*(Cfrg,g)*, capacitance between the substrate and channel (Cfrg,sub)areclassified as Fringing capacitance. Being a strong function of device geometry, importance of fringing capacitance lies in evaluating the device speed accurately[9]. The outer fringing capacitance *(Cof)*alone is considered here and other fringes are out of scope of the work.*Cof* is assumed to be independent of *Hgate* and divided into two categories. One at the ends *Cof,e* and the other at the middle *Cof,m* same way as the method followed to do*Cgc*.
For wrap around gate FET,

$$Cof,m = \frac{2\alpha}{\eta_1} Cof,e + \left(\frac{1-2\alpha}{\eta_1}\right).\left(\frac{\pi\kappa_2\varepsilon_0 Lsd}{1/3 cosh^{-1}\left(\frac{(4h^2)+(0.56Lsd)^2}{d_o}\right)}\right) \quad (11)$$

Where,

$$\alpha = exp\left(\frac{N-3}{\tau_2 N}\right), N \geq 3 \quad (11a)$$

$$Cof,e = \frac{\pi\kappa_2\varepsilon_0 Lsd}{ln\left(\frac{(4h^2)+(0.56Lsd)^2+s^2}{s}\right) + ln\left(\frac{\sqrt{(s/2^2)}}{2}\right) + exp\left(\frac{\sqrt{Na^2-2N}+N-2}{\tau_1 N}\right) .\frac{1}{3} cosh^{-1}\left(\frac{(4h^2)+(0.56Lsd)^2}{d_o}\right)}, N \geq 2 \quad (12)$$

$\tau_1\tau_2$ are fitting parameters describing the rate of decrement in electric flux of the neighbouring cylinders with increase in distance between them.$\tau_1,\tau_2$are taken as 2.5 and 2.0 respectively from [9]

The gate-to-gate (or gate-to-S/D) coupling capacitance(C_{gtg}).

*Cgtg*is one more main capacitance and it can be separated into

1. Gate-to-gate fringe capacitance per unit length *Cgtg,fr*
2. Gate-to-gate plate capacitance per unit length *Cgtg,nr* due to normal electric field between the two channels.

*Cgtg*is the summation ofbothGate-to-gate fringe capacitance per unit length *Cgtg,fr and* Gate-to-gate plate capacitance per unit length *Cgtg,nr*.

$$C_{gtg} = \frac{3\kappa_2\varepsilon_0 H_{gate}}{Lsd} + \alpha_{gtg,sr}\frac{\pi\kappa_2\varepsilon_0}{ln\left(\frac{2\pi(Lsd+L_g)}{2L_g+\tau_{bk}\left(H_{gate}+h+r_O\right)}\right)} \quad (13)$$

$\alpha_{gtg}$is the factor due to screening effect of neighbouring conductors(Gate/Source/Drain)
(α_{gtg} = 0.7 for H_{adj} =H_{gate})
Where,

$$\tau_{bk} = \exp\left(\frac{\left(2-2\sqrt{1+2}(H_{gate}+L_g)\right)}{Lsd}\right), \quad (13b)$$

The drive capacitance is calculated [10] using the following relation,

$$C = C_g L_g + f_{miller}.2\left(C_{of}^{(g)}L_s + C_{gtg}W_{pitch}\right) + C_{gsub}$$

Where,
f_{miller}=1.5.

Results and Discussion

Single-walled and Double-walledGate Wrap Around array of CNTFET are analysedwith the chiralities of (26, 0) and (17, 0) for the outer and the inner walls of the channelrespectively. The diameter ofsingle walled channel is same as thatofthe outer wall of double wallchannel device. For simplicity, DWGWA CNTFET and SWGWA CNTFET are called as DWGWA and SWGWA respectively.The parametric values used for calculation are tabulated in TABLE 1. The gate to outer wall of thechannel capacitance is calculated for end and middleelement of the array of channels,similarly the fringe capacitance is also calculated for end and middle channels of the array. The equations for gate wrap around CNTare taken from [9] and substituted in the relations of array of double-walled channels [8]. New equations for gate wrap around double-walled array of channelled CNTFET are thus derived. The comparisons of SWGWA and DWGWA are plotted for studying the behaviour of the individual devices as well as to project the wellness of multi-wall channelled device. The effect ofgate oxide dielectric(k1), gate distance to the channel(h),pitch distance(s), source/drain length(Lsd), number of channels(N) and gate height(Hgate) onthe capacitances are studied.The example for each graph for the actual values is attached as annexure.

Table 1:

Details of Parametric Values		
S.No	Parameters	Values
1.	CNT Diameter(do,d_I)	2nm,1.34nm
2.	No.of CNT	3
3.	Oxide Thickness(Tox)	4nm
4.	Gate Dielectric	16
5.	Power Supply	0.9V
6.	Gate/Source/Drain(Lsd)	16/32/32nm
7.	Gate Height(Hgate)	12nm
8.	Pitch distance(s)	20nm
9.	Bulk dielectric Thickness(Hsub)	10μm
10.	Bulk dielectric Value(κ2)	4
11.	Flat Band Voltage	0V
12.	n11, n12	26,0
13.	n21,n22	17,0
14.	Lattice Constant(a)	2.49A°
15.	Temperature	100K

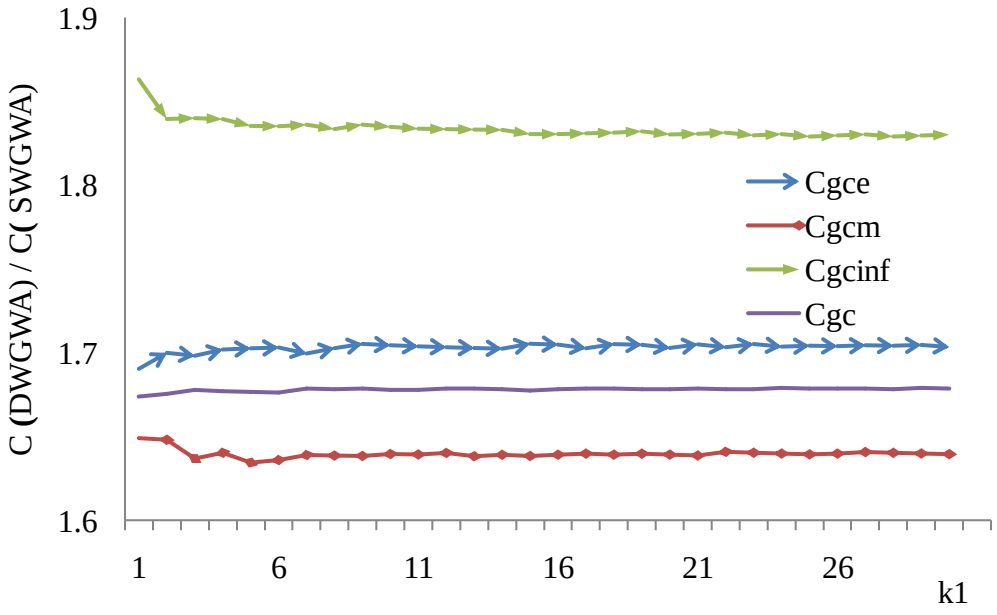

Figure 5: Capacitance ratio between DWGWA and SWGWA for different gate dielectrics

The Gate to Channel capacitances of middle (Cgcm), end (Cgce) channels of the array,the capacitances without any screening effects (Cgcinf)for DWGWA and

SWGWA with respect to gate dielectric values are compared. Fig.5. is the capacitance ratio between GWACNT for different gate dielectrics. From all these linear curves it is found that the slope of DWGWA is greater than SWGWA. Actual values are projected in A.1 of appendix. From the capacitance ratio graph, it is found that Cgcevalues ofDWGWA areabout 1.67 times greater,than that of SWGWA. The end and middle gate capacitances(Cgce,Cgcem) shows1.7 ,1.63 times greater value for DWGWA compared to SWGWA while in the case of the capacitance without screening effects it is 1,83 times greater for DWGWA than its counterpart. With all screening and imaging effects of neighbouring walls and channels of the array, thegate to channel capacitances (Cgc) for GWACNTshows that DWGWA gives higher values than its counterpart.This proves that DWGWA has more capacitance values than that of SWGWAand ratio increases with increase ingate oxide dielectric value.

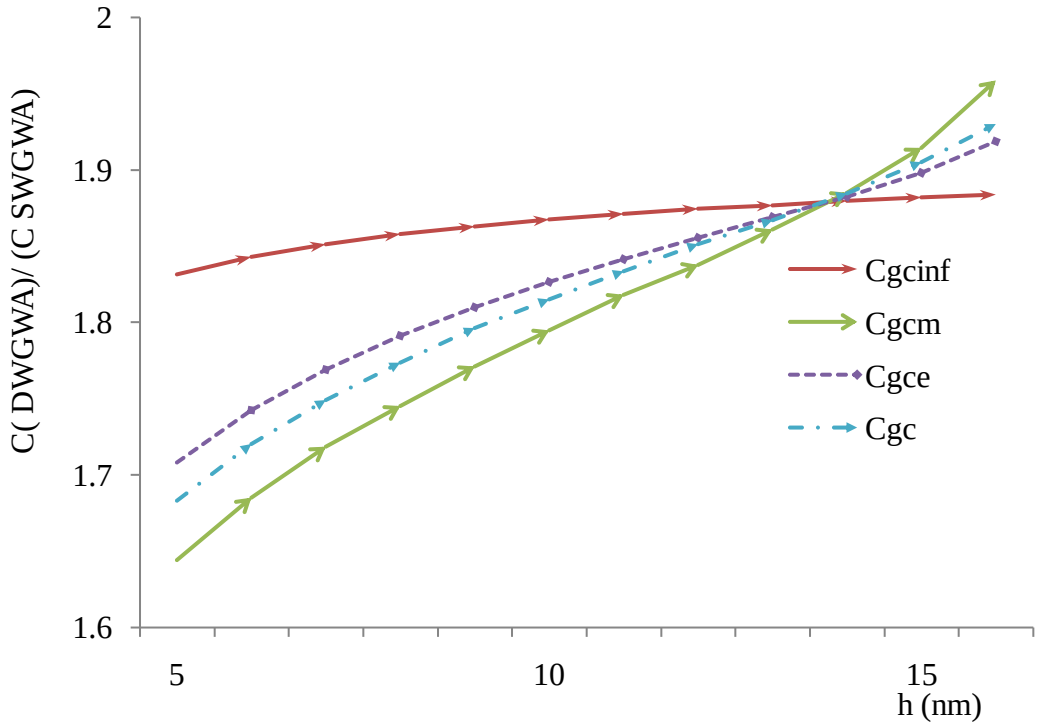

Figure 6: Capacitance ratio between DWGWA and SWGWA for various h distances

Variation of gate distance from the channel is one of the important parameter deending upon which the capacitance value varies. Fig.6 is the graph ofvarious gate capacitance componenets with respect to the distance of gate from the channel.From the capacitance ratio graph, the changes of (Cgce),(Cgcm),(Cgcinf) and(Cgc) are observed for GWACNT. Thevalue ofallcapacitances is more than 1.6 times for smaller h reaching about 1.9 times for 14 nm distance.Actual values are plotted inA.2 and A.3 of appendix. While designing such1-D devices care should be taken for the selection of'h' distance, since all curves meet at h=14nm after which Cgcmincreases,

Cgcinf maintains the same value and the other two curves follow the same rate of change.

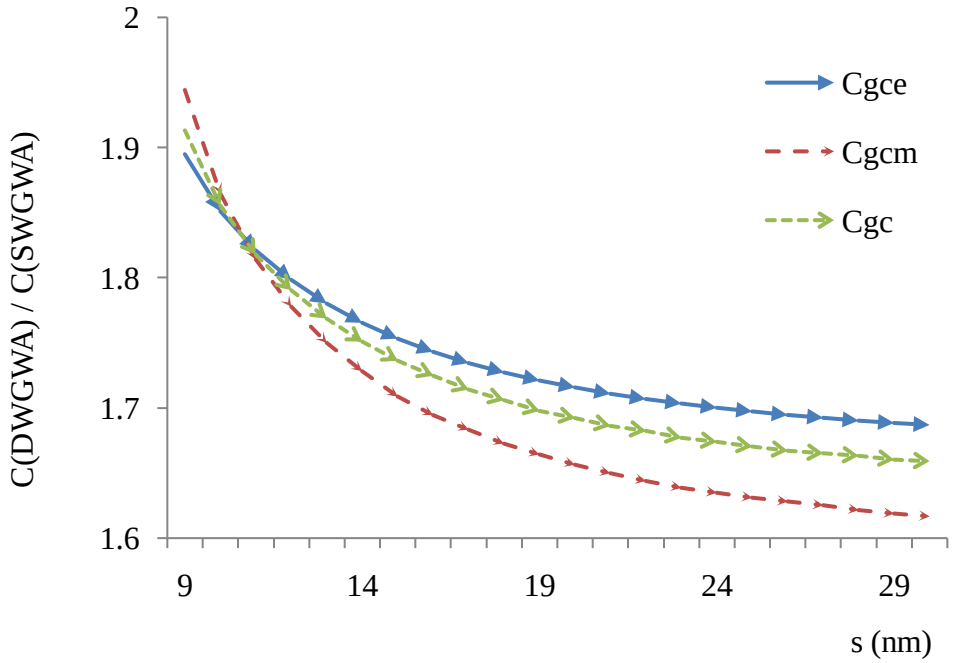

Figure 7: Capacitance ratio between DWGWA and SWGWA for different pitch distances.

The distance between adjacent channels disturbs the capacitance values with its screening and imaging effects. Therefore, it becomes necessary to read the corresponding changes. Fig.7 compares the Gate to channel capacitances of middle (Cgce) and end (Cgcm) channels of the array, the capacitances without any screening effects (Cgcinf), for various values of pitch distances along with all screeningandimaging effects of neighbouring walls. It is observed that the capacitance of the channels of the array (Cgc) for GWACNT are reducing with respect to increasing‘s’ distances.The reducing ratiowith increasing in ‘s’ distance showing the limitation of‘s’ distance. The corresponding values of the curves are in A4, A5 of annexure.

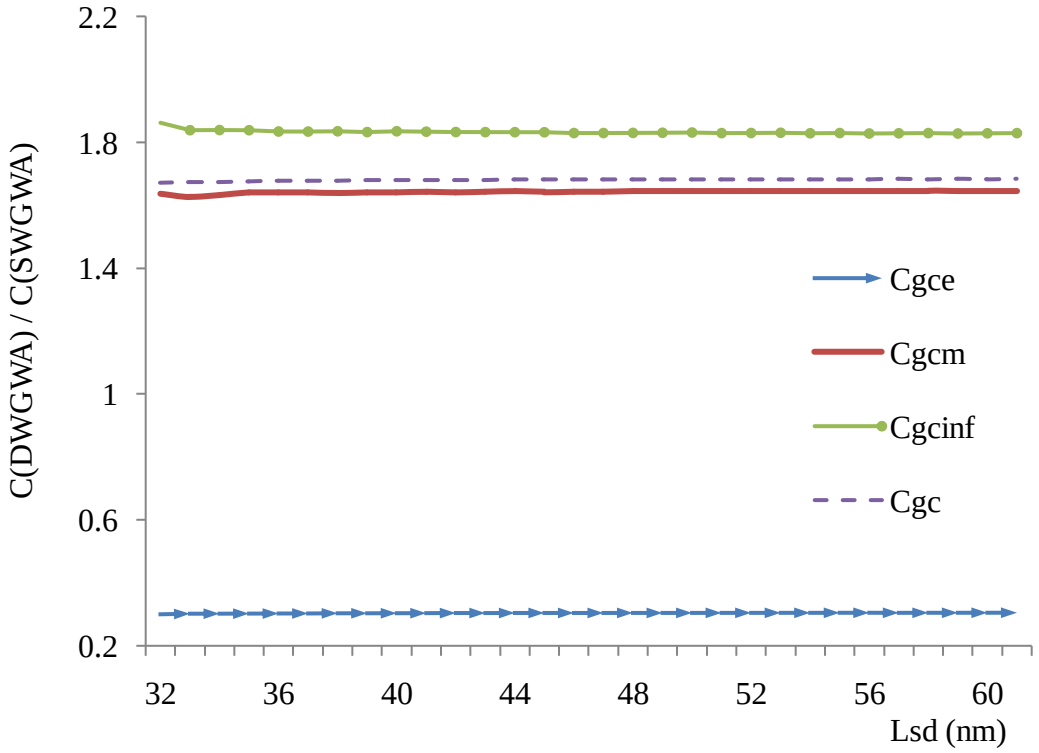

Figure 8: Capacitance ratio between DWGWA and SWGWA for varied source/drain lengths.

Similarly,Fig.8.comparesgate-to-channel capacitance of end and middle GWACNT,Gate-to-channel capacitance without any screeningeffects (Cgcinf) and Gate-to-channel capacitanceincluding all screening effects of GWACNT(Cgc) for varied source/drain lengths. In all the curves DWGWA capacitances increase linearly at a rate greater than SWGWA. The rate of increment of the capacitances is greater for DWGWA than its counterpart.Cgc, Cgcm, Cgcinf shows 1.68, 1.64 and 1.83 times greater value for DWGWA than SWGWA. But in case ofCgce, the value of SWGWA dominates with that of DWGWA.Intrinsic capacitance ratioof DWGWA is about 1.6 to 1.8 times larger than that of SWGWA. The corresponding values are plotted in A6, A7.

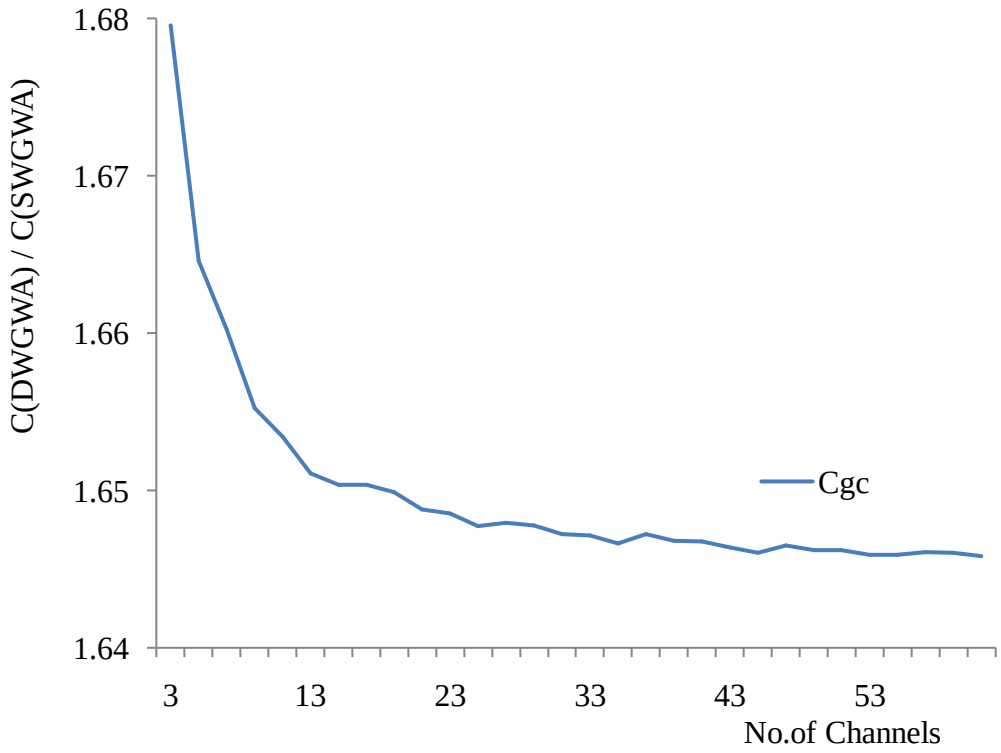

Figure 9: Capacitance ratio between DWGWA and SWGWA with respect to number of channels.

The number of channels plays an important role in determining the capacitance values of the device. Increasing the number of channels provides more gate capacitance as well as more parasitic capacitance with its fringing effects. Fig.9.dipicts the capacitance ratio ofgate-to-channel capacitance(Cgc)of GWACNT with respect to number of channels. The improvement of DWGWA 2.2fF over SWGWA(1.4fF) is being proved in the graph plotted in the fig A8. Capacitance ratio reaches 1.64 times fornumber of channelsgreater than 20 and maintains constant after N = 20 , reaching the limitation for the number of channels.

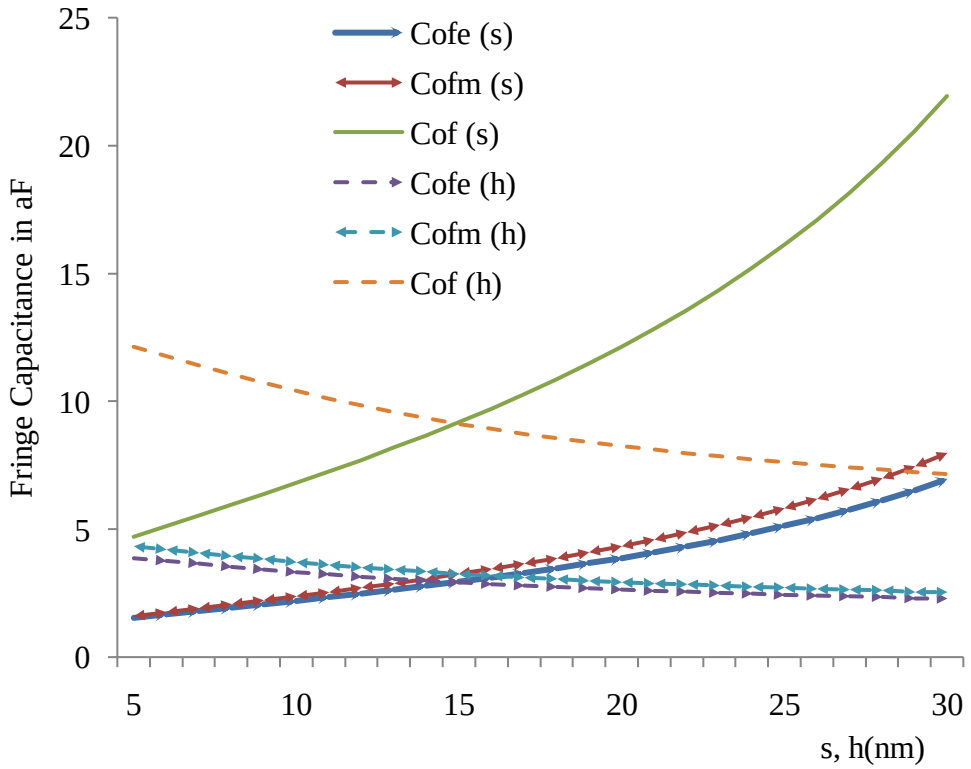

Figure 10: Variation offringe capacitances (end, middle and cumulative) of GWACNTwith change in ‘s’,’h’ distances.

Fringing capacitances are due to screening, imaging effects of neighbouring channels and theindividual walls of the channels. The values are to be studied to attribute thedevice performance. More the fringing effect, more will be the parasitic values in turnmore will be the reduction of total output capacitance values. Fig.10.projects the change of fringe capacitances (end, middle and cumulative) of GWACNT with respect to‘s’ and ‘h’ distances. Itis increasingwith ‘s’ and decreasing with ‘h’ distances.A trade off can be assumed while selecting the above two parameters.

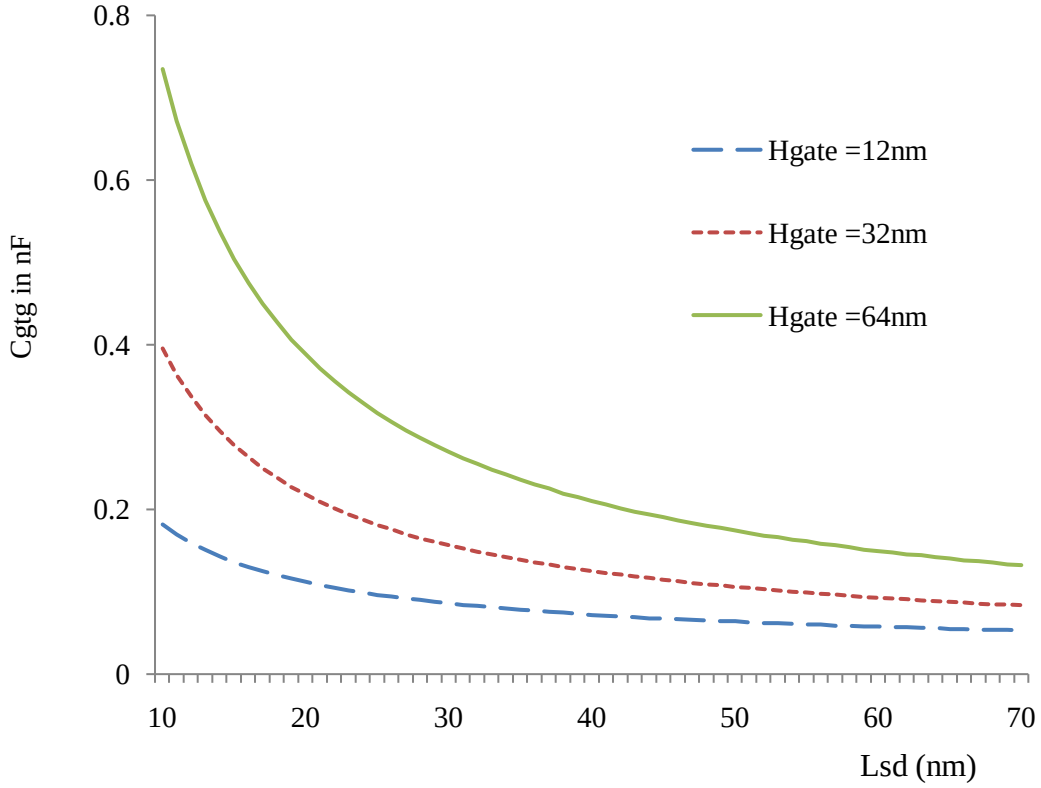

Figure 11: Variation ofgate-to-gate capacitance with respect to Lsd for GWCNT.

The summation ofboth Gate-to-gate fringe capacitance per unit length *Cgtg,fr*andGate-to-gate plate capacitance per unit length *Cgtg,nr is* plotted for studying the improvement of DWGWA over SWGWA and planar gate devices. Fig.11shows that variation of gate-to-gate capacitance with respect to LsdGWCNT. The values are in fF forSWGWA[9]and in pF forcylindrical channels[7]. The simulation environment may vary for the above reference model but it may not be larger. In our model, it is in nF which ensures that DWGWA provides an enhanced device.

Conclusion

DWGWA CNTFET is examined theoretically and it is found that it confirmshigherperformance in capacitance values compared to that of SWGWA CNTFET. Core capacitances aremodelled and analysed for the device. For a wide range of values of parameters like gate oxide dielectric(κ1), Source/Drain length(Lsd), the pitch distance(s) between the channels, normal distance between the gate and the channel(h) and number of channels(N)-the intrinsic, fringe, gate to gate anddrive capacitances of DWGWA CNTFET andSWGWA CNTFET are calculated. Channel density will not disturb the individual end and middle channel capacitances. It is

proved that the device with double-walled channels demonstrate its enhanced presentation by providing higher capacitance values with respectto the corresponding single wall channelled device. The variation is apparent for higher gate dielectric value (κ1), channel density(N), normal distance between the gate and the channel (h) andSource/Drain length(Lsd).The limitations are for larger values of's', distance. That is, the imaging effects can be reduced by increasing the pitch(s) distance. For the assumed values, the capacitance values of double-walled channel are at least 1.6 times and at most 2 times greater thanthat of single-wall. So, this work ensures a better device model which can be helpful for strengthening the future vision of next generation electron devices.

Annexure

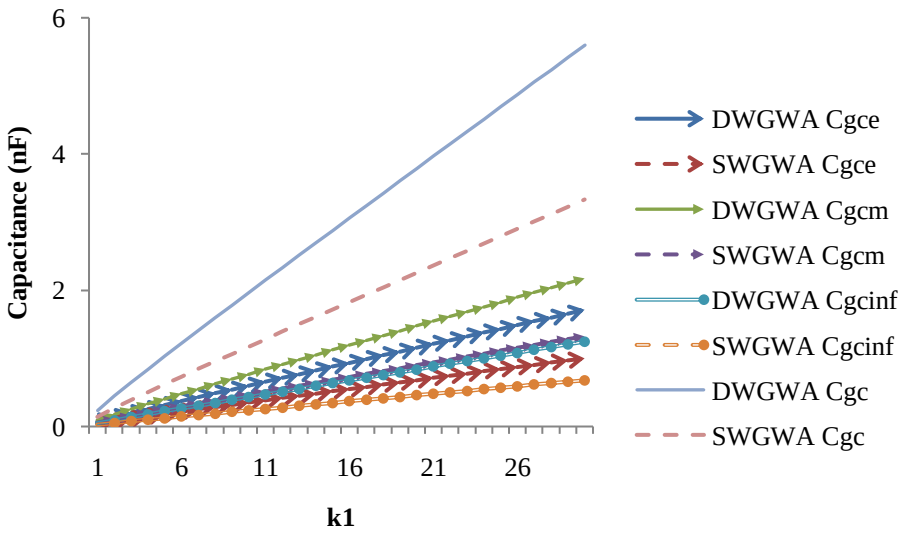

Figure A.1: Variations of capacitanceof DWGWA and SWGWA for different gate dielectrics.

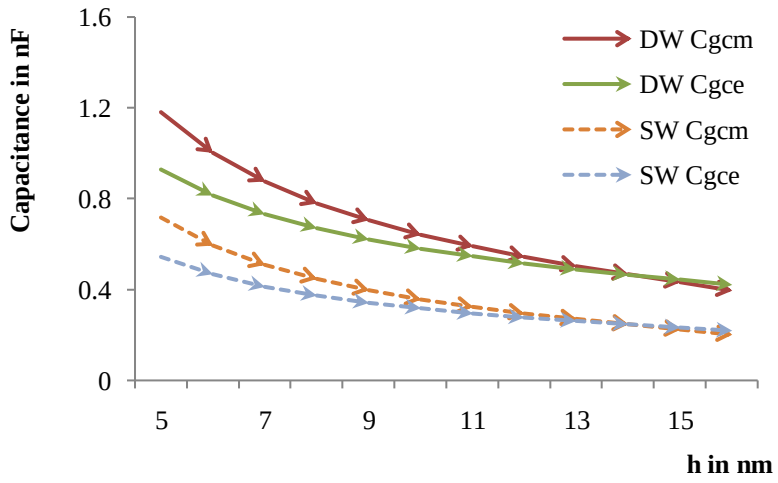

Figure A.2: Variation of Cgce,Cgcmof DWGWA and SWGWA for various h distances

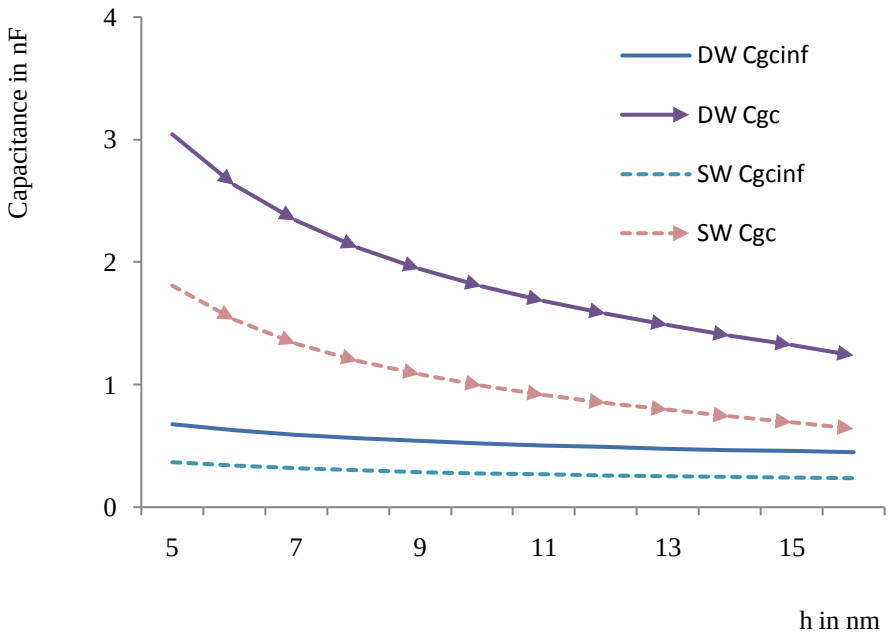

Figure A.3: Variation of Cginf, Cgcof DWGWA and SWGWA for various h distances.

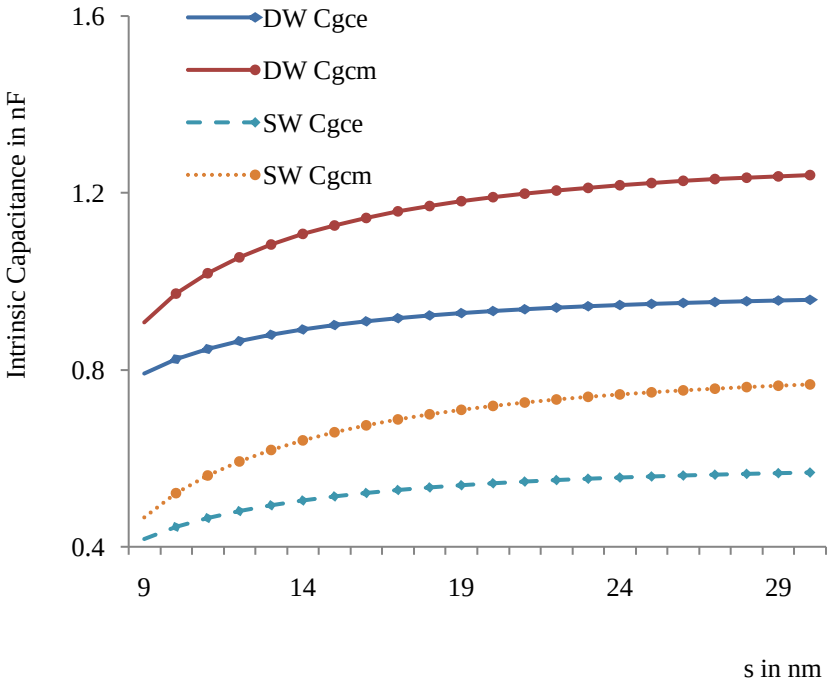

Figure A4: Variation of Cgce, Cgcm of DWGWA and SWGWA for different pitch distances.

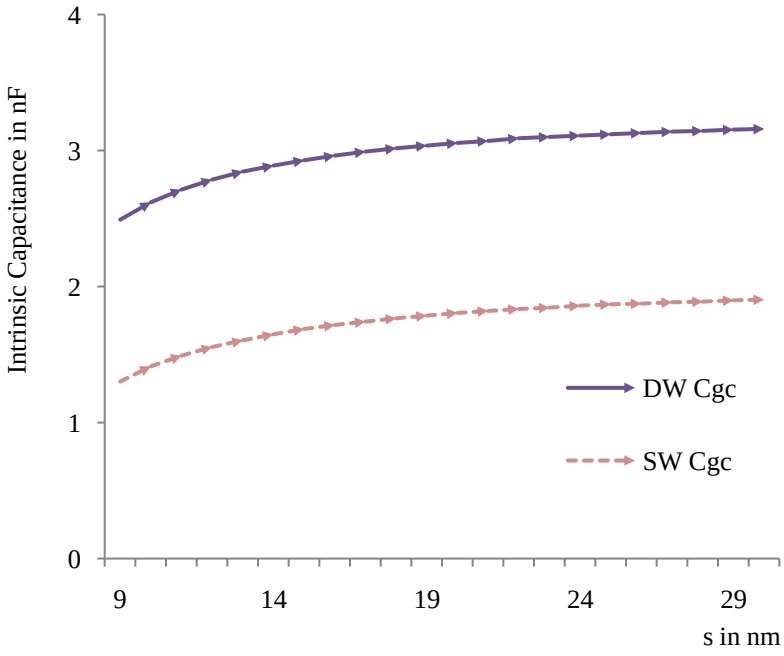

Figure A5: VariationofCgc of DWGWA and SWGWA for different pitch distances.

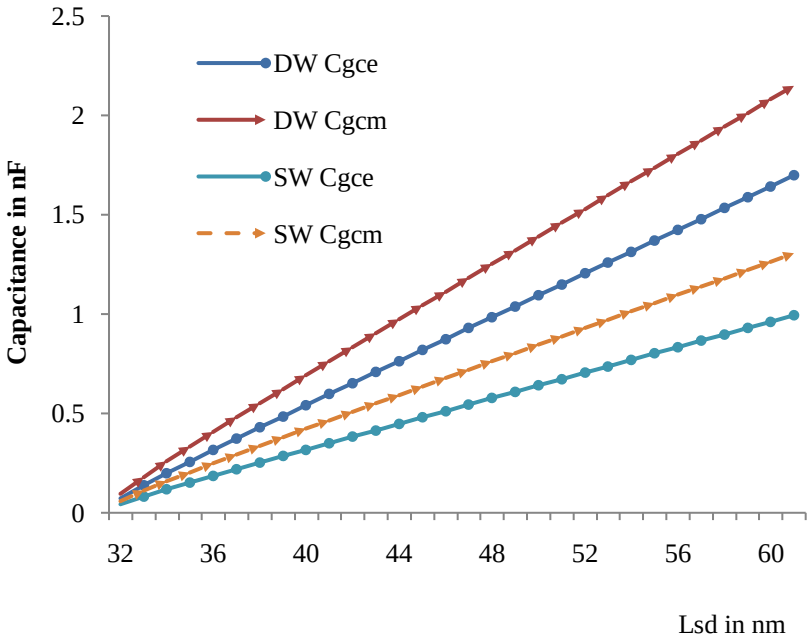

Figure A6: Variation of Cgce, Cgcm of DWGWA and SWGWA for varied source/drain lengths.

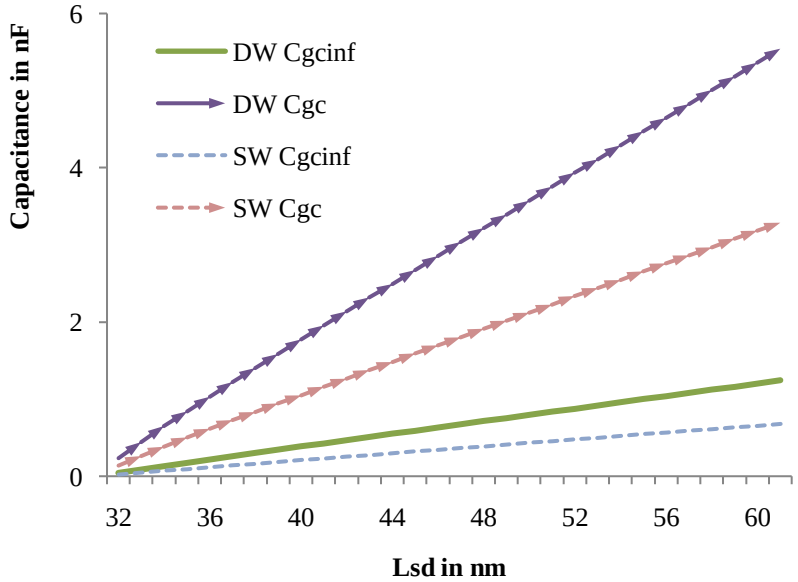

Figure A7: Variation of Cinf, Cgc of DWGWA and SWGWA for varied source/drain lengths.

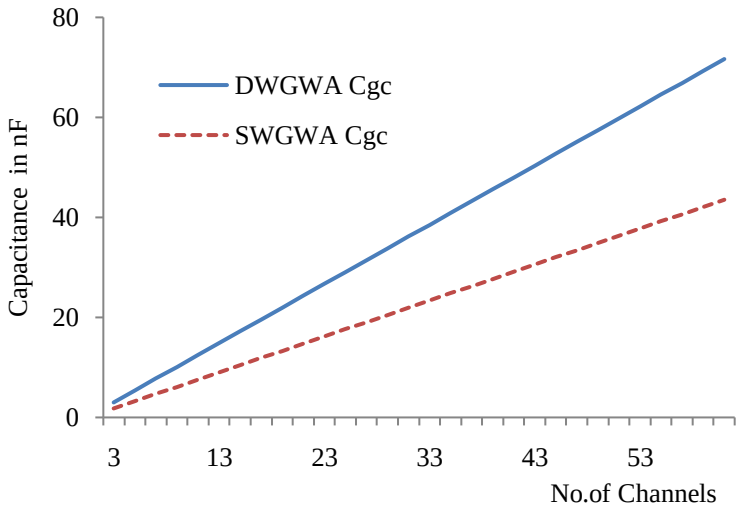

Figure A8: Variation of Cgc of DWGWA and SWGWA with respect to number of channels.

References

[1] E.Ramayya,D.Vasileska,S.M.Goodnick and I,Knezevic,"Electron transport in Si Nanowires",Journal ofPhysics Conference Series 38(2006),pp.126-129.

[2] AnisurRehman, Jin Guo,SuryaDatta and Mark Lundstrom"Theory of Ballistic Transistor", IEEETransactions on Electron Devices,50(9),2003,pp.1853-1864.

[3] Benjamin Iniguez, Antonio Lazaro,HamdyAbd EI Hamid,Oana Moldovan,BogdanNae, JaumeRoig,David Jimenez, "Charge based compact modelling of multiple gate MOSFET," *IEEE Custom Integrated Circuits Conference*, pp. 49-56.

[4] Bastin COUSIN, Lover ROZEAU, Marie-Anne JAUD, Jala JOMAAH, "Compact modelling of Quantizationeffects for cylindrical gate-all-around MOSFETs," 10th conference on IEEE2009, pp.269 – 272.

[5] TrondYtterdal, YuhuaChengandTor A. Fjeldly, MOSFET Device Physics and Operation in DeviceModelling for Analog and RF CMOS Circuit Design, E-Published : 10 JUN 2003 p.1-45.

[6] J.DengandH.-S.P.Wong,"Modeling andanalysisofplanar-gate electrostaticcapacitance of1-DFETwithmultiplecylindricalconducting channels,"*IEEETrans.Electron Devices*,vol.54,no.9,pp.2377–2385, Sep.2007.

[7] Jun Zh.Huang and Wen-Yan Yin,"Modeling and Performancecharacterization of Double-Walled Carbon Nanotube Array

Field-Effect Transistors", IEEE Transactions on Electron Devices, Vol.58, No.1 Jan 2011.

[8] Md.RakibulKarimAkanda and QuaziD.M.Khosru, "FEM Model of WraparoundCNTFET With Multi-CNT and Its Capacitance Modelling," *IEEETrans.Electron Devices*,vol.60, No.1,pp. 97–102,Jan.2013.

[9] JoergAppenzeller, " Carbon nanotubes for high-performance electronics-Progress and prospect," Invited paper, *Proceedings of IEEE*, vol.96, No. 2, pp.201-211, Feb. 2008.

[10] [Online].Available:http://www.nanohub.org