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High Step-up Single Switch DC-DC Converter with Resonance Soft Switching

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Abstract

In this paper, an isolated high step-up single switch dc-dc converter is proposed for photovoltaic source. In the proposed converter, high step-up voltage is obtained by single power switching technique that operates low duty cycle. It alleviates the conventional converters high duty ratio and high voltage stress on power devices. The presented converter recycles the leakage energy by using passive clamp which includes reverse recovery energy of the power diode and improves the efficiency. To achieve high output voltage gain, the isolated transformer primary and secondary terminals are connected in series during switching operation. The proposed scheme experimented with solar cell characteristic. PSIM software has been used for simulation. The operation is verified by simulation and validated by implementing in the hardware model at 40Vdc/400Vdc, 100kHz, 500Watts

Keywords-Single Switch; DC-DC Converter; Clamp Circuit; Photovoltaic; Solar cell.

1. Introduction

Photovoltaic (PV) is the direct transformation of solar energy into electricity. Solar energy become one of the main contributors in the future energy crises. The renewable energy has several advantages such as pollution-free power generation, low maintenance cost, low operation cost and supply limitations. PV systems helps further technology improvement and cost reduction along the value chain [2]. PV technology is not only to improve the efficiency of the cells but also of the modules and hence it make it more feasible for various applications [3]. PV electricity is one of the best options for sustainable future energy requirements of the world. The present PV

market is growing at the very high market [4]. In recent years, the high step up dc-dc converters have played a vital role in renewable energy applications. The boost converters are needed for increasing low dc voltage to high dc voltage. The conventional boost converters are not preferred, because with high voltage duty ratio, it causes severe losses in power devices and high voltage stress across the switching devices, which generate high conduction losses, thus resulting in the increase of complicity. To avoid these problems, the isolated high step-up single switch dc-dc converter with new single switching technique proposed [1] and improved version of this converter are analyzed in this paper. To reduce the stress on the active switch resonant boost converter for photovoltaic application is proposed [5]. Active switch method is adopted to increase the voltage gain and efficiency and a Z-source based topology that can boost the input voltage to desired level with low voltage stress [6]. The input current doubler and output voltage doubler are suitable for better performance in fuel cell power system [7]. The coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors [11].

The conventional boost converters are not able to provide high voltage gain [8]. High voltage gain with high efficiency can be achieved by the intergraded boost flyback converter system [9]. The investigation of high-efficiency clamped voltage dc-dc converter with reduced reverse-recovery current and switch-voltage stress and designed by way of the combination of inductor and transformer to increase the corresponding voltage gain [10]. The passive lossless clamp circuit is implemented instead of an active clamp circuit to recycle the leakage energy, also simpler and easier to design [12].

In this paper, an isolated high step-up single switch dc-dc converter is proposed and implemented. In the proposed, converter high step-up voltage is obtained by single power switching technique operating low duty cycle with isolated transformer inductors and switched capacitors and power diodes. The proposed converter eliminates the switching losses and recycles the leakage energy. The isolated transformer primary and secondary terminals are connected in series during switching operation. The output of the boost converter and isolated switched-capacitor cell are connected in series for high step-up with a low turn-on ratio which has already been discussed [12]. The proposed converter alleviates the conventional converters high duty ratio and high voltage stress on power devices. The proposed converter eliminates the switching losses by the method of series resonance soft switching. PSIM software has been used for simulation. Simulation circuit is analyzed at 40Vdc/400Vdc, 500Watts and this operation is validated by implementing in hardware model at 40Vdc/400Vdc, 500Watts with the switching frequency 100kHz.

2. Proposed Circuit Diagram

The block diagram of the proposed isolated high step-up converter with single power switch is shown in Fig.1. The block diagram shows the input PV model, high frequency isolated transformer, power capacitors and power diodes with single power

switch. The single power switch is controlled through the controller dSPACE. The output is connected with the resistive load model.

The passive lossless clamped circuit is proposed. The clamped capacitor (C_c) and clamp diode (D_c) connected across IGBT switch to reduce the voltage stress. The V_c is the clamped capacitor voltage. The clamp circuit recycles the energy stored in the leakage inductance. The voltage gain is obtained by significant value by providing a switched capacitor (C_{sc}) and secondary inductor L_s and switched diode (D_s). The switched capacitor voltage is given by V_{sc}. The output diode (D_o) current is I_o. The topology is modeled with an ideal transformer with corresponding turns ratio (n) equal to n_2/n_1. L_m is the magnetizing inductor L_k is the leakage inductance. I_{LK} is the leakage inductance current. V_d is the output diode stress. Hence, here the fast recovery diode used the capacitance effect of the depletion layer of the diodes neglected even reverse-recovery interval. The circuit is operated in six operating modes as explained below.

The key operating waveforms are sketched in Fig.2. V_{ce} and I_e are switch collector to emitter voltage and current. I_s-is the isolated transformer with secondary current. The clamp diode current is named as I_{dc} and clamp capacitor current named as I_c.

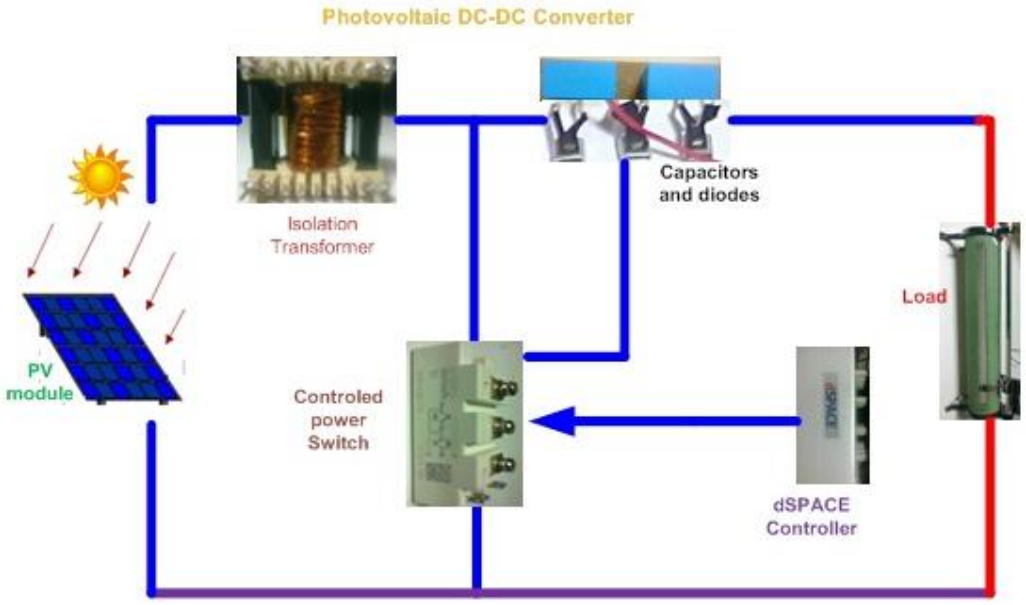

Fig.1 Block diagram of the proposed PV DC-DC Converter

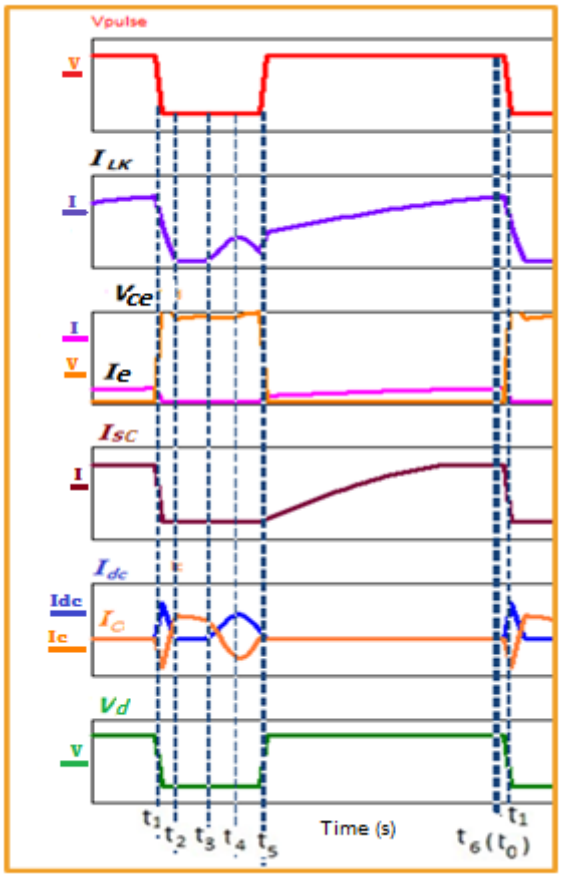

Fig.2. Proposed converter operating waveforms

3. Principle of operation

3.1 Mode I

The active switch(S) is turned ON state, the output diode D_o and clamp diode D_c are operating in reverse bias and turn OFF. The magnetizing inductor (L_m) is energized by switched capacitor (C_s) which energy is already stored in the previous cycle. The source (V_{in}) the magnetizing current i_{lk} linearly increases. L_s and L_p inductors are connected via clamp diode D_c. The current flow through the secondary winding is controlled by leakage inductor L_k and i_{lk} is given by,

$$\frac{V_{in}(t_1 - t_o)}{L_m + L_p} \approx i_c(t_1) - I_c(t_o) \approx i_{Lk}(t) \tag{1}$$

The voltage equation is given by

$$V_{in} = V_{LK}(t_o - t_1) + \frac{V_{CS}}{n} \tag{2}$$

3.2 Mode II

In mode-II (t_1-t_2). When switch is turned OFF at t_1. The input current as the two path via clamp diode (I_{dc}). Switching voltage is clamped to the capacitor voltage. L_k resonate with clamp diode current ($I_{c)}$ and clamped capacitor (C_c). So that the current through the leakage inductor i_{lk} linearly decreases through the secondary winding. L_k is discharged by the clamped capacitor voltage V_c.

$$\frac{V_C(t_1-t_2)}{L_k} - I_{Lk}(t_1) \approx i_{Lk}(t) \tag{3}$$

3.3 Mode III

During mode-III (t_2-t_3) the secondary winding current is down to zero, then the switched capacitor C_s employs throughout this period. The voltages of switched capacitor and clamped diode current stay simultaneous, then switched capacitor is resonate with leakage inductor, switched capacitance decreases, but at the same time leakage inductor current i_{lk} decreases. The secondary transformer current (I_s) is started raising. D_o and D_c carries the same current.

$$I_{Lk}(t_2) - \frac{V_o - V_c(t_3)}{L_k} \approx i_{Lk}(t) \tag{4}$$

3.4 Mode IV

Mode-IV (t_3-t_4), here, the switch is being turned OFF, the voltage across the switched capacitor is high and then the diode D_o is operated. The magnetizing inductor (L_m) releases the stored energy and sends its energy to load, and clamp diode discharge energy when secondary magnetizing energy weakens and the parasitic capacitance of all the diodes is thus neglected.

$$\frac{V_o - [V_{Sc} + V_c](t_3 - t_4)}{nL_m} + I_{Lm}(t_3) \approx i_{Lm}(t) \tag{5}$$

$$n = \frac{n_2}{n_1} = 1$$

$$\frac{[L_p + L_m](t_3 - t_4)}{nL_p} i_{Lm}(t_3) \approx i_{Lk}(t) \tag{6}$$

The voltage equation from t_1 to t_4 is given by

$$V_o = (V_c + V_{cs} + n) \times (V_c - V_{Lk(t_1 - t_4)} - V_{in}) \tag{7}$$

3.5 Mode V

In Mode-V (t_4-t_5) the switch leakage inductor (L_k) current falls to zero, the magnetizing inductor is discharged linearly. Secondary inductor passes energy to the load through the converter hence I_s decreases. Small charge in magnetizing current is equal to i_{Lm} as given below.

$$\frac{V_o - [V_{sc} + V_c](t_4 - t_5)}{nL_m} + I_{Lm}(t_4) \approx i_{Lm}(t) \tag{8}$$

The clamped diode discharges its energy, hence the clamped diode cathode potential is less than the anode and so the diode starts conduct and about resonate the single switch with clamped capacitor.

3.6 Mode VI

The switch is turned ON (t_5-t_6), the leakage inductance increases from zero, the switch is turned on by the ZVS condition V_{ce} completely zero, the leakage current is controlled by leakage inductor and the equations are given by

$$\frac{V_{in}+[V_o-V_{sc}(t_5)-V_c(t_5)]}{L_k}(t_5-t_6)\approx i_{Lk}(t) \tag{9}$$

4. Performance analysis

Analysis performed by considering clamped capacitor and switched capacitors are constant and current through the magnetizing inductor (L_m) also constant. When the switch is turned on, the L_m is charged by the input voltage is given by,

$$V_{lm}=V_{in} \tag{10}$$

Switched capacitor voltage (V_{sc}) can be given by

$$V_{sc}=n\times V_{in} \tag{11}$$

When switch is turned off the L_m is discharged and voltage is expressed by,

$$V_{Lm}=\frac{V_o}{n+1}-V_{in} \tag{12}$$

The voltage gain can be obtained from inductor volt-second balance principle

$$DV_{in}-\frac{V_o}{n+1}(1-D)+V_{in}(1-D)=0 \tag{13}$$

$$V_{GN}=\frac{V_o}{V_{in}}=\frac{n+1}{1-D} \tag{14}$$

$$V_o=\left(\frac{n+1}{1-D}\right)V_{in} \tag{15}$$

Also the Output voltage can be reanalyzed as follows,

$$DV_{in}-\frac{V_o}{n}(1-D)+\frac{V_c}{n}+\frac{V_{sc}}{n}+\frac{V_d}{n}=0 \tag{16}$$

$$\frac{nDV_{in}}{(1-D)}+\frac{V_c}{n}+\frac{V_{sc}}{n}+\frac{V_d}{n}=V_o \tag{17}$$

The voltage gain increases greatly when the turns ratio (n) increases. Extreme duty cycle can be designed to optimize the load regulation performance to the proposed isolated high boost dc-dc converter. n=0 is the conventional converter. The voltage gain of the proposed converter is increased greatly by using a proper turns ratio design. The voltage stress of the switch and clamp diode can be written as,

$$V_{stress}=\frac{V_{in}}{1-D} \tag{18}$$

In the circuit design the turn's ratio design plays an important role. By using this, the voltage stress (V_{stess}) of the switch is found out and duty ratio is obtained, it is given by

$$n = \left[\frac{(1-D) \times V_o}{V_{in}} \right] - 1 \tag{19}$$

The voltage gain of the converter is gained greatly by using a proper turn's ratio design. The output capacitors are used as filter and the aim is to reduce the ripples in the capacitors. The relationship between the output power and voltage ripple is given by

$$C = \frac{P_o}{V_o \times \Delta V_c \times f_s} \tag{20}$$

$$P_o = V_o \times \Delta V_C \times C \times f_s \tag{21}$$

In the above equation, ΔV_c is voltage ripple on the capacitor C_c or C_s. ΔV_c it assumed as 2%. The proposed dc-dc converter is defined as low loss converter. The efficiency of the converter is the ratio of the output power to the input power. The input power is the sum of the output power and the losses of the individual device.

$$P_{mos} = P_{sw(cond)} + P_{sw(off)} \tag{22}$$

$$P_i = P_o + P_{switch} + P_{diode} + P_{others} \tag{23}$$

Thus the efficiency expression is

$$\eta = \frac{P_o}{P_o + P_{switch} + P_{diode} + P_{others}} \tag{24}$$

4.1 Boundary Operating condition between CCM and DCM

Output Analysis by applying voltage-second balance to mutual inductance (L_m), relationship between the main duty cycle (D) and output diode's conduction time ratio is determined as

$$i_d(t) = i_c(t) + I_o \tag{25}$$

$$\langle i_d(t) \rangle = \langle i_c(t) \rangle + \frac{V}{R}$$

$$i_c(t) = 0 \tag{26}$$

$$\langle i_d(t) \rangle = \frac{1}{T} \int_0^{T_s} i_d(t).dt \tag{27}$$

$$\frac{V_{in} D_1 (1-D) T_s}{2L} - \frac{V}{R} = 0 \tag{28}$$

$$\frac{V_o}{R(1-D)} \le \frac{D V_{in} T_s}{2L} \tag{29}$$

Eqn.(17) is substituted in the eqn. (29). Then,

$$R \left[\frac{nD V_{in}}{D'^2} + \frac{V_c + V_{sc} + V_d}{nD'} \right] \le \frac{D T_s V_{in}}{2L} \tag{30}$$

$$\frac{2L}{RT_s} \le \left[\frac{D'^2}{n} + \frac{D D' V_{in}}{V_c + V_{sc} + V_d} \right] \tag{31}$$

Here $V_{in} \approx V_c \approx V_{sc} \approx 3V_d$

Then the eqn.(29) can be rearranged as

$$\frac{2L}{RT_s} \leq \left[\frac{nDD'}{2nD+5D'}\right]$$

$$\frac{2L}{RT_s} = K \tag{32}$$

Dimensionless conduction parameter

$$K_{critical} = \left[\frac{nDD'}{2nD+5D'}\right] \tag{33}$$

Fig.4. shows the DCM and CCM boundary with n=2 at rated full load and the rated input of the photovoltaic isolated dc-dc converter.

When $K < K_{critical}$ (34)

The converter falls discontinues conduction mode (DCM). The proposed converter is operated mainly in DCM covers more area as shown Fig.4, hence this converter in the DCM at operating full load duty cycle at 70%. It has some salient features like low turn ON loss, soft recovery and low circuit inductance.

And when $K > K_{critical}$ (35)

The converter current conducts in continuous mode.

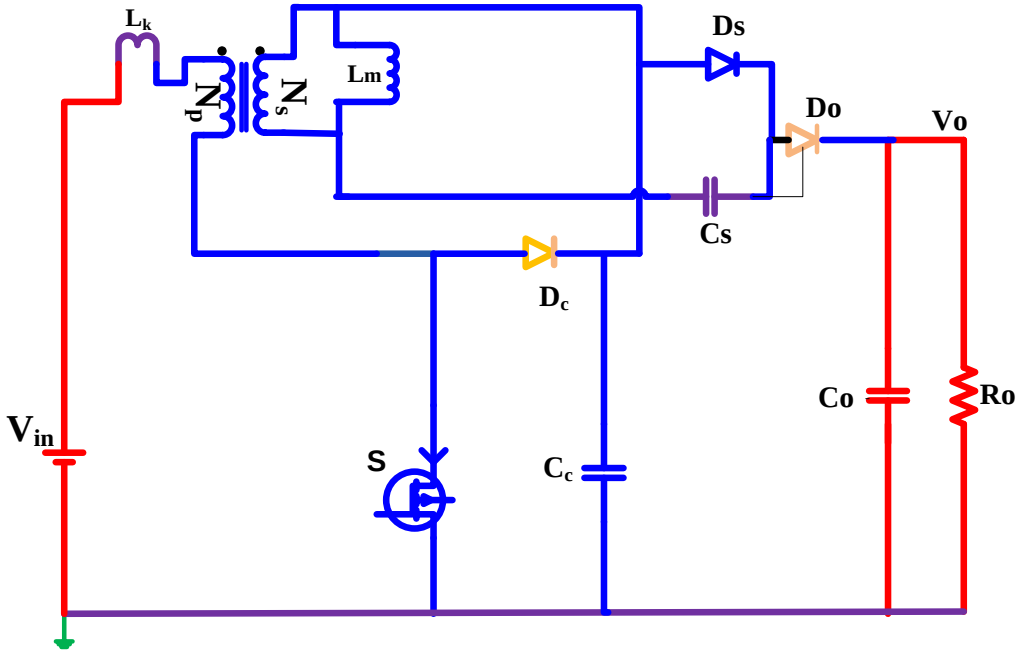

Fig.3. Proposed converter operation circuit

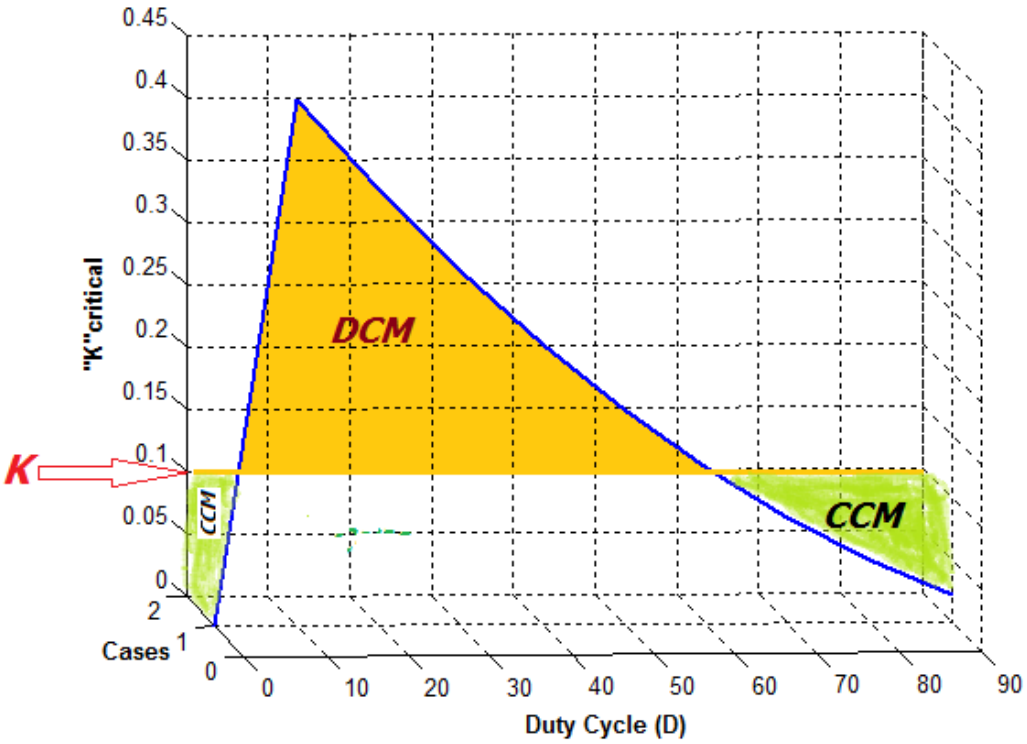

Fig.4. DCM and CCM boundary operation with n=2

5. Results

5.1 Simulation results

The proposed high boost dc-dc converter is simulated using PSIM software and output voltage and output gain are described before implementing. The switching frequency, input voltage 100kHz, 40V_{dc} are respectively used for simulation. Step-up output voltage obtains 403V_{dc}. The voltage gain (V_{GN}) is equal to 10. This is matched with the theoretical value given in eqn.(15) & eqn.(17). Full load rating 500Watts is used in the simulation. At rated input current, the gate pulse (S), output voltage (V_o), output current (I_o) are shown in the Fig.5. The output currents of power diodes D_o, D_r, and D_c are shown in Fig.6. during the switching operation. The Fig.7. shows the clamp capacitor wave during the series resonance with transformer inductance and diode forward current as operation given during mode-V. The output voltage is lifted up to 403V. Hence, it is realized with the theoretical output voltage (V_o) given in the eqn.(15) & eqn.(17).

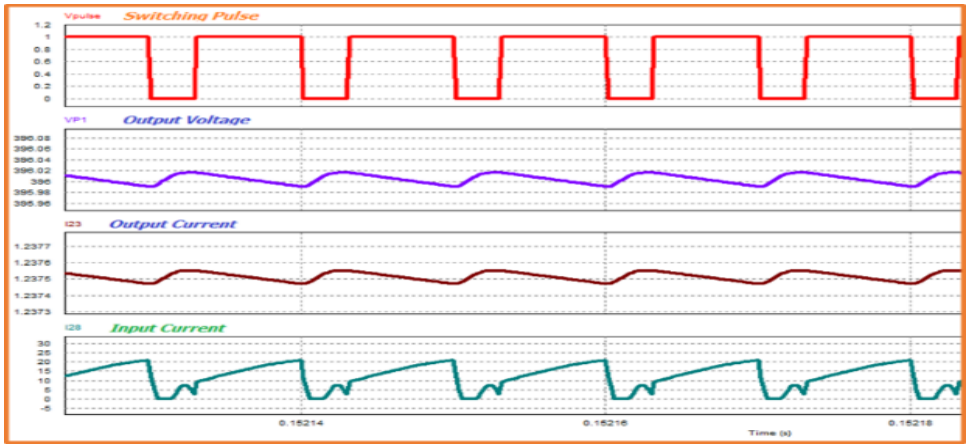

Fig.5. Waveforms of the proposed converter at rated input voltage (40V)

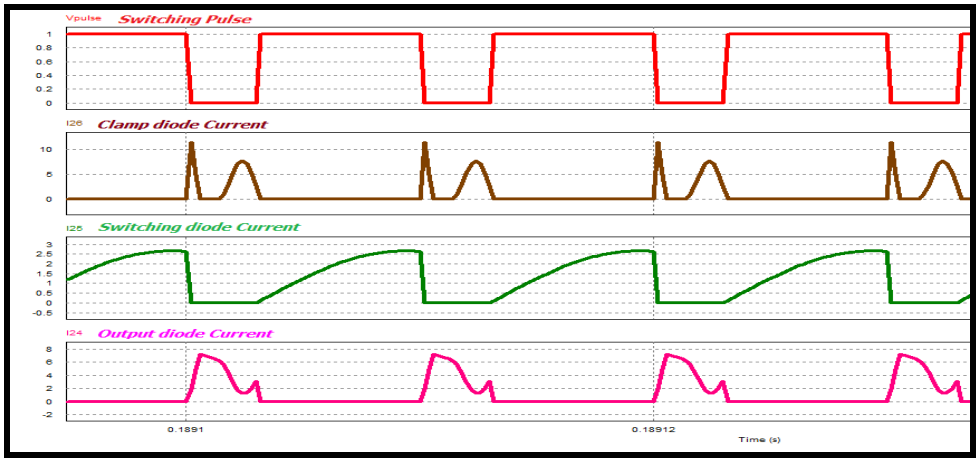

Fig.6. Diode currents during switching operations

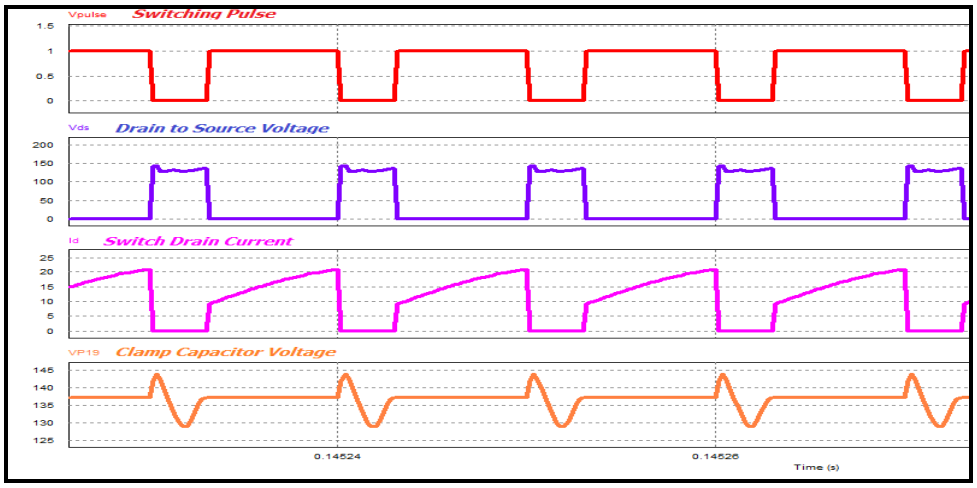

Fig.7. Switch voltage, Current and Clamp capacitor voltage

5.2 Soft Switching

In Fig.8. shows the voltage between collector to emitter of the IGBT power switch and current through the switch reaches zero before the gate pulse (S) is applied to controlled switch. Then the voltage starts increasing through the switch. This ensures ZVS of the switch. ZVS does not affect the switching loss that arises from the power switch output capacitance and it may not influence the loss induced by diode reverse recovery, hence ZVS is of no help in improving of converter efficiency. The practically measured switch stress (V_{CE}) and current (I_e) is shown in Fig.9. This ensures ZVS of the switch which is depicted in the arrow point in the Fig.9. The measured maximum switch voltage is equal 130V. The main switch voltage is clamped to that of the clamp capacitor by the clamp diode, when the switch is turned off at series resonance with isolated transformer inductance. The resonance frequency is greater than the switching frequency. From the waveforms in the Fig.9. it can be seen that ZVS turn on condition is achieved for the active switch, which reduces the switching losses.

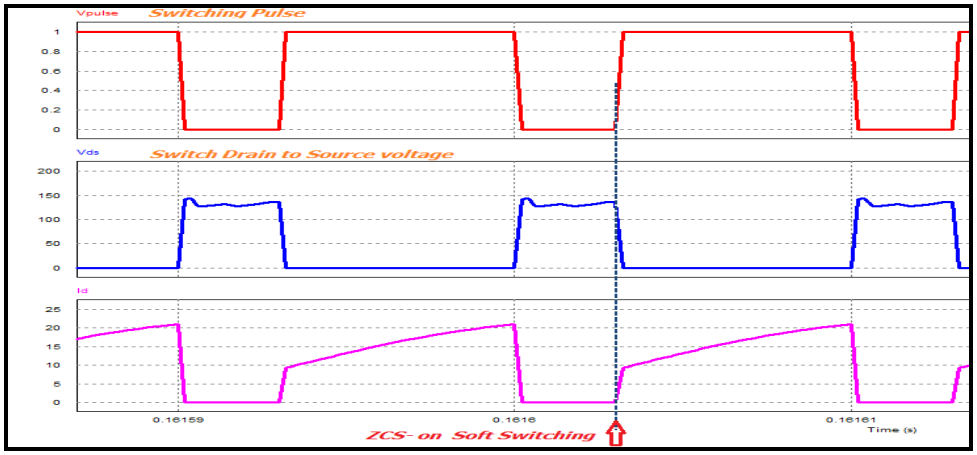

Fig.8. Switch voltage V_{CE} and Switch Current (I_e) (ZVS)

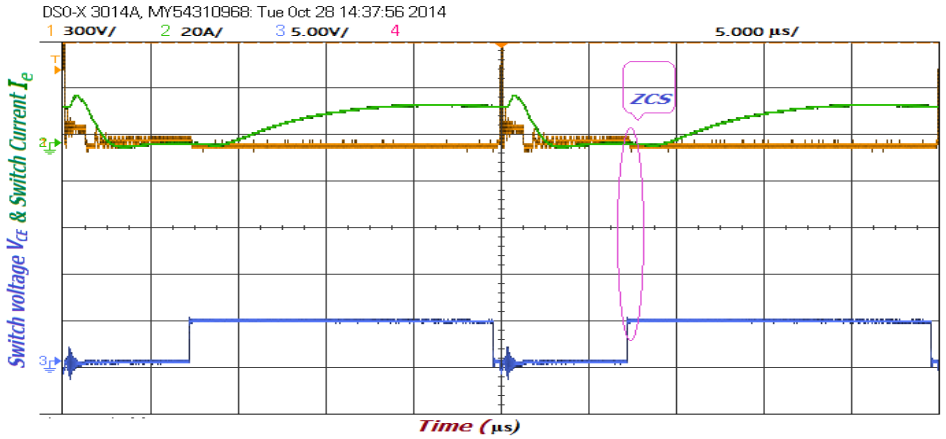

Fig.9. Soft switching (ZVS) Switch Voltage and Current

5.3 Experimental Results

A 500W prototype of the proposed converter is built to verify the theory. The hardware prototype model is shown in Fig.13. The hardware prototype is validated with simulated design. The proposed model is 500Watts with 40Volts at 100kHz switching operation. The measured clamp diode (D_c) and the switched diode (D_s) current with switching pulse are illustrated in Fig.10. The input to the prototype model is given $40V_{dc}$ from the available DC power supply source. (Chroma-62012P-80-60) and the controlled single switch is controlled through DSP (TMS320F28335) controller. The hardware and simulation parameters are shown in Table 1.

The fixed DC source validated to renewable source by considering single solar cell measurement. the I-V and P-V curves are plotted as shown in the Fig.11. For study 57mm diameter silicon solar cell under 1 Sun (1000 W/m^2) at 33˚C the voltage and current are measured. From this available experimental data, MPP is roughly estimated.

The solar cell open circuit, short circuit and maximum power point data are V_{oc}=0.5727V, I_{sc}=0.7605A, I_{mp}=0.6755A and V_{mp}=0.4590V. MPP is pointed between two steady operating points. These operating points the voltages are 0.415V and 0.475V. These values are per solar cell. For the practical case from the 40V DC source the load operating points are validated with different input voltages. These voltages are based on percentage variation in the single solar cell. The calculated variable voltage ranges are 42.1 40V, and 44.2V at full load, half load and no load respectively. The output waveform is observed by using Mixed Signal Oscilloscope and measured. The measured input and output voltages are at various operating voltages with different load conditions.

The switching pulse duty cycle (D) ranges vary accordingly from 70% to 65% during full load to no load. The experimental results show that the output voltage can be boosted upto the voltage gain 10 when it turns ratio (n) equal to 1:2. Thus, the proposed boost converter is capable to interface to the inverter grid at the user end. The experimental results are tabulated in Table 2.

The efficiency of the hardware model system is calculated at 4 different loads. By using the measured output power, the efficiency of the proposed dc-dc converter curve plotted with conventional converter efficiency are shown in Fig.12. The theoretical efficiency equation is given in eqn.(24). The practical calculated efficiency of the proposed model at full load is 96.5%.

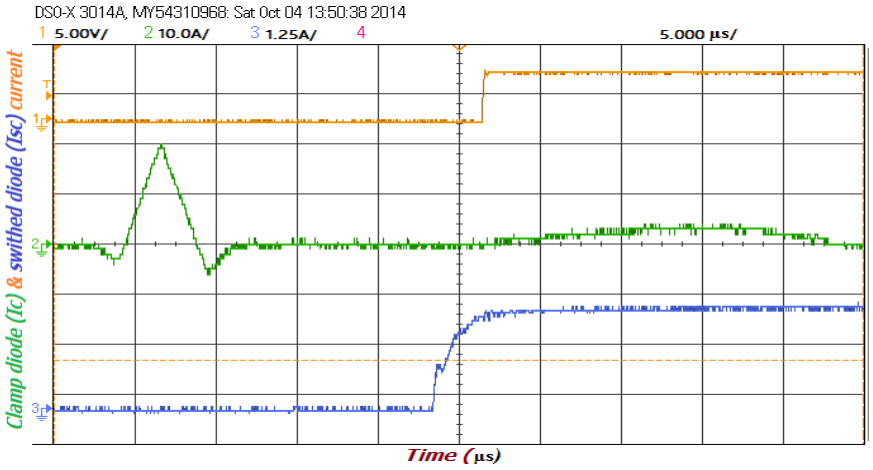

Fig.10. Clamp diode & Switched diode measured current

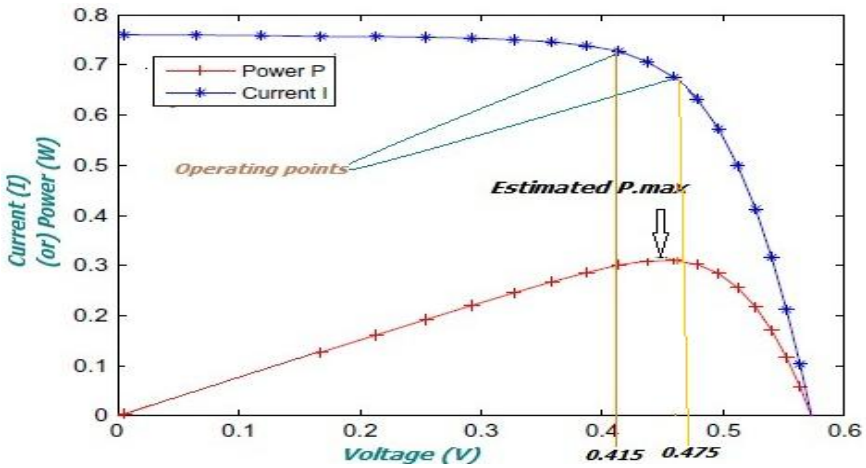

Fig.11. Solar cell I-V and P-V curve

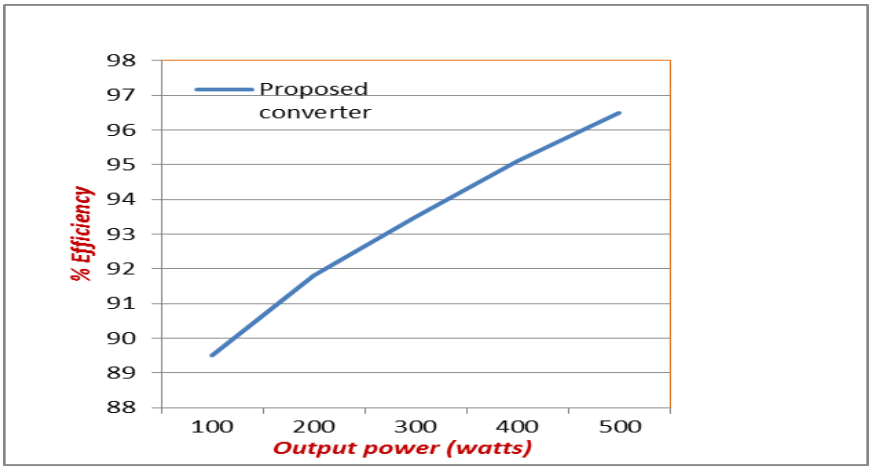

Fig.12. Percentage Efficiency Vs Output power (Watts)

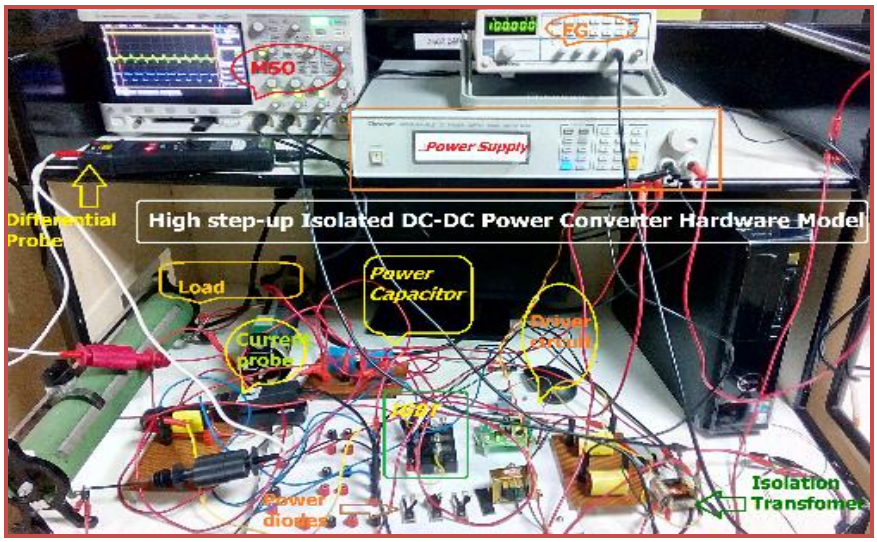

Fig.13. Hard ware model: Proposed isolated DC-DC Converter

Table 1. Hardware and Simulation parameters

Parameters	Specifications Simulation	Specifications Hardware
Input voltage	40V	40V
Output voltage	400V	400V
IGBT	Ideal	CM100DU12H
Diode	Ideal	BY329X
Capacitors	C_c=563F C_{sc}=41.66uF C_o=330uF	C_c=0.5uF C_{sc}=40uF C_o= 330uF
Isolation transformer	Turns ratio= 1:2 L_m =160 Uh L_k=0.3uH	Turns ratio=1: 2 L_m = 163uH L_k=0.231uH
Load	500W	500W
Driver IC		FOD3180

Table 2. Experimental Specifications

S.No.	Parameters	Specification
1	DC voltage input	40V-45V
2	DC voltage output	400V
3	Output power (max)	500 W
4	Switching Frequency	100 kHz
5	Output current	1.26 A
6	Output Voltage ripple	2V ±5 %
7	Output Current ripple	0.4mA

6. Conclusion

This isolated high boost converter with switched capacitor and magnetizing inductor are used to get the high voltage gain. The transformer isolation can be accomplished and it provides better significant influence on efficiency of whole energy condition PV system. An application of fast recovery diodes eliminates the reverse recovery problems. Thus it allows quick diode turn-off without significant power losses. The leakage inductor of the clamp circuit and the series resonance achieve ZVS condition. High boost voltage operation can reduce stress on active switch. The passive lossless clamp circuit helps to recover the leakage energy of the diode and clamped capacitor to get high efficiency at high power value. All these features improve the circuit efficiency effectively. Hence, the application of this high step-up dc-dc converter in the PV system can improve along with the power system value chain.

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