Custom Digital Design of High Speed 8 Bit Multiplier Using Cadence Tool

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Abstract

Many digital systems, comprising computers, necessitate implementation of integer and/or floating point multiplication and division. Further, numerous of these applications expect that multiplication and division for operands of significant size be performed at very high speeds. Historically, the recursive algorithms for these two operations if implemented in a direct fashion as sequential circuits with maximum hardware reprocess have very specific performance. Our objectives here are to exhibit these recursive algorithms for integer multiplication and division, put in two fundamental techniques to improved performance, and to provide an implementation of each algorithm that executes at high speed. This is the necessities document for implementation of a custom digital design of high speed 8 bit multiplier using cadence tool.

Keywords: Multiplier; cadence tool; high speed; wallace tree applications.

1. Introduction

A multiplier is one of the important hardware blocks in majority of digital and top execution systems such as digital signal processors, FIR filters and microprocessors, etc. with improvements in technology, numerous research workers have attempted and are working to design multipliers which propose either of the these- low power consumption, high speed, regularity of layout and hence little domain or even
assemblage of them in multiplier. Thus causing them fit for several low power, high speed, and impacted VLSI executions.

However speed and area are two inconsistent constraints. So ameliorating speed ensues perpetually in vaster areas. So here we attempt to determine the optimum trade off result among the both of them. Usually as we know multiplication comes in two fundamental steps partial product and then addition. Thus in this research work it is attempted to design distinct adders and equate their speed and complexity of circuit i.e. the area in use and then designed multipliers and have equated the speed in them.

While equating the adders it is determined that Ripple Carry Adder had a littler area while having lesser speed, in counterpoint to which Carry Select Adders are high speed but have a vaster area and a Carry Look Ahead Adder is in amongst the spectrum having an appropriate trade-off amongst time and area complexities. After designing and equating the adders we moved to multipliers. Ab initio Parallel Multiplier is examined and so Wallace Tree Multiplier. Meanwhile it is assessed that delay amount was substantially diminished when Carry Save Adders were used in Wallace Tree applications and examined the execution of all the multipliers.

The result of this explore helps to make an appropriate selection of distinct multipliers in constructing in distinct arithmetic units as well as creating a selection among distinct adders in distinct digital applications allowing to requirements. Further work on Low Power Techniques on different multipliers requires to be done in order to make us choose an appropriate multiplier in accordance with the necessities by making the closest achievable trade-off choice amongst Speed and Power in distinct conditions.

2. Tools and Requirements
A schematic design of the proposed high speed multiplier in 180 nm technology will be completed using cadence virtuoso schematic editor. The design will then be thoroughly verified applying the cadence spectre circuit simulator. The asserted design will then undergo layout design using the cadence virtuoso layout editor tool suite. The cadence assura tools will be utilized for physical confirmation like DRC, LVS and extraction. At last the extracted simulation will be operating to realize the functioning of the proposed high speed 8 bit multiplier with parasitic.

3. High-Performance Multipliers
The speed of multiple operation is of big significance in digital signal processing too as in the ordinary processors nowadays, particularly since the media processing took off. Formally multiplication was commonly applied via a series of addition, subtraction, and shift operations.

3.1 Binary Multiplier
A Binary multiplier is an electronic hardware device utilized in digital electronics or a computer or some other electronic device to execute rapid multiplication of two counts
in binary display. It is constructed utilizing binary adders. The principles for binary multiplication can be expressed as follows:

- If the multiplier digit is a 1, the multiplicand is merely copied down and represents the product.
- If the multiplier digit is a 0, the product is also 0.

3.2 Wallace Tree Multiplier
A rapid procedure for multiplication of two numbers was developed by Wallace. Utilizing this technique, a three step process is accustomed multiply two numbers; the bit products are constituted, the bit product matrix is minimized to a two row matrix where sum of the row equalizes the sum of bit products, and the two ensuing rows are added up with a fast adder to expose a product.

3.3 Vedic Multiplier
The use of Vedic mathematics lies in the reality that it dilutes the typical calculations in conventional mathematics to extremely easy ones. This is so because the Vedic formulae are claimed to be established on the normal rules on which the human intellect functions.

4. Schematics
4.1 Schematic of 8-bit Multiplier
After depict the schematic, it is determined that circuit is functioning in properly or not so, employing test bench assumption the period and pulse width, voltages to all input and related see the output after simulation. So the consequence in simulation window is demonstrated.
5. Testbench and Simulation

5.1 Layout of 8-bit Multiplier

Figure 3: (a), (b) and (c) The layout of 8 bit multiplier
5.2 Parasitic extraction of 8 bit multiplier

![Image](image1.png)

**Figure 4:** Parasitic extraction of 8 bit multiplier.

6. Conclusions
This paper gives a clear concept of distinct multiplier and their execution. It is determined that the parallel multipliers are greater choice than the serial multiplier. It is resolved from the result of power consumption and the total area. In event of parallel multipliers, the whole area is much less than that of serial multipliers. Hence the power consumption is also little. This speeds up the computation and constitutes the system quicker.

Multipliers are one the most distinguished component of many systems. So it is always needed to find an improved solution in case of multipliers. Our multipliers should constantly consume less power and cover less power. So through this research it is attempted to find out which of the three algorithms functions the ample..

It can be stated that Wallace Tree Multiplier is excellent in all respect like speed, delay, area, complexity, power consumption. However Array Multiplier demands more power consumption and affords optimum number of components demanded, but delay for this multiplier is greater than Wallace Tree Multiplier. Ancient Indian Vedic Mathematics devotes efficient algorithms or formulae for multiplication which enhance the speed of devices.

References


[9] Principles of CMOS VLSI design A system perspective, NEIL H. E. WESTE, KAMRAN ESHRAGHIAN