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Design Switched Capacitor Filter Sub Circuit Using Tanner EDA Tool

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Abstract

Switched Capacitor circuits are Pervasive in highly integrated, mixed signal Applications. Switched capacitor circuits fill a Critical role in analog/digital interfaces particularly highly integrated applications. This Chapter describes the basic building blocks that Comprise switched Capacitor circuits. These Blocks are the sample-and-hold (S/H), gain Stage. From these elements more complex Circuits can be built such as filters, analog-to- Digital converters (ADC) and digital-to-analog Converters (DAC). All sampled-data circuits, Such as these, require a pre-conditioning, Continuous-time; anti-alias filters to avoid Aliasing distortion.

1. Sample-and-hold (S/H)

The sample-and-hold is the most basic and ubiquitous switched-capacitor building block. Before a signal is processed by a discrete-time system, it must be sampled and stored. This often greatly relaxes the bandwidth requirements of following circuitry which now can work with a DC voltage. Because the S/H is often the first block in the signal processing chain, the accuracy and speed of entire application cannot exceed that of the S/H.

1.1 Top-plate S/H

In CMOS technology, the simplest S/H consists of a MOS switch and a capacitor as shown in figure 1.1. When Vg is high the NMOS transistor acts like a linear resistor, allowing the output Vo to track the input signal Vi. When Vg transitions low, the transistor cuts off isolating the input from the output, and the signal is held on the capacitor at Vo.

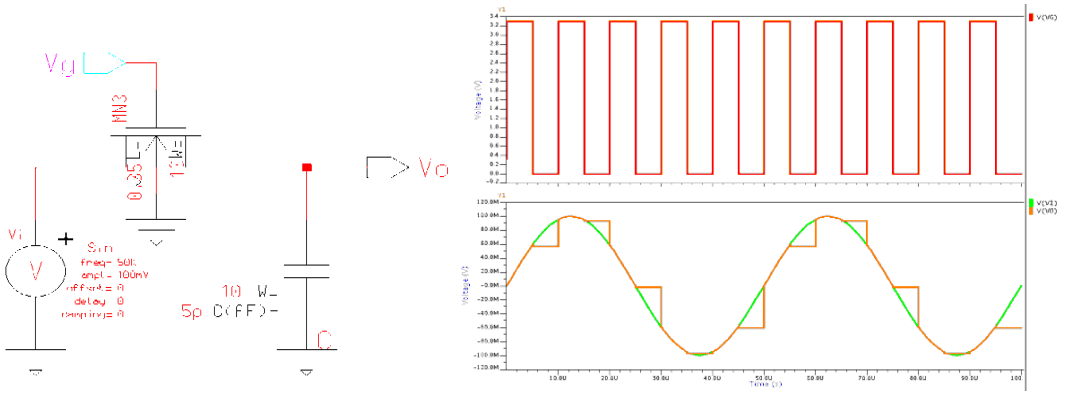

Figure 1.1: MOS sample-and-hold circuit.

There are several practical limitations to this circuit. Because the RC network has finite bandwidth, the output cannot instantaneously track the input when the switch is enabled. Therefore, a short acquisition period must be allocated for this (exponentially decaying) step response. After the S/H has acquired the signal, there will be a tracking error due to the non-zero phase lag and attenuation of the sampling network. The latter linear, low-pass filtering does not introduce distortion and is usually benign for most applications. The on-conductance, however, of the transistor is signal dependent:

$$I_D = u\ Cox\ W/L\ (Vg - Vi - Vt) \qquad (1.1)$$

Thus the transfer function from input to output can become significantly nonlinear if (Vg - Vi - Vt) is not sufficiently large.

When the switch turns off, clock feed-through and charge injection introduces error in the output. When the gate signal Vg transitions from high to low, this step AC couples to the output Vo via parasitic capacitances, such as Cgs and Cgd. Because the output is a high impedance node, there is no way to restore the DC level. This coupling is called clock feed-through. This error is usually not a performance limitation because it is signal-independent and therefore only introduces an offset and not distortion. To first order this error can be eliminated using a differential configuration. Charge injection, however, is a signal-dependent error.

When switch is turned off quickly, the charge in the channel of the transistor is forced into the drain and source, resulting in an error voltage. The charge in the channel is approximately given by equation 1.2 because q is signal dependent; it represents a gain error in the S/H output. There have been several efforts do accurately characterize this error.

$$q = WL\ Cox\ (Vg - Vi - Vt) \quad (1.2)$$

This circuit is also sensitive to parasitic capacitance. Any parasitic capacitance at the output change the amount of signal charge sampled, which is often the critical

quantity in switched-capacitor circuits. Bottom-plate sampling can greatly reduce these errors.

1.2 Gain stage

Figure 1.2 shows a gain stage that samples the input, applies gain, and holds the output value. A single-ended version is shown for simplicity, but the following analysis applies to a differential version which is most commonly used in practice.

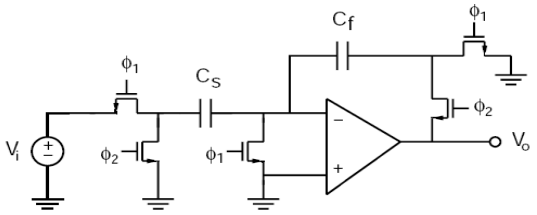

Fig. 1.2: Single ended gain stage

To better understand the operation of this circuit, figures 1.3(a) and 1.3(b) show the states of the switches during phase 1 and phase 2 respectively. During phase 1 (figure 1.3a), the input Vi is sampled across Cs. The op-amp is not used during this phase, and this time can be used to perform auxiliary tasks such as resetting common-mode feedback

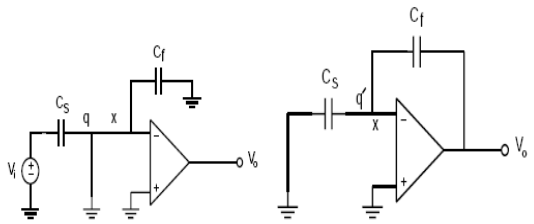

Figure 1.3 (a): Phase 1 Figure 1.3(b): Phase 2

The charge q is:

$$q = Cs\ (0 - Vi) = -Cs\ Vi \qquad (1.3)$$

Notice there is no charge stored on Cf since both sides are grounded. Bottom plate sampling is employed, and the sampling instant is defined by Φ' as before. During phase 2 (figure 1.3b), the op-amp is put in a negative feedback configuration, forcing node x to zero (virtual ground). Because the input is also ground, there is no charge storage on Cs, and all the charge is transferred to Cf. Thus, a voltage gain of Cs/Cf is achieved. Analytically, charge on node x is conserved,

o q = q'

q = q' (1.4)

Cs Vi = Cf(0 - Vo) (1.5)

— — (1.6)

If we consider the input Vi as a discrete-time sequence Vi (n) = Vi (nT), where T is the sampling period, then the output is

——— (1.7)

This equation reflects the one period latency of this discrete-time circuit.

1.3 Non-overlapping clock

Non overlapping clocks are essential in switched capacitor circuits. These clocks determine when the charge transfers occur and they must be non-overlapping in order to guarantee charge is not inadvertently lost. As shown in fig 1.4(a), the term non-overlapping clocks refers to two logic signals running at the same frequency and arranged in such a way that at no time are both signals high.

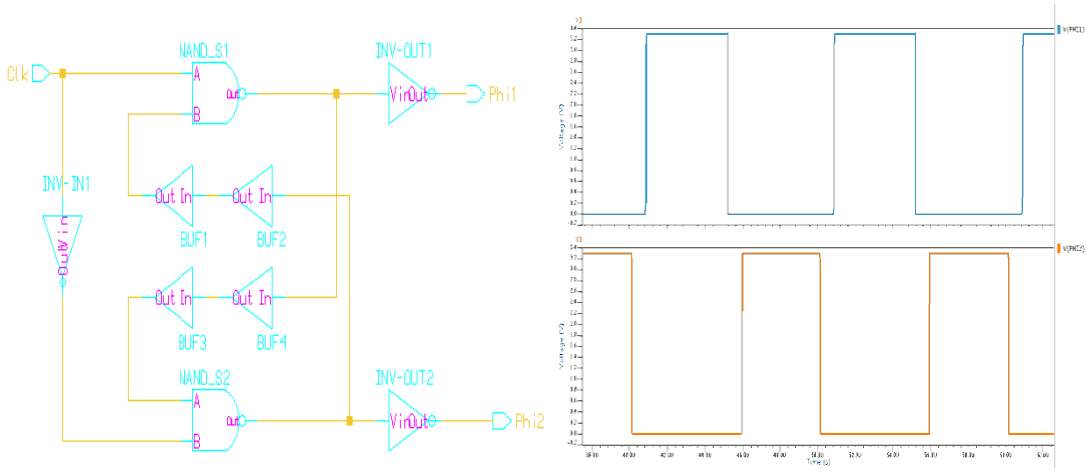

Fig. 1.4: (a) Circuit of nonoverlapping clocks. **Fig 1.4 (b)**: Clock signal Φ1 and Φ2.

The time axis in fig 1.4(a) has been normalized with respect to clock period, T. Such normalization illustrates the location of the sample numbers of the discrete-time signals that occur in switched capacitor filters. As a convention, we denote the

sampling numbers to be integer values, just before the end of clock phase 1, while the end of clock phase 2 is deemed to be ½ samples off the integer values as shown in fig. 1.4(b). However, it should be noted that it is not important that the falling clock edge of Φ2 occur precisely one half a clock period earlier than the falling edge of Φ1. In general, the location of the clock edges of Φ1 and Φ2 need only be moderately controlled to allow for complete charge settling. One simple method for generating non-overlapping clocks is shown in fig 3.4(a).Here, delay blocks are used to ensure that the clocks remain non-overlapping.

1.4 Resistor Emulation of Switched Capacitor

The essence of the switched-capacitor is the use of capacitors and analog switches to perform the same function as a resistor. Why one would want to replace the resistor with such an apparently complex assembly of parts as switches and capacitors. The switched-capacitor is area intensive and the use of the switched-capacitor will be seen to give frequency tunability to active filters.

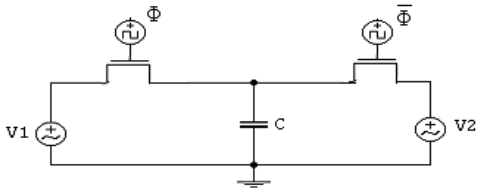

Fig 1.5: Two NMOS's, driven by alternating, non-overlapping clock.

Figure 1.5 shows the basic setup for a switched-capacitor, including two N-channel Metal-Oxide Semiconductor Field-Effect Transistors (NMOS) and a capacitor. There are two clock phases, Φ and Φ', which are non-overlapping. The MOSFET's, either M1 or M2, will be turned ON when the gate voltage is high, and the equivalent resistance of the channel in that case will be low, RON → 1 KΩ → 10 KΩ. Conversely, when the gate voltage goes LOW, the channel resistance will look like ROFF ≈ 1012Ω.With such a high ratio of OFF to ON resistances, each MOSFET can be taken for a switch. Furthermore, when the two MOSFET's are driven by non-overlapping clock signals, then M1 and M2 will conduct during alternate half-cycles.

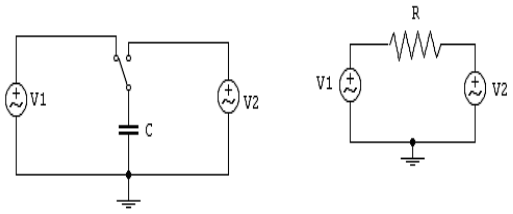

Fig. 1.6: Equivalent resistor model for switched capacitor circuit in Fig. 1.5.

The operation of this circuit is as follows. When the switch in Figure 3.6(a) is thrown to the left, the capacitor will charge up to V1. When the switch is thrown to the right, the capacitor will discharge down to/charge up to V2. As a result of these consecutive switching events, there will be a net charge transfer

$$\Delta Q = C \cdot \Delta V = C \cdot (V1 - V2)$$

Now, if one flips the switch back and forth at a rate of fclk cycles/sec, then the charge transferred in one second is

$$f_{CLK} \cdot \Delta Q = C \cdot f_{CLK} \cdot (V1 - V2)$$

Which has the units of current? The average current,

$$I_{AVG} = C \cdot f_{CLK} \cdot (V1 - V2)$$

If f clk is much higher than the frequency of the voltage waveforms, then the switching process can be taken to be essentially continuous, and the switched-capacitor can then be modelled as an equivalent resistance, as shown below in Figure 1.6(b). The value of the equivalent resistance is given by:

$$\text{Req} = \frac{\text{V1}-\text{V2}}{\text{Iavg}} = \frac{1}{\text{C.fclk}} \qquad (1.8)$$

Therefore, this equivalent resistance, in conjunction with other capacitors, and Op-amp integrators, can be used to synthesize active filters. It is now clear from Equation (1.8) how the use of the switched-capacitor leads to tunability in the active filters, by varying the clock frequency.

This equivalent resistance has features which make it advantageous when realized in integrated-circuit form:

(a) High-value resistors can be implemented in very little silicon area.

(b) Very accurate time constants can be realized, because the time constant is proportional to the ratio of capacitances, and inversely proportional to the clock frequency

$$time\ constant = ReqC1 = \frac{C1}{C.fclk}$$

Capacitor ratios, especially in monolithic form, are very robust against changes in temperature, and clock frequencies can also be strictly controlled, so that accurate time constants are now available in the switched-capacitor technology.

The principal constraint in using the switched-capacitor is that inherent in all sampled-data systems: the clock frequency must be much higher than the critical frequency set by the RC products in the circuit. Furthermore, on either side of the

analog switches, i.e., the MOSFET's, there must be essentially zero-impedance nodes (voltage sources).

1.5 Accuracy of Switched Capacitor Circuits

Frequency or time precision of an analog signal processing circuits is determined by the accuracy of circuit time constants. Consider the simple first order low pass filter

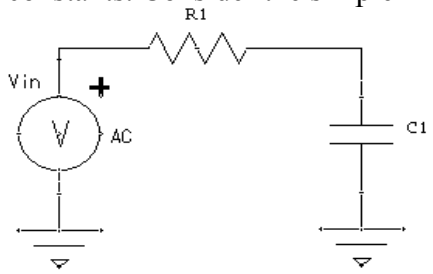

Fig. 1.7: Simple 'RC' low-pass filter.

Transfer function of this circuit in frequency domain:

$$H(jw) = \frac{V2(JW)}{V1(JW)} = \frac{1}{(1+jwR1C1)}$$

$$= \frac{1}{(1+jw\tau)}$$

τ = R1C1

τ = Time Constant

To compare the accuracy of continuous time circuit with discrete time or switched capacitor circuit, let us designate $\tau = \tau c$

Accuracy of τc can be expressed as

$$\underline{d\tau c} = \underline{dR1} + \underline{dC1}$$

$$\tau c \quad R1 \quad C1$$

Accuracy is equal to the sum of accuracy of resistor R1 and accuracy of capacitor C1. In standard CMOS tech. the accuracy of τc can vary between 5 to 20%. This accuracy is insufficient for most signal processing application.

If we replaced R1 by one of switched capacitor circuit. Assume $\tau = \tau d$

$$\tau d = \underline{TC1} = \underline{C1}$$

$$C2 \quad fcC2$$

Accuracy of τd is

$$\underline{d\tau d} = \underline{dC1} - \underline{dC2} - \underline{dfc}$$

$$\tau d\ C1\ C2\ fc$$

Accuracy of discrete time constant τd is equal to relative accuracy of C1 and C2 and clock frequency. Assume that clock frequency is perfectly accurate then accuracy of this circuit can be small as 0.1% in cmos tech. This accuracy is more than sufficient for most signal processing application.

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